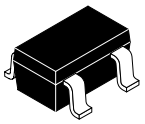


SLVS417B – MARCH 2002 – REVISED OCTOBER 2002

HIGH-EFFICIENCY, SOT23 STEP-DOWN, DC-DC CONVERTER

FEATURES

- **High Efficiency Synchronous Step-Down Converter With up to 95% Efficiency**
- **2.5 V to 6.0 V Input Voltage Range**
- **Adjustable Output Voltage Range From 0.7 V to V_I**
- **Fixed Output Voltage Options Available**
- **Up to 300 mA Output Current**
- **1 MHz Fixed Frequency PWM Operation**
- **Highest Efficiency Over Wide Load Current Range Due to Power Save Mode**
- **15-μA Typical Quiescent Current**
- **Soft Start**
- **100% Duty Cycle Low-Dropout Operation**
- **Dynamic Output-Voltage Positioning**
- **Available in a Tiny 5-Pin SOT23 Package**

APPLICATIONS

- **PDAs and Pocket PC**
- **Cellular Phones, Smart Phones**
- **Low Power DSP Supply**
- **Digital Cameras**
- **Portable Media Players**
- **Portable Equipment**

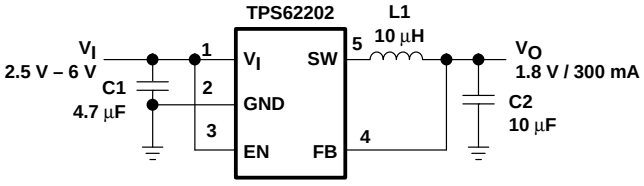
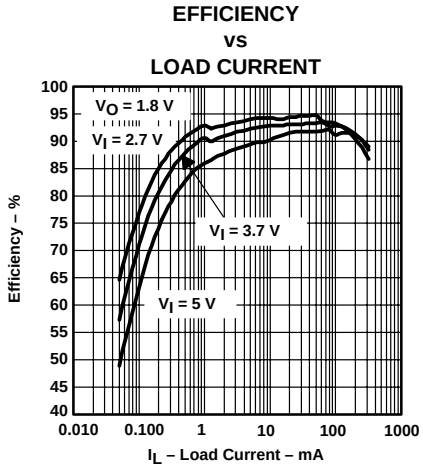


Figure 1. Typical Application (Fixed Output Voltage Version)

DESCRIPTION

The TPS6220x devices are a family of high-efficiency synchronous step-down converters ideally suited for portable systems powered by 1-cell Li-Ion or 3-cell NiMH/NiCd batteries. The devices are also suitable to operate from a standard 3.3-V or 5-V voltage rail.

With an output voltage range of 6.0 V down to 0.7 V and up to 300 mA output current, the devices are ideal to power low voltage DSPs and processors used in PDAs, pocket PCs, and smart phones. Under nominal load current, the devices operate with a fixed switching frequency of typically 1 MHz. At light load currents, the part enters the power save mode operation; the switching frequency is reduced and the quiescent current is typically only 15 μA; therefore it achieves the highest efficiency over the entire load current range. The TPS6220x needs only three small external components. Together with the tiny SOT23 package, a minimum system solution size can be achieved. An advanced fast response voltage mode control scheme achieves superior line and load regulation with small ceramic input and output capacitors.



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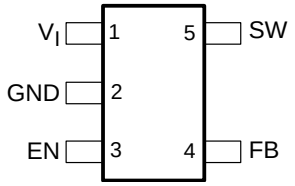
ORDERING INFORMATION†

T_A	OUTPUT VOLTAGE	SOT23 PACKAGE	SYMBOL
–40°C to 85°C	Adjustable	TPS62200DBV	PHKI
	1.5 V	TPS62201DBV	PHLI
	1.6 V	TPS62204DBV	PHSI
	1.8 V	TPS62202DBV	PHMI
	2.5 V	TPS62205DBV	PHTI
	3.3 V	TPS62203DBV	PHNI

† The DBV package is available in tape and reel. Add R suffix (DBVR) to order quantities of 3000 parts. Add T suffix (DBVT) to order quantities of 250 parts

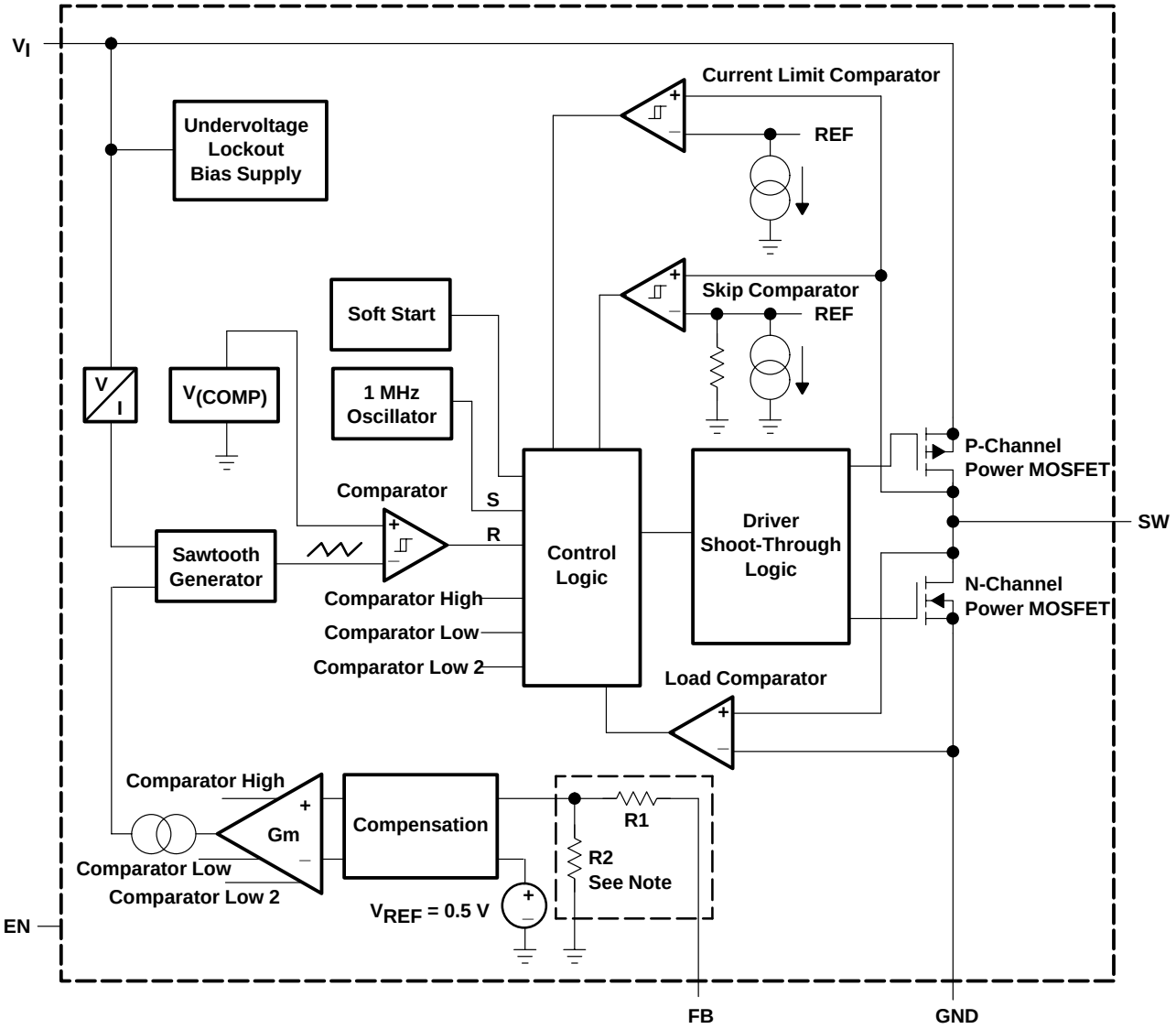
DBV PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
EN	3	I	This is the enable pin of the device. Pulling this pin to ground forces the device into shutdown mode. Pulling this pin to Vin enables the device. This pin must not be left floating and must be terminated.
FB	4	I	This is the feedback pin of the device. Connect this pin directly to the output if the fixed output voltage version is used. For the adjustable version an external resistor divider is connected to this pin. The internal voltage divider is disabled for the adjustable version.
GND	2		Ground
SW	5	I/O	Connect the inductor to this pin. This pin is the switch pin and is connected to the internal MOSFET switches.
V_I	1	I	Supply voltage pin

functional block diagram



NOTE: For the adjustable version (TPS62200) the internal feedback divider is disabled and the FB pin is directly connected to the internal GM amplifier

detailed description

operation

The TPS6220x is a synchronous step-down converter operating with typically 1MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents and in power save mode operating with pulse frequency modulation (PFM) at light load currents.

During PWM operation the converter uses a unique fast response, voltage mode, controller scheme with input voltage feed forward. This achieves good line and load regulation and allows the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal (S), the P-channel MOSFET switch is turned on, and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator also turns off the switch in case the current limit of the P-channel switch is exceeded. Then the N-channel rectifier switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock signal again turning off the N-channel rectifier and turning on the P-channel switch.

The GM amplifier and input voltage determines the rise time of the Sawtooth generator; therefore any change in input voltage or output voltage directly controls the duty cycle of the converter. This gives a very good line and load transient regulation.

power save mode operation

As the load current decreases, the converter enters the power save mode operation. During power save mode, the converter operates with reduced switching frequency in PFM mode and with a minimum quiescent current to maintain high efficiency.

Two conditions allow the converter to enter the power save mode operation. One is when the converter detects the discontinuous conduction mode. The other is when the peak switch current in the P-channel switch goes below the skip current limit. The typical skip current limit can be calculated as

$$I_{skip} \leq 66\ mA + \frac{Vin}{160\ \Omega}$$

During the power save mode the output voltage is monitored with the comparator by the thresholds comp low and comp high. As the output voltage falls below the comp low threshold set to typically 0.8% above Vout nominal, the P-channel switch turns on. The P-channel switch is turned off as the peak switch current is reached. The typical peak switch current can be calculated:

$$I_{peak} = 66\ mA + \frac{Vin}{80\ \Omega}$$

The N-channel rectifier is turned on and the inductor current ramps down. As the inductor current approaches zero the N-channel rectifier is turned off and the P-channel switch is turned on again, starting the next pulse. The converter continues these pulses until the comp high threshold (set to typically 1.6% above Vout nominal) is reached. The converter enters a sleep mode, reducing the quiescent current to a minimum. The converter wakes up again as the output voltage falls below the comp low threshold again. This control method reduces the quiescent current typically to 15 μA and reduces the switching frequency to a minimum, thereby achieving the high converter efficiency. Setting the skip current thresholds to typically 0.8% and 1.6% above the nominal output voltage at light load current results in a dynamic output voltage achieving lower absolute voltage drops during heavy load transient changes. This allows the converter to operate with a small output capacitor of just 10 μF and still have a low absolute voltage drop during heavy load transient changes. Refer to Figure 2 for detailed operation of the power save mode.

power save mode operation (continued)

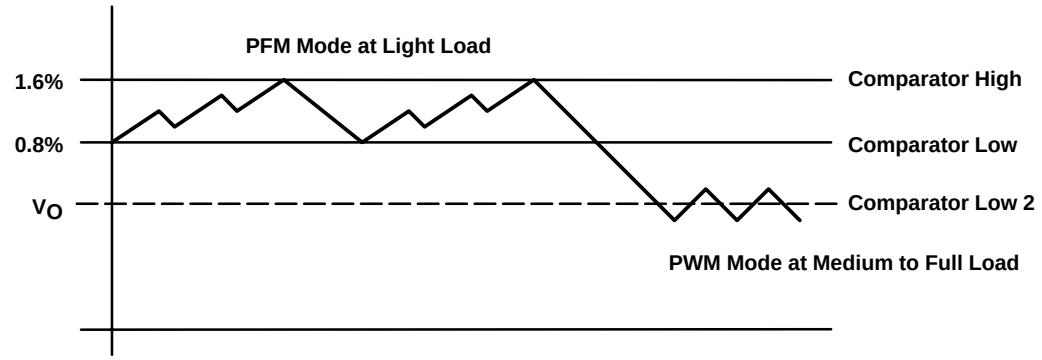


Figure 2. Power Save Mode Thresholds and Dynamic Voltage Positioning

The converter enters the fixed frequency PWM mode again as soon as the output voltage falls below the comp low 2 threshold.

dynamic voltage positioning

As described in the power save mode operation sections and as detailed in Figure 2, the output voltage is typically 0.8% above the nominal output voltage at light load currents, as the device is in power save mode. This gives additional headroom for the voltage drop during a load transient from light load to full load. During a load transient from full load to light load, the voltage overshoot is also minimized due to active regulation turning on the N-channel rectifier switch.

soft start

The TPS6220x has an internal soft start circuit that limits the inrush current during start-up. This prevents possible voltage drops of the input voltage in case a battery or a high impedance power source is connected to the input of the TPS6220x.

The soft start is implemented as a digital circuit increasing the switch current in steps of typically 60 mA, 120 mA, 240 mA and then the typical switch current limit of 480 mA. Therefore the start-up time mainly depends on the output capacitor and load current. Typical start-up time with 10 µF output capacitor and 200 mA load current is 800 µs.

low dropout operation 100% duty cycle

The TPS6220x offers a low input to output voltage difference, while still maintaining operation with the 100% duty cycle mode. In this mode, the P-channel switch is constantly turned on. This is particularly useful in battery powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain regulation, depending on the load current and output voltage, can be calculated as

$$Vin_{min} = Vout_{max} + Iout_{max} \times \left(r_{ds}(ON)_{max} + R_L \right)$$

$Iout_{max}$ = maximum output current plus inductor ripple current
$r_{ds}(ON)_{max}$ = maximum P-channel switch $r_{ds}(ON)$
R_L = DC resistance of the inductor
$Vout_{max}$ = nominal output voltage plus maximum output voltage tolerance

detailed description (continued)

enable

Pulling the enable low forces the part into shutdown, with a shutdown quiescent current of typically 0.1 μA. In this mode, the P-channel switch and N-channel rectifier are turned off, the internal resistor feedback divider is disconnected, and the whole device is in shutdown mode. If an output voltage, which could be an external voltage source or super cap, is present during shutdown, the reverse leakage current is specified under electrical characteristics. For proper operation the enable pin must be terminated and must not be left floating.

Pulling the enable high starts up the TPS6220x with the soft start as previously described.

undervoltage lockout

The undervoltage lockout circuit prevents the device from misoperation at low input voltages. It prevents the converter from turning on the switch or rectifier MOSFET under undefined conditions.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltages, V_I (see Note 1) . . . . . –0.3 V to 7.0 V
Voltages on pins SW, EN, FB (see Note 1) . . . . . –0.3 V to V_{CC} +0.3 V
Continuous power dissipation, P_D . . . . . See Dissipation Rating Table
Operating junction temperature range, T_J . . . . . –40°C to 85°C
Storage temperature, T_{stg} . . . . . –65°C to 150°C
Lead temperature (soldering, 10 sec) . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DBV	357 mW	35 mW/°C	192 mW	140 mW

NOTE: The thermal resistance junction to ambient of the 5-pin SOT23 is 250°C/W.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_I	2.5		6.0	V
Output voltage range for adjustable output voltage version, V_O	0.7		V_I	V
Output current, I_O			300	mA
Inductor, L (see Note 2)		10		μH
Input capacitor, C_I (see Note 2)		4.7		μF
Output capacitor, C_O (see Note 2)		10		μF
Operating ambient temperature, T_A	–40		85	°C
Operating junction temperature, T_J	–40		125	°C

NOTE 2: Refer to application section for further information

electrical characteristics, V_I = 3.6 V, V_O = 1.8 V, I_O = 200 mA, EN = VIN, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

supply current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I	Input voltage range		2.5		6.0	V
I_Q	Operating quiescent current	I_O = 0 mA, Device is not switching		15	30	µA
	Shutdown supply current	EN = GND		0.1	1	µA
	Undervoltage lockout threshold		1.5		2.0	V

enable

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(EN)}$	EN high level input voltage		1.3			V
	EN low level input voltage				0.4	V
$I_{(EN)}$	EN input bias current	EN = GND or VIN		0.01	0.1	µA

power switch

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$r_{ds(ON)}$	P-channel MOSFET on-resistance	V_{IN} = V_{GS} = 3.6 V		530	690	mΩ
		V_{IN} = V_{GS} = 2.5 V		670	850	
	N-channel MOSFET on-resistance	V_{IN} = V_{GS} = 3.6 V		430	540	mΩ
		V_{IN} = V_{GS} = 2.5 V		530	660	
$I_{lkg\_(P)}$	P-channel leakage current	V_{DS} = 6.0 V		0.1	1	µA
$I_{lkg\_(N)}$	N-channel leakage current	V_{DS} = 6.0 V		0.1	1	µA
$I_{(LIM)}$	P-channel current limit	2.5 V < Vin < 6.0 V	380	480	670	mA

oscillator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_S	Switching frequency		650	1000	1500	kHz

electrical characteristics, V_I = 3.6 V, V_O = 1.8 V, I_O = 200 mA, EN = VIN, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

output

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Adjustable output voltage range	TPS62200		0.7		V_{IN}	V
V_{ref}	Reference voltage				0.5		V
	Feedback voltage, See Note 3	TPS62200	V_I = 3.6 V to 6.0 V, I_O = 0 mA	0%		3%	
		Adjustable	V_I = 3.6 V to 6.0 V, 0 mA ≤ I_O ≤ 300 mA	–3%		3%	
V_O	Fixed output voltage	TPS62201	V_I = 2.5 V to 6.0 V, I_O = 0 mA	0%		3%	
		1.5V	V_I = 2.5 V to 6.0 V, 0 mA ≤ I_O ≤ 300 mA	–3%		3%	
		TPS62204	V_I = 2.5 V to 6.0 V, I_O = 0 mA	0%		3%	
		1.6V	V_I = 2.5 V to 6.0 V, 0 mA ≤ I_O ≤ 300 mA	–3%		3%	
		TPS62202	V_I = 2.5 V to 6.0 V, I_O = 0 mA	0%		3%	
		1.8V	V_I = 2.5 V to 6.0 V, 0 mA ≤ I_O ≤ 300 mA	–3%		3%	
		TPS62205	V_I = 2.7 V to 6.0 V, I_O = 0 mA	0%		3%	
		2.5V	V_I = 2.7 V to 6.0 V, 0 mA ≤ I_O ≤ 300 mA	–3%		3%	
		TPS62203	V_I = 3.6 V to 6.0 V, I_O = 0 mA	0%		3%	
		3.3V	V_I = 3.6 V to 6.0 V, 0 mA ≤ I_O ≤ 300 mA	–3%		3%	
	Line regulation		V_I = 2.5 V to 6.0 V, I_O = 10 mA		0.26		%/V
	Load regulation		I_O = 100 mA to 300 mA		0.0014		%/mA
I_{lkg}	Leakage current into SW pin		Vin > Vout, 0 V ≤ Vsw ≤ Vin		0.1	1	µA
I_{lkg}(Rev)	Reverse leakage current into pin SW		Vin = open, EN=GND, V_{SW} = 6.0 V		0.1	1	µA

NOTE 3: For output voltages ≤1.2 V and 22 µF output capacitor value is required to achieve a maximum output voltage accuracy of 3% while operating in power save mode (PFM mode)

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
η	Efficiency	vs Load current	3,4,5
		vs Input voltage	6
I_Q	No load quiescent current	vs Input voltage	7
f_s	Switching frequency	vs Temperature	8
V_o	Output voltage	vs Output current	9
r_{ds}(on)	r_{ds}(on) – P-channel switch,	vs Input voltage	10
	r_{ds}(on) – N-Channel rectifier switch	vs Input voltage	11
	Line transient response		12
	Load transient response		13
	Power save mode operation		14
	Start-up		15

TYPICAL CHARACTERISTICS

EFFICIENCY
vs
LOAD CURRENT

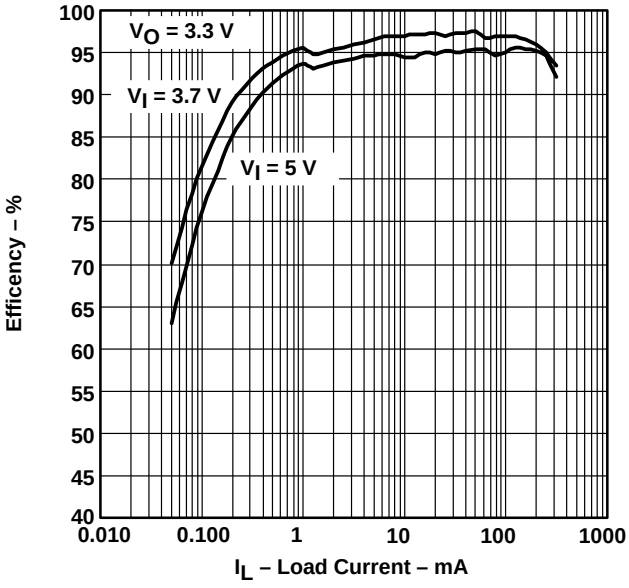


Figure 3

EFFICIENCY
vs
LOAD CURRENT

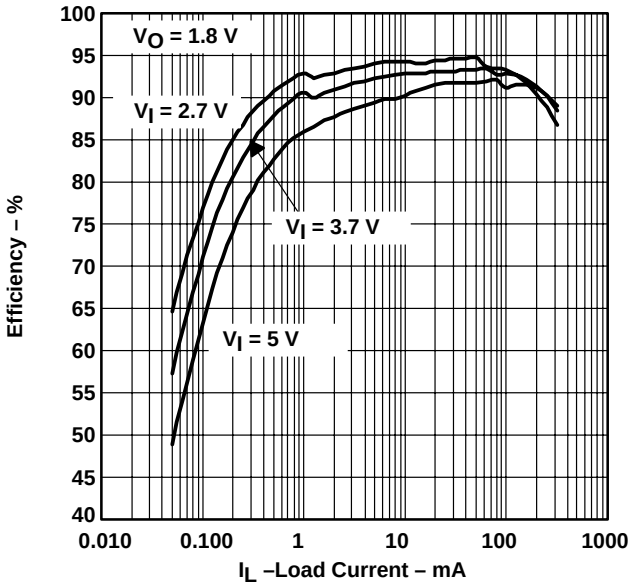


Figure 4

EFFICIENCY
vs
LOAD CURRENT

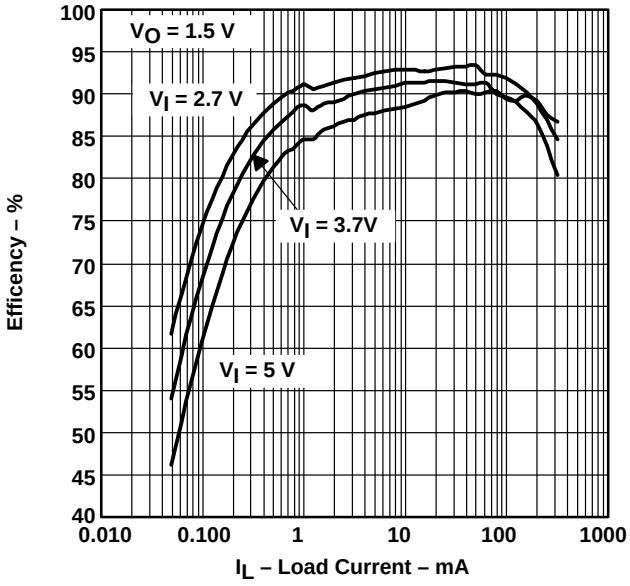


Figure 5

EFFICIENCY
vs
INPUT VOLTAGE

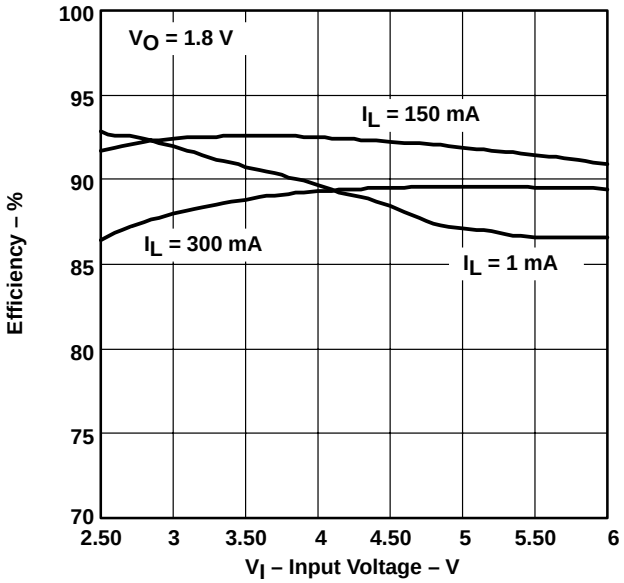


Figure 6

TYPICAL CHARACTERISTICS

NO LOAD QUIESCENT CURRENT
vs
INPUT VOLTAGE

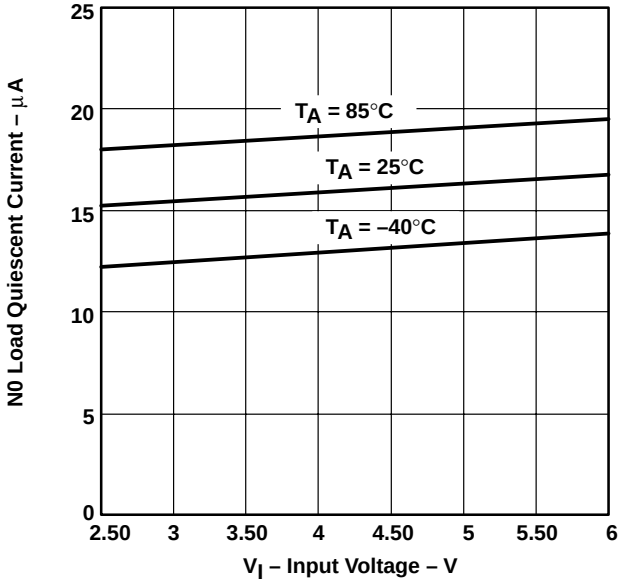


Figure 7

FREQUENCY
vs
TEMPERATURE

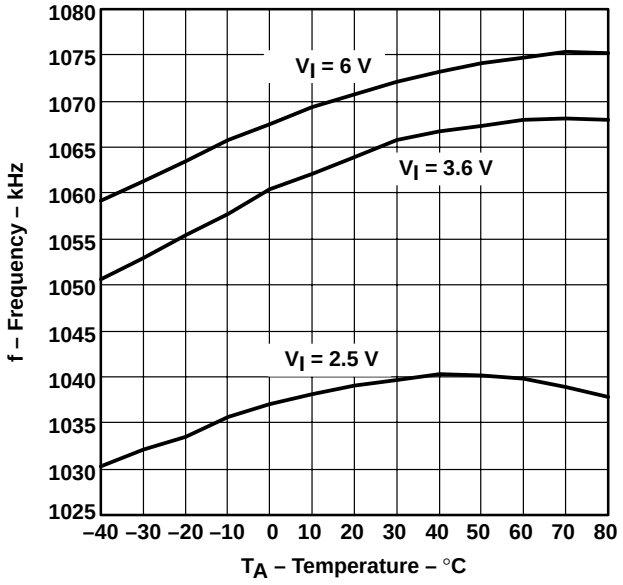


Figure 8

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

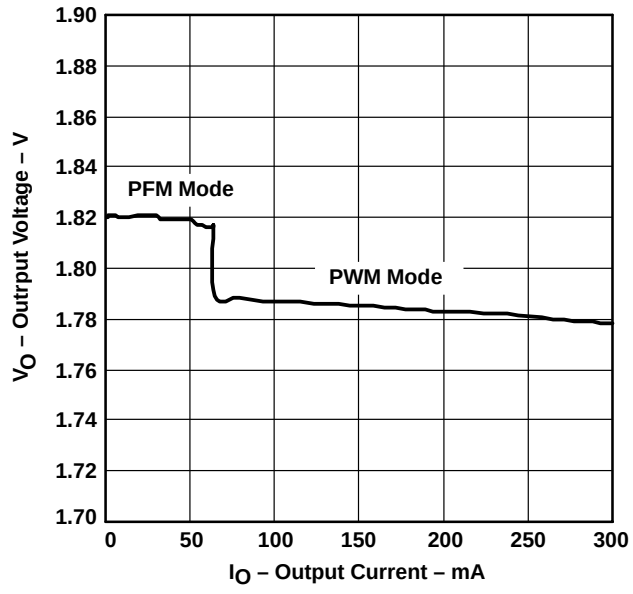


Figure 9

r_{ds}(on) P-CHANNEL SWITCH
vs
INPUT VOLTAGE

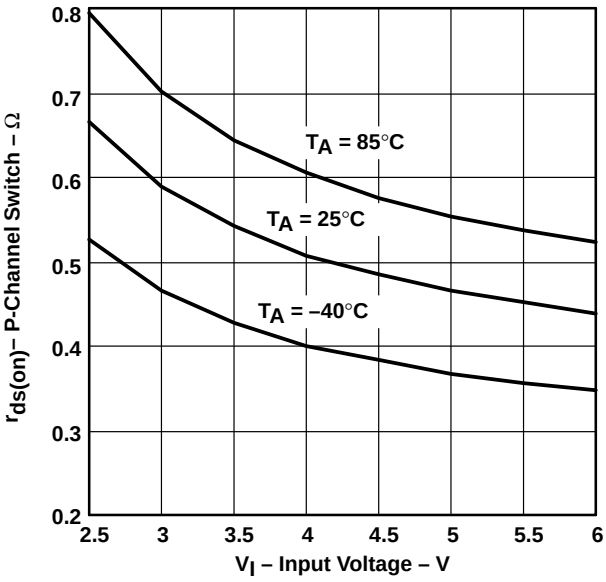


Figure 10

TYPICAL CHARACTERISTICS

$r_{ds}(on)$ N-CHANNEL SWITCH vs INPUT VOLTAGE

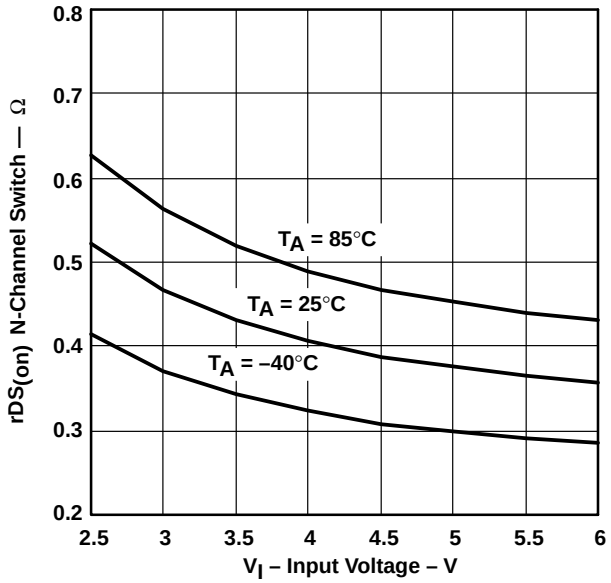


Figure 11

LINE TRANSIENT RESPONSE

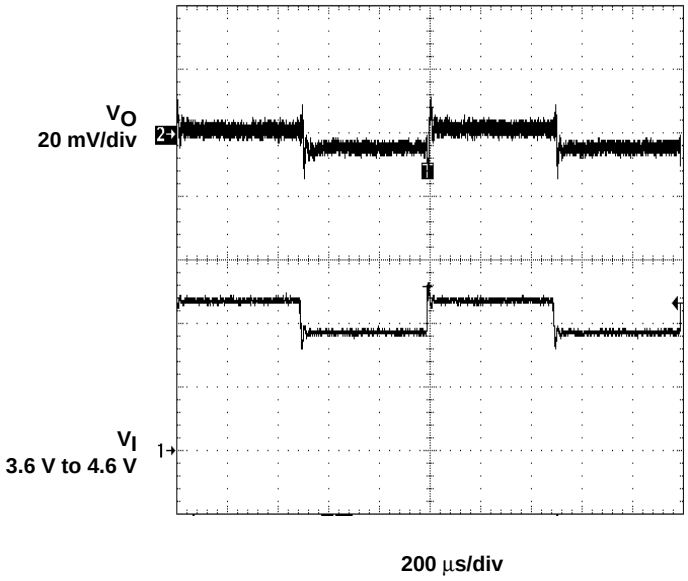


Figure 12

TYPICAL CHARACTERISTICS

LOAD TRANSIENT RESPONSE

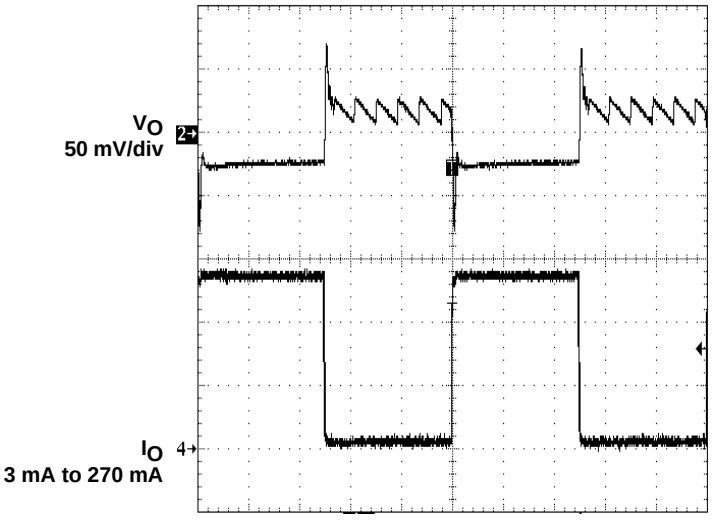


Figure 13

POWER SAVE MODE OPERATION

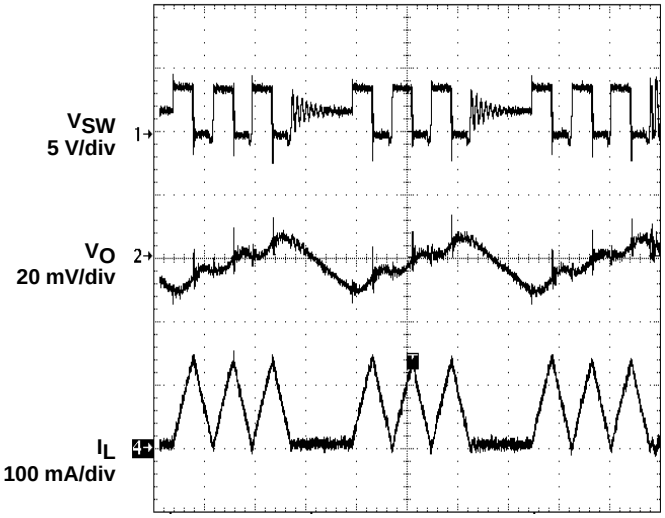


Figure 14

TYPICAL CHARACTERISTICS

START-UP

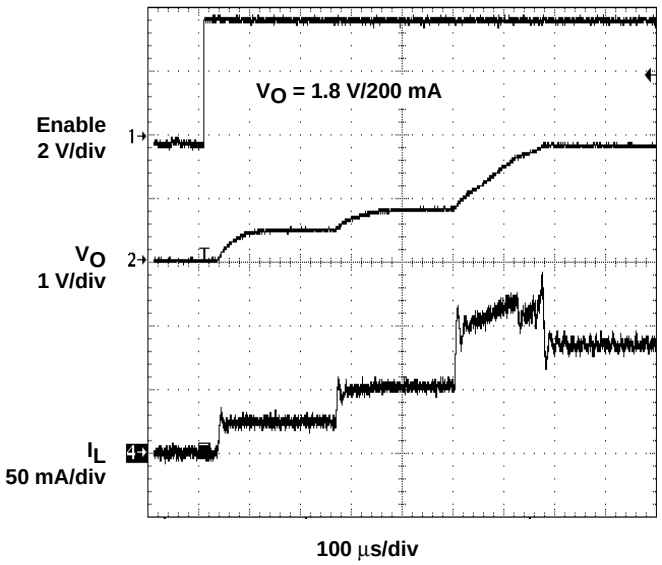


Figure 15

APPLICATION INFORMATION

adjustable output voltage version

When the adjustable output voltage version TPS62200 is used, the output voltage is set by the external resistor divider. See Figure 16.

The output voltage is calculated as

$$V_{out} = 0.5\ V \times \left(1 + \frac{R1}{R2}\right)$$

R1 + R2 ≤ 1 MΩ and internal reference voltage V(ref)typ = 0.5 V

R1 + R2 should not be greater than 1 MΩ for reasons of stability. To keep the operating quiescent current to a minimum, the feedback resistor divider should have high impedance with R1+R2 ≤ 1 MΩ. Because of the high impedance and the low reference voltage of V_{ref} = 0.5 V, the noise on the feedback pin (FB) needs to be minimized. Using a capacitive divider C1 and C2 across the feedback resistors minimizes the noise at the feedback without degrading the line or load transient performance.

C1 and C2 should be selected as

$$C1 = \frac{1}{2 \times \pi \times 10\ kHz \times R1}$$

R1 = upper resistor of voltage divider
C1 = upper capacitor of voltage divider

For C1 a value should be chosen that comes closest to the calculated result.

$$C2 = \frac{R1}{R2} \times C1$$

R2 = lower resistor of voltage divider
C2 = lower capacitor of voltage divider

For C2 the selected capacitor value should always be selected larger than the calculated result. For example, in Figure 16 for C2, 100 pF are selected for a calculated result of C2 = 86.17 pF.

If quiescent current is not a key design parameter, C1 and C2 can be omitted, and a low-impedance feedback divider must be used with R1+R2 <100 kΩ. This design reduces the noise available on the feedback pin (FB) as well, but increases the overall quiescent current during operation.

APPLICATION INFORMATION

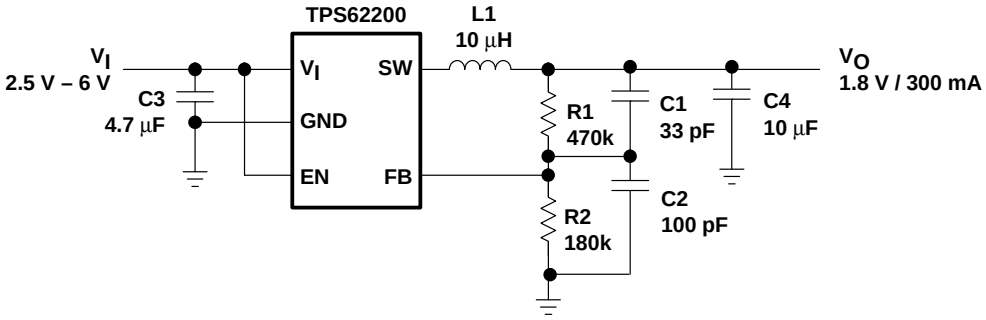


Figure 16. Typical Application Circuit for the Adjustable Output Voltage

inductor selection

The TPS6220x device is optimized to operate with a typical inductor value of 10 µH.

For high efficiencies, the inductor should have a low dc resistance to minimize conduction losses. Although the inductor core material has less effect on efficiency than its dc resistance, an appropriate inductor core material must be used.

The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current, and the lower the conduction losses of the converter. On the other hand, larger inductor values cause a slower load transient response. Usually the inductor ripple current, as calculated below, is around 20% of the average output current.

In order to avoid saturation of the inductor, the inductor should be rated at least for the maximum output current of the converter plus the inductor ripple current that is calculated as

$$\Delta I_L = Vout \times \frac{1-\frac{Vout}{Vin}}{L \times f} \qquad I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2}$$

f = switching frequency (1 MHz typical, 650 kHz minimal)

L = inductor valfue

ΔI_L = peak-to-peak inductor ripple current

I_{Lmax} = maximum inducator current

The highest inductor current occurs at maximum Vin.

A more conservative approach is to select the inductor current rating just for the maximum switch current of 670 mA. Refer to Table1 for inductor recommendations.

APPLICATION INFORMATION

Table 1. Recommended Inductors

INDUCTOR VALUE	COMPONENT SUPPLIER	COMMENTS
10 µH 10 µH 10 µH 10 µH	Sumida CDRH5D28–100 Sumida CDRH5D18–100 Sumida CDRH4D28–100 Coilcraft DO1608–103	High efficiency
6.8 µH 10 µH 10 µH 10 µH 10 µH	Sumida CDRH3D16–6R8 Sumida CDRH4D18–100 Sumida CR32–100 Sumida CR43–100 Murata LQH4C100K04	Smallest solution

input capacitor selection

Because the buck converter has a pulsating input current, a low ESR input capacitor is required. This results in the best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. Also the input capacitor must be sufficiently large to stabilize the input voltage during heavy load transients.

For good input voltage filtering, usually a 4.7 µF input capacitor is sufficient. It can be increased without any limit for better input-voltage filtering.

input capacitor selection (continued)

If ceramic output capacitors are used, the capacitor RMS ripple current rating always meets the application requirements. For completeness, the RMS ripple current is calculated as

$$I_{RMS} = I_{outmax} \times \sqrt{\frac{Vout}{Vin} \times \left(1 - \frac{Vout}{Vin}\right)}$$

The worst case RMS ripple current occurs at D=0.5 and is calculated as

$$I_{RMS} = \frac{Iout}{2}$$

Ceramic capacitors show a good performance because of the low ESR value, and they are less sensitive against voltage transients and spikes compared to tantalum capacitors.

Place the input capacitor as close as possible to the input pin of the device for best performance (refer to Table 2 for recommended components).

output capacitor selection

The advanced fast response voltage mode control scheme of the TPS6220x allows the use of tiny ceramic capacitors with a value of 10 µF without having large output voltage under and overshoots during heavy load transients.

Ceramic capacitors with low ESR values have the lowest output voltage ripple and are therefore recommended. If required, tantalum capacitors may be used as well (refer to Table 2 for recommended components).

If ceramic output capacitors are used, the capacitor RMS ripple current rating always meets the application requirements. Just for completeness the RMS ripple current is calculated as

$$I_{RMSCout} = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \frac{1}{2 \times \sqrt{3}}$$

APPLICATION INFORMATION

At nominal load current the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta Vout = Vout \times \frac{1-\frac{Vout}{Vin}}{L \times f} \times \left(\frac{1}{8 \times Cout \times f} + ESR\right)$$

where the highest output voltage ripple occurs at the highest input voltage Vin.

At light load currents, the device operates in power save mode, and the output voltage ripple is independent of the output capacitor value. The output voltage ripple is set by the internal comparator thresholds. The typical output voltage ripple is 1% of the output voltage Vo.

Table 2. Recommended Capacitors

CAPACITOR VALUE	CASE SIZE	COMPONENT SUPPLIER	COMMENTS
4.7 µF	0805	Taiyo Yuden JMK212BY475MG	Ceramic
10 µF	0805	Taiyo Yuden JMK212BJ106MG TDK C12012X5ROJ106K	Ceramic Ceramic
10 µF	1206	Taiyo Yuden JMK316BJ106KL TDK C3216X5ROJ106M	Ceramic
22 µF	1210	Taiyo Yuden JMK325BJ226MM	Ceramic

layout considerations

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator shows stability problems as well as EMI problems.

Therefore use wide and short traces for the main current paths, as indicated in bold in Figure 17. The input capacitor, as well as the inductor and output capacitor, should be placed as close as possible to the IC pins

The feedback resistor network must be routed away from the inductor and switch node to minimize noise and magnetic interference. To further minimize noise from coupling into the feedback network and feedback pin, the ground plane or ground traces must be used for shielding. This becomes very important especially at high switching frequencies of 1 MHz.

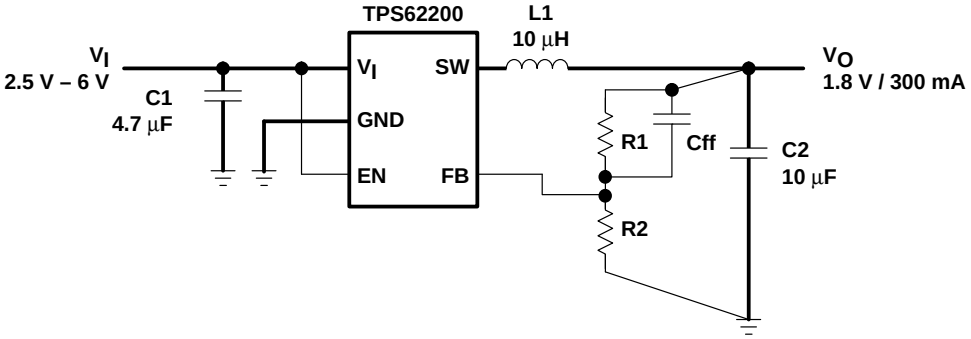
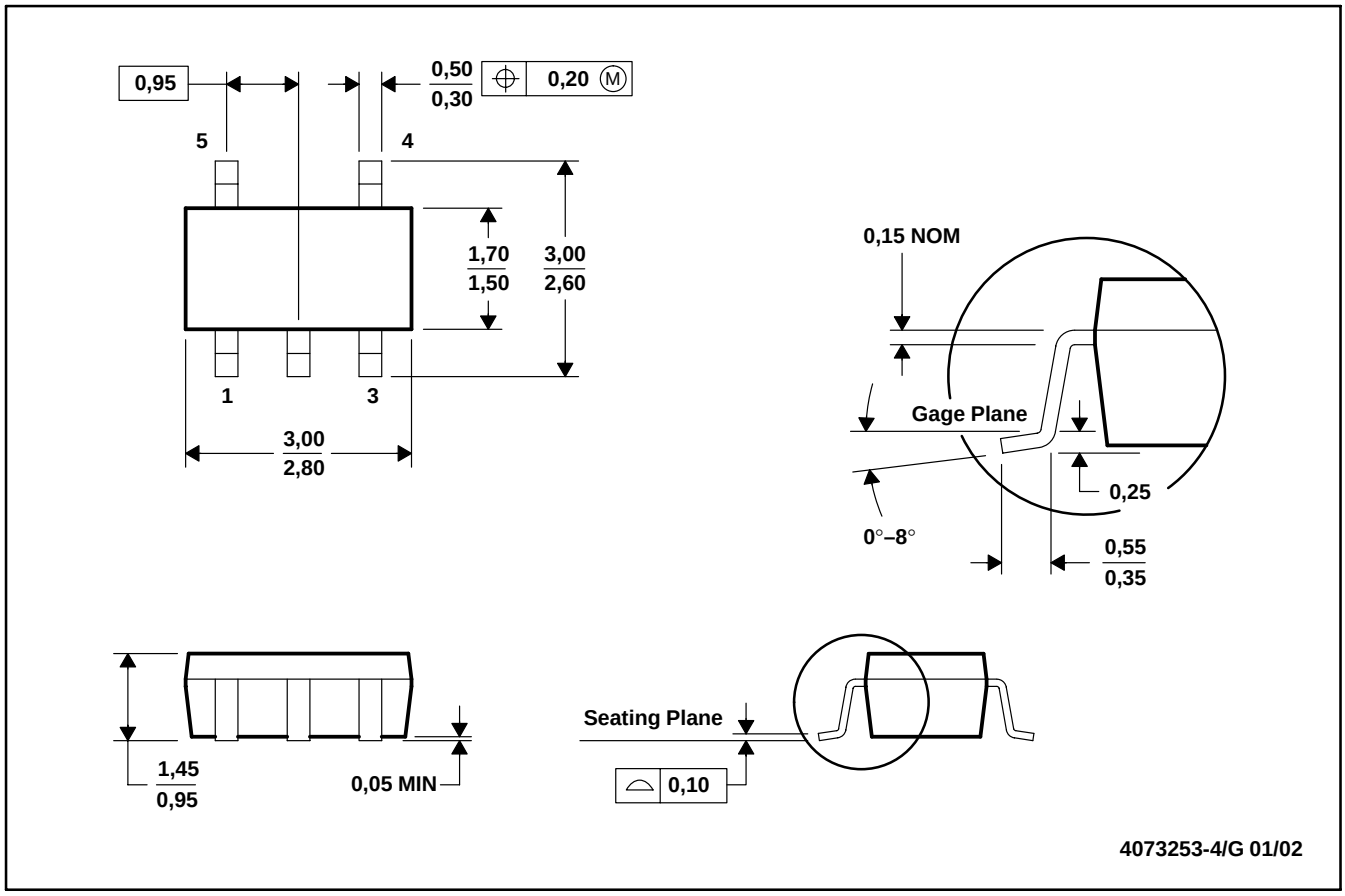


Figure 17. Layout Diagram

MECHANICAL DATA

DBV (R-PDSO-G5) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-178

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