STEREO DIGITAL AMPLIFIER POWER STAGE

TM

FEATURES

- 2×125 W at 10% THD+N Into 4-Ω BTL
- 2×98 W at 10% THD+N Into 6-Ω BTL
- 2×76 W at 10% THD+N Into 8-Ω BTL
- 4×45 W at 10% THD+N Into 3-Ω SE
- 4×35 W at 10% THD+N Into 4-Ω SE
- 1×192 W at 10% THD+N Into 3-Ω PBTL
- 1×240 W at 10% THD+N Into 2-Ω PBTL
- >100 dB SNR (A-Weighted)
- <0.1% THD+N at 1 W
- Thermally Enhanced Package Option:
  - DKD (36-Pin PSOP3)
- High-Efficiency Power Stage (>90%) With 140-mΩ Output MOSFETs
- Power-On Reset for Protection on Power Up Without Any Power-Supply Sequencing
- Integrated Self-Protection Circuits Including:
  - Undervoltage
  - Overtemperature
  - Overload
  - Short Circuit
- Error Reporting
- EMI Compliant When Used With Recommended System Design
- Intelligent Gate Drive

APPLICATIONS

- Mini/Micro Audio System
- DVD Receiver
- Home Theater

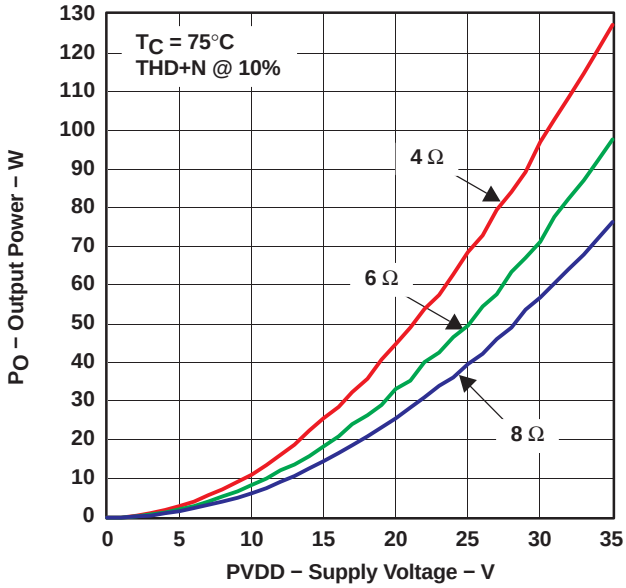
DESCRIPTION

The TAS5152 is a third-generation, high-performance, integrated stereo digital amplifier power stage with improved protection system. The TAS5152 is capable of driving a 4-Ω bridge-tied load (BTL) at up to 125 W per channel with low integrated noise at the output, low THD+N performance, and low idle power dissipation.

A low-cost, high-fidelity audio system can be built using a TI chipset, comprised of a modulator (e.g., TAS5508) and the TAS5152. This system only requires a simple passive LC demodulation filter to deliver high-quality, high-efficiency audio amplification with proven EMI compliance. This device requires two power supplies, 12 V for GVDD and VDD, and 35 V for PVDD. The TAS5152 does not require power-up sequencing due to internal power-on reset. The efficiency of this digital amplifier is greater than 90% into 6 Ω, which enables the use of smaller power supplies and heatsinks.

The TAS5152 has an innovative protection system integrated on-chip, safeguarding the device against a wide range of fault conditions that could damage the system. These safeguards are short-circuit protection, overcurrent protection, undervoltage protection, and overtemperature protection. The TAS5152 has a new proprietary current-limiting circuit that reduces the possibility of device shutdown during high-level music transients. A new programmable overcurrent detector allows the use of lower-cost inductors in the demodulation output filter.

BTL OUTPUT POWER vs SUPPLY VOLTAGE



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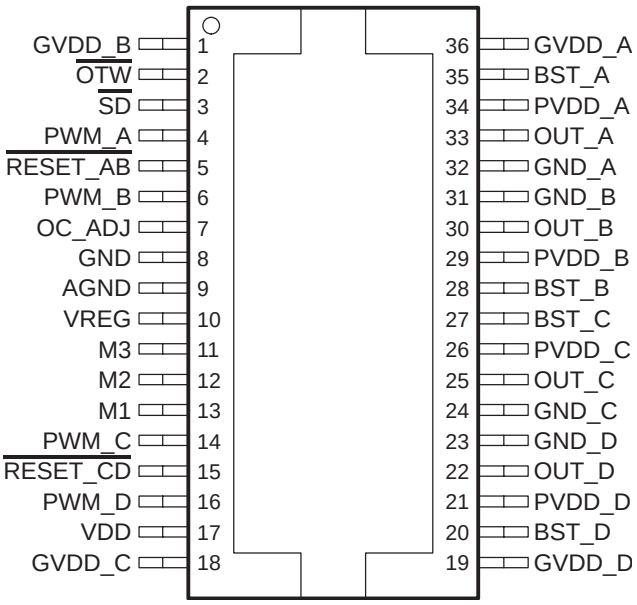
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

GENERAL INFORMATION

The TAS5152 is available in a 36-pin PSOP3 (DKD) thermally enhanced package. The package contains a heat slug that is located on the top side of the device for convenient thermal coupling to the heatsink.

DKD PACKAGE
(TOP VIEW)



MODE Selection Pins

MODE PINS			PWM INPUT	OUTPUT CONFIGU-RATION	PROTECTION SCHEME
M3	M2	M1			
0	0	0	2N (1) AD/BD modulation	2 channels BTL output	BTL mode (2)
0	0	1	Reserved		
0	1	0	1N (1) AD modulation	2 channels BTL output	BTL mode (2)
0	1	1	1N (1) AD modulation	1 channel PBTL output	PBTL mode. Only PWM_A input is used.
1	0	0	1N (1) AD modulation	4 channels SE output	Protection works similarly to BTL mode (2). Only difference in SE mode is that OUT_x is Hi-Z instead of a pulldown through internal pulldown resistor.
1	0	1	Reserved		
1	1	0			
1	1	1			

(1) The 1N and 2N naming convention is used to indicate the required number of PWM lines to the power stage per channel in a specific mode.

(2) An overload protection (OLP) occurring on A or B causes both channels to shut down. An OLP on C or D works similarly. Global errors like overtemperature error (OTE), undervoltage protection (UVP) and power-on reset (POR) affect all channels.

Package Heat Dissipation Ratings (1)

PARAMETER	TAS5152DKD
$R_{\theta JC}$ (°C/W)—2 BTL or 4 SE channels (8 transistors)	1.28
$R_{\theta JC}$ 〈°C/W)—1 BTL or 2 SE channel(s) (4 transistors)	2.56
$R_{\theta JC}$ (°C/W)—(1 transistor)	8.6
Pad area (2)	80 mm^2

(1) JC is junction-to-case, CH is case-to-heatsink.

(2) $R_{\theta CH}$ is an important consideration. Assume a 2-mil thickness of typical thermal grease between the pad area and the heatsink. The $R_{\theta CH}$ with this condition is 0.8°C/W for the DKD package and 1.8°C/W for the DDV package.

Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1)

TAS5152	
VDD to AGND	–0.3 V to 13.2 V
GVDD_X to AGND	–0.3 V to 13.2 V
PVDD_X to GND_X (2)	–0.3 V to 50 V
OUT_X to GND_X (2)	–0.3 V to 50 V
BST_X to GND_X (2)	–0.3 V to 63.2 V
VREG to AGND	–0.3 V to 4.2 V
GND_X to GND	–0.3 V to 0.3 V
GND_X to AGND	–0.3 V to 0.3 V
GND to AGND	–0.3 V to 0.3 V
PWM_X, OC_ADJ, M1, M2, M3 to AGND	–0.3 V to 4.2 V
$\overline{\text{RESET\_X}}$, $\overline{\text{SD}}$, $\overline{\text{OTW}}$ to AGND	–0.3 V to 7 V
Maximum continuous sink current ($\overline{\text{SD}}$, $\overline{\text{OTW}}$)	9 mA
Maximum operating junction temperature range, T_J	0°C to 125°C
Storage temperature	–40°C to 125°C
Lead temperature, 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Minimum pulse width low	50 ns

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) These voltages represent the dc voltage + peak ac waveform measured at the terminal of the device in all conditions.

Ordering Information

T_A	PACKAGE	DESCRIPTION
0°C to 70°C	TAS5152DKD	36-pin PSOP3

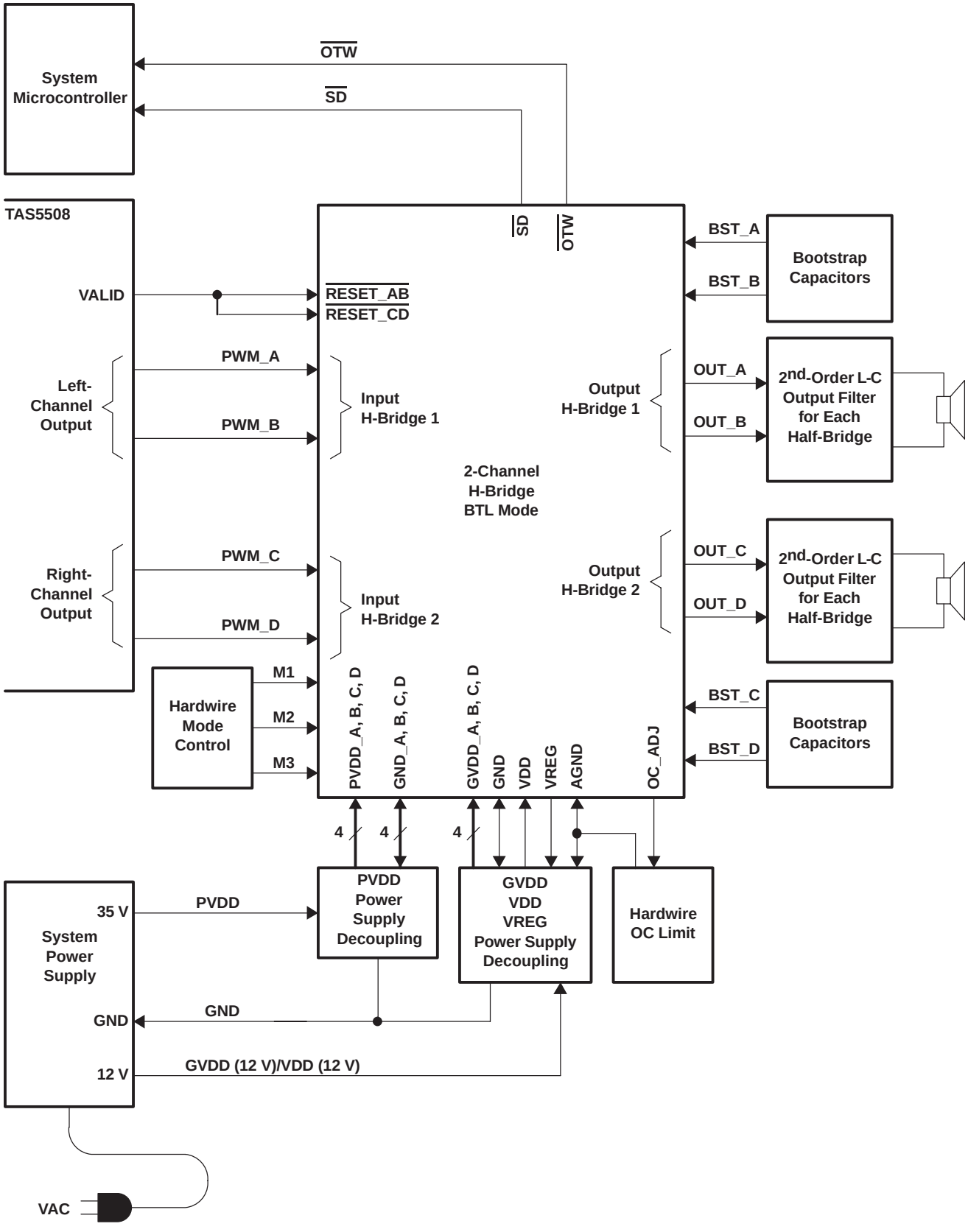
For the most current specification and package information, see the TI Web site at www.ti.com.

Terminal Functions

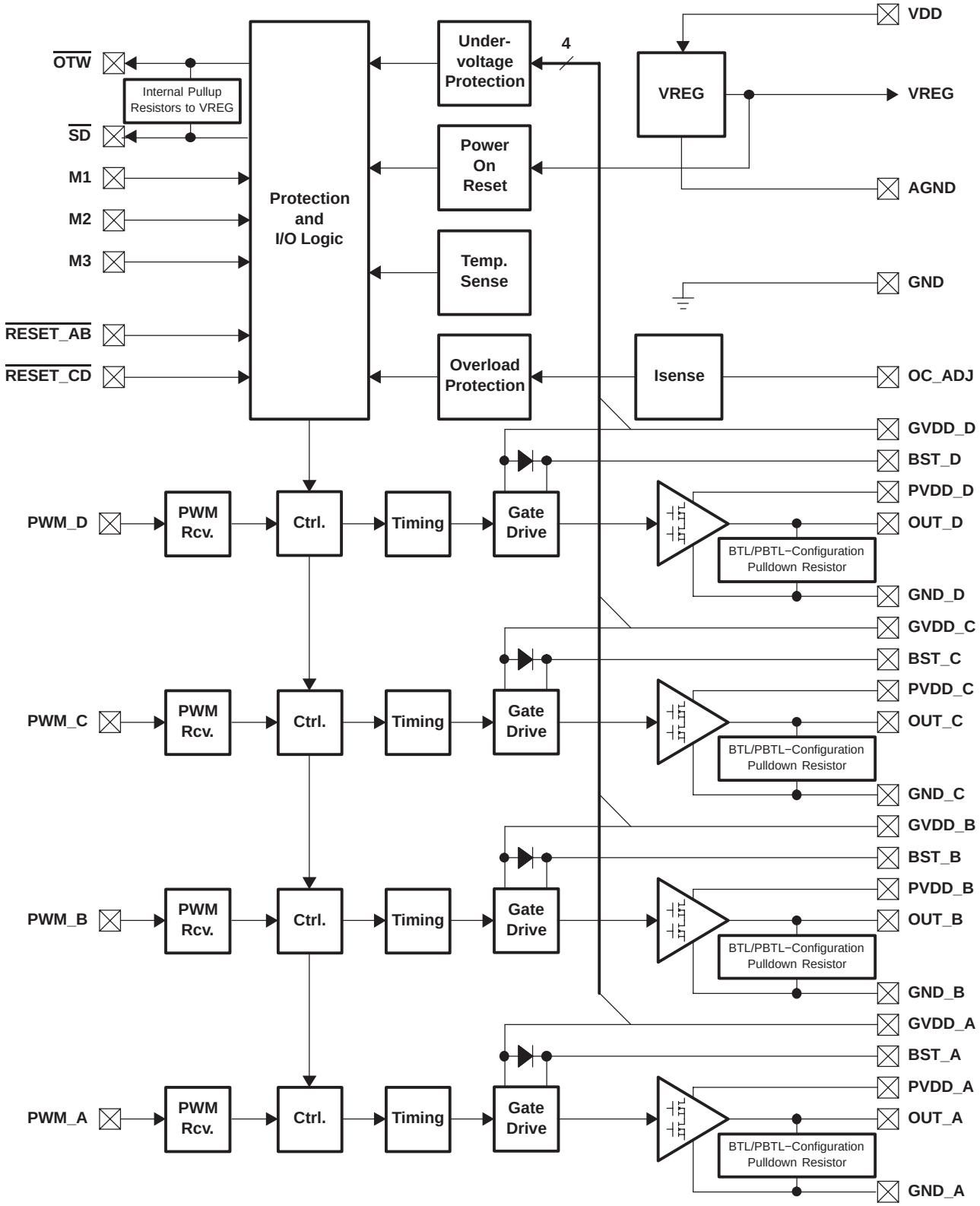
TERMINAL		FUNCTION (1)	DESCRIPTION
NAME	NO.		
AGND	9	P	Analog ground
BST_A	35	P	HS bootstrap supply (BST), external capacitor to OUT_A required
BST_B	28	P	HS bootstrap supply (BST), external capacitor to OUT_B required
BST_C	27	P	HS bootstrap supply (BST), external capacitor to OUT_C required
BST_D	20	P	HS bootstrap supply (BST), external capacitor to OUT_D required
GND	8	P	Ground
GND_A	32	P	Power ground for half-bridge A
GND_B	31	P	Power ground for half-bridge B
GND_C	24	P	Power ground for half-bridge C
GND_D	23	P	Power ground for half-bridge D
GVDD_A	36	P	Gate-drive voltage supply requires 0.1-μF capacitor to AGND
GVDD_B	1	P	Gate-drive voltage supply requires 0.1-μF capacitor to AGND
GVDD_C	18	P	Gate-drive voltage supply requires 0.1-μF capacitor to AGND
GVDD_D	19	P	Gate-drive voltage supply requires 0.1-μF capacitor to AGND
M1	13	I	Mode selection pin
M2	12	I	Mode selection pin
M3	11	I	Mode selection pin
OC_ADJ	7	O	Analog overcurrent programming pin requires resistor to ground
$\overline{\text{OTW}}$	2	O	Overtemperature warning signal, open drain, active-low
OUT_A	33	O	Output, half-bridge A
OUT_B	30	O	Output, half-bridge B
OUT_C	25	O	Output, half-bridge C
OUT_D	22	O	Output, half-bridge D
PVDD_A	34	P	Power supply input for half-bridge A requires close decoupling of 0.1-μF capacitor to GND_A
PVDD_B	29	P	Power supply input for half-bridge B requires close decoupling of 0.1-μF capacitor to GND_B
PVDD_C	26	P	Power supply input for half-bridge C requires close decoupling of 0.1-μF capacitor to GND_C
PVDD_D	21	P	Power supply input for half-bridge D requires close decoupling of 0.1-μF capacitor to GND_D
PWM_A	4	I	Input signal for half-bridge A
PWM_B	6	I	Input signal for half-bridge B
PWM_C	14	I	Input signal for half-bridge C
PWM_D	16	I	Input signal for half-bridge D
$\overline{\text{RESET\_AB}}$	5	I	Reset signal for half-bridge A and half-bridge B, active-low
$\overline{\text{RESET\_CD}}$	15	I	Reset signal for half-bridge C and half-bridge D, active-low
$\overline{\text{SD}}$	3	O	Shutdown signal, open drain, active-low
VDD	17	P	Power supply for digital voltage regulator requires 0.1-μF capacitor to GND.
VREG	10	P	Digital regulator supply filter pin requires 0.1-μF capacitor to AGND

(1) I = input, O = Output, P = Power

SYSTEM BLOCK DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

		CONDITIONS	MIN	NOM	MAX	UNIT
PVDD_x	Half-bridge supply	DC supply voltage	0	35	37	V
GVDD_x	Supply for logic regulators and gate-drive circuitry	DC supply voltage	10.8	12	13.2	V
VDD	Digital regulator input	DC supply voltage	10.8	12	13.2	V
R_L (BTL)	Load impedance	Output filter: L = 10 µH, C = 470 nF Output AD modulation, switching frequency > 350 kHz	3	4		Ω
R_L (SE)			2	3		
R_L (PBTL)			1.5	2		
L_{Output} (BTL)	Output-filter inductance	Minimum output inductance under short-circuit condition		10		µH
L_{Output} (SE)				10		
L_{Output} (PBTL)				10		
F_{PWM}	PWM frame rate		192	384	432	kHz
T_J	Junction temperature		0		125	°C

AUDIO SPECIFICATIONS (BTL)

PVDD_X = 35 V, GVDD = VDD = 12 V, BTL mode, R_L = 4 Ω, audio frequency = 1 kHz, AES17 filter, F_{PWM} = 384 kHz, case temperature = 75°C, unless otherwise noted. Audio performance is recorded as a chipset, using TAS5508 PWM processor with an effective modulation index limit of 96.1%. All performance is in accordance with recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TAS5152			UNIT
			MIN	TYP	MAX	
P_o	Power output per channel	R_L = 4 Ω,10% THD, clipped input signal		125		W
		R_L = 6 Ω,10% THD, clipped input signal		98		
		R_L = 8 Ω,10% THD, clipped input signal		76		
		R_L = 4 Ω, 0 dBFS, unclipped input signal		96		
		R_L = 6 Ω, 0 dBFS, unclipped input signal		72		
		R_L = 8 Ω, 0 dBFS, unclipped input signal		57		
THD+N	Total harmonic distortion + noise	0 dBFS		0.3		%
		1 W		0.1		
V_n	Output integrated noise	A-weighted		145		µV
SNR	Signal-to-noise ratio (1)	A-weighted		102		dB
DNR	Dynamic range	A-weighted, input level = –60 dBFS using TAS5508 modulator		102		dB
		A-weighted, input level = –60 dBFS using TAS5518 modulator		110		dB
P_{idle}	Power dissipation due to idle losses (IPVDDx)	P_O = 0 W, 2 channels switching (2)		2		W

(1) SNR is calculated relative to 0-dBFS input level.
(2) Actual system idle losses are affected by core losses of output inductors.

AUDIO SPECIFICATIONS (Single-Ended Output)

PVDD_X = 35 V, GVDD = VDD = 12 V, SE mode, R_L = 4 Ω, audio frequency = 1 kHz, AES17 filter, F_{PWM} = 384 kHz, case temperature = 75°C, unless otherwise noted. Audio performance is recorded as a chipset, using TAS5086 PWM processor with an effective modulation index limit of 96.1%. All performance is in accordance with recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TAS5152			UNIT
			MIN	TYP	MAX	
P_o	Power output per channel	R_L = 3 Ω,10% THD, clipped input signal		45		W
		R_L = 4 Ω,10% THD, clipped input signal		35		
		R_L = 3 Ω, 0 dBFS, unclipped input signal		35		
		R_L = 4 Ω, 0 dBFS, unclipped input signal		25		
THD+N	Total harmonic distortion + noise	0 dBFS		0.2		%
		1 W		0.1		
V_n	Output integrated noise	A-weighted		90		μV
SNR	Signal-to-noise ratio (1)	A-weighted		100		dB
DNR	Dynamic range	A-weighted, input level = –60 dBFS using TAS5508 modulator		100		dB
P_{idle}	Power dissipation due to idle losses (IPVDDx)	P_O = 0 W, 4 channels switching (2)		2		W

(1) SNR is calculated relative to 0-dBFS input level.
(2) Actual system idle losses are affected by core losses of output inductors.

AUDIO SPECIFICATIONS (PBTL)

PVDD_X = 35 V, GVDD = VDD = 12 V, PBTL mode, R_L = 3 Ω, audio frequency = 1 kHz, AES17 filter, F_{PWM} = 384 kHz, case temperature = 75°C, unless otherwise noted. Audio performance is recorded as a chipset, using TAS5508 PWM processor with an effective modulation index limit of 96.1%. All performance is in accordance with recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TAS5152			UNIT
			MIN	TYP	MAX	
P_o	Power output per channel	R_L = 3 Ω,10% THD, clipped input signal		192		W
		R_L = 2 Ω,10% THD, clipped input signal		240		
		R_L = 3 Ω, 0 dBFS, unclipped input signal		145		
		R_L = 2 Ω, 0 dBFS, unclipped input signal		190		
THD+N	Total harmonic distortion + noise	0 dBFS		0.2		%
		1 W		0.1		
V_n	Output integrated noise	A-weighted		160		μV
SNR	Signal-to-noise ratio (1)	A-weighted		102		dB
DNR	Dynamic range	A-weighted, input level = –60 dBFS using TAS5508 modulator		102		dB
		A-weighted, input level = –60 dBFS using TAS5518 modulator		110		dB
P_{idle}	Power dissipation due to idle losses (IPVDDx)	P_O = 0 W, 1 channel switching (2)		2		W

(1) SNR is calculated relative to 0-dBFS input level.
(2) Actual system idle losses are affected by core losses of output inductors.

ELECTRICAL CHARACTERISTICS

R_L= 4 Ω. F_{PWM} = 384 kHz, unless otherwise noted. All performance is in accordance with recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TAS5152			
			MIN	TYP	MAX	UNITS
Internal Voltage Regulator and Current Consumption						
VREG	Voltage regulator, only used as a reference node	VDD = 12 V	3	3.3	3.6	V
IVDD	VDD supply current	Operating, 50% duty cycle		7	17	mA
		Idle, reset mode		6	11	
IGVDD_x	Gate supply current per half-bridge	50% duty cycle		5	16	mA
		Reset mode		0.3	1	
IPVDD_x	Half-bridge idle current	50% duty cycle, without output filter or load		15	25	mA
		Reset mode, no switching		7	25	μA
Output Stage MOSFETs						
$R_{DSon,LS}$	Drain-to-source resistance, LS	T_J= 25°C, includes metallization resistance, GVDD = 12 V		140	155	mΩ
$R_{DSon,HS}$	Drain-to-source resistance, HS	T_J= 25°C, includes metallization resistance, GVDD = 12 V		140	155	mΩ

ELECTRICAL CHARACTERISTICS (continued)

R_L= 4 Ω. F_{PWM} = 384 kHz, unless otherwise noted. All performance is in accordance with recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TAS5152			
			MIN	TYP	MAX	UNITS
I/O Protection						
$V_{uvp,G}$	Undervoltage protection limit, GVDD_x			9.8		V
$V_{uvp,hyst}$(1)	Undervoltage protection hysteresis			250		mV
OTW(1)	Overtemperature warning		115	125	135	°C
OTW_{HYST}(1)	Temperature drop needed below OTW temp. for $\overline{OTW}$ to be inactive after the $\overline{OTW}$ event			25		°C
OTE(1)	Overtemperature error		145	155	165	°C
OTE-OTW differential(1)	OTE-OTW differential			30		°C
OTE_{HYST}(1)	Temperature drop needed below OTE temp. for $\overline{SD}$ to be released following an $\overline{OTE}$ event			25		°C
OLPC	Overload protection counter	F_{pwm} = 384 kHz		1.25		ms
I_{OC}	Overcurrent limit protection	Resistor-programmable, high end, R_{OCP} = 15 kΩ	8.5	10.8	11.8	A
I_{OCT}	Overcurrent response time			210		ns
R_{OCP}	OC programming resistor range	Resistor tolerance = 5%	15		69	kΩ
R_{PD}	Internal pulldown resistor at the output of each half-bridge	Connected when $\overline{RESET}$ is active to provide bootstrap capacitor charge. Not used in SE mode		2.5		kΩ
Static Digital Specifications						
V_{IH}	High-level input voltage	PWM_A, PWM_B, PWM_C, PWM_D, M1, M2, M3, RESET_AB, RESET_CD	2			V
V_{IL}	Low-level input voltage				0.8	V
Leakage	Input leakage current		–10		10	µA
OTW/SHUTDOWN (SD)						
R_{INT_PU}	Internal pullup resistance, $\overline{OTW}$ to VREG, $\overline{SD}$ to VREG		20	26	32	kΩ
V_{OH}	High-level output voltage	Internal pullup resistor	3	3.3	3.6	V
		External pullup of 4.7 kΩ to 5 V	4.5		5	
V_{OL}	Low-level output voltage	I_O = 4 mA		0.2	0.4	V
FANOUT	Device fanout $\overline{OTW}$, $\overline{SD}$	No external pullup		30		Devices

(1) Specified by design

TYPICAL CHARACTERISTICS, BTL CONFIGURATION

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

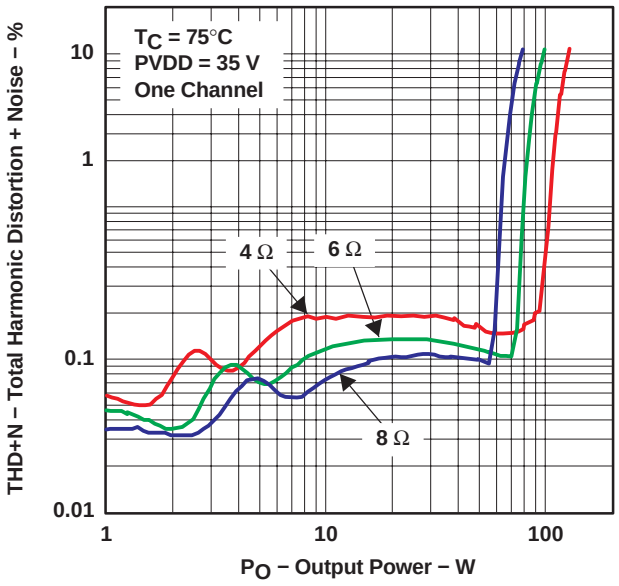


Figure 1

OUTPUT POWER
vs
SUPPLY VOLTAGE

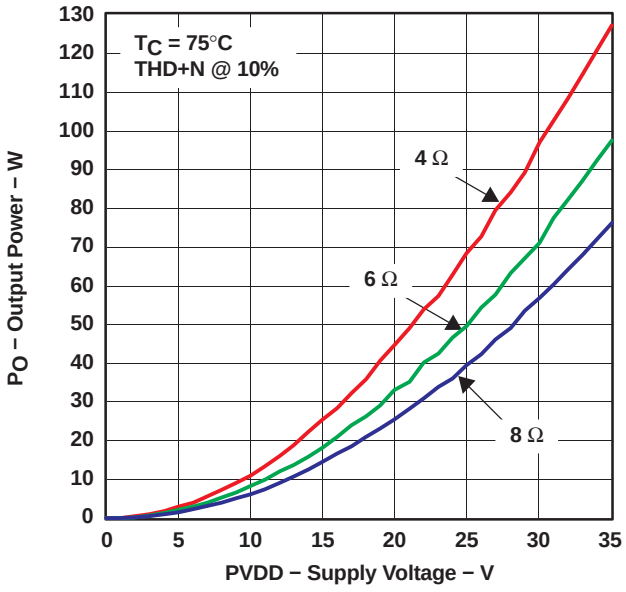


Figure 2

UNCLIPPED OUTPUT POWER
vs
SUPPLY VOLTAGE

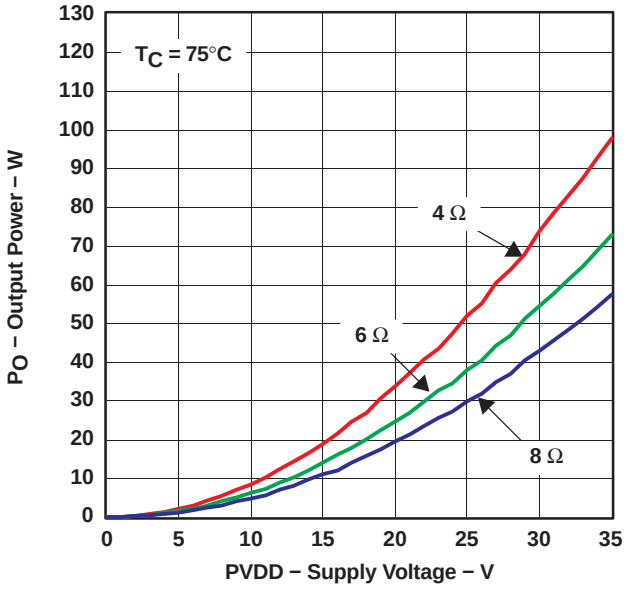


Figure 3

SYSTEM EFFICIENCY
vs
OUTPUT POWER

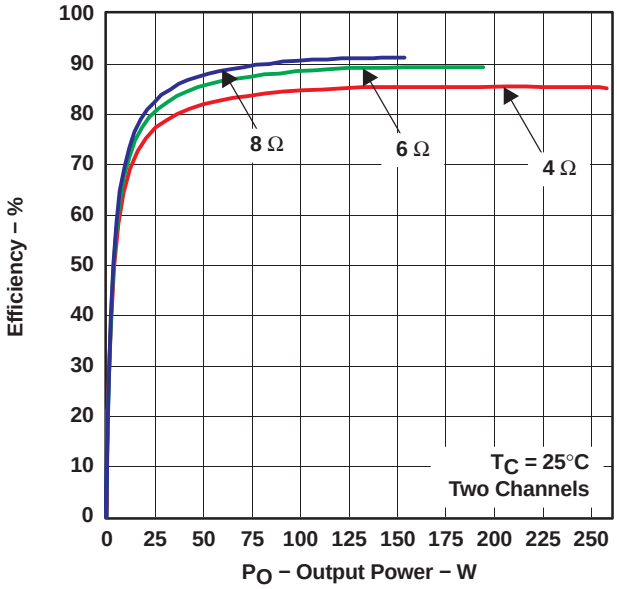


Figure 4

SYSTEM POWER LOSS
vs
OUTPUT POWER

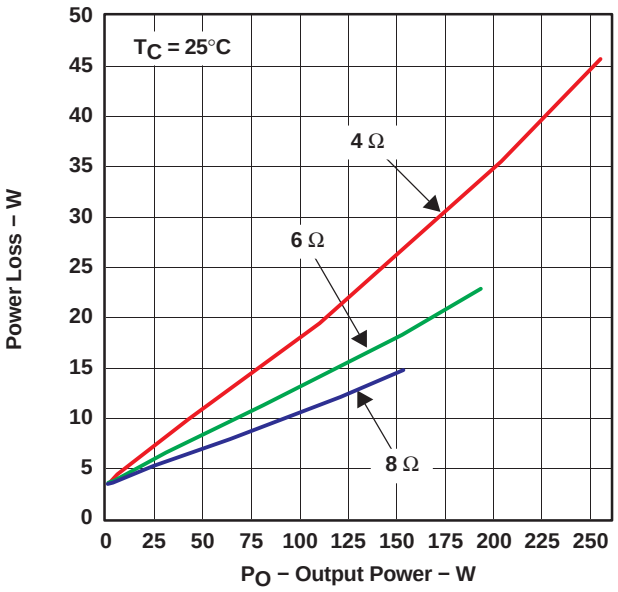


Figure 5

SYSTEM OUTPUT POWER
vs
CASE TEMPERATURE

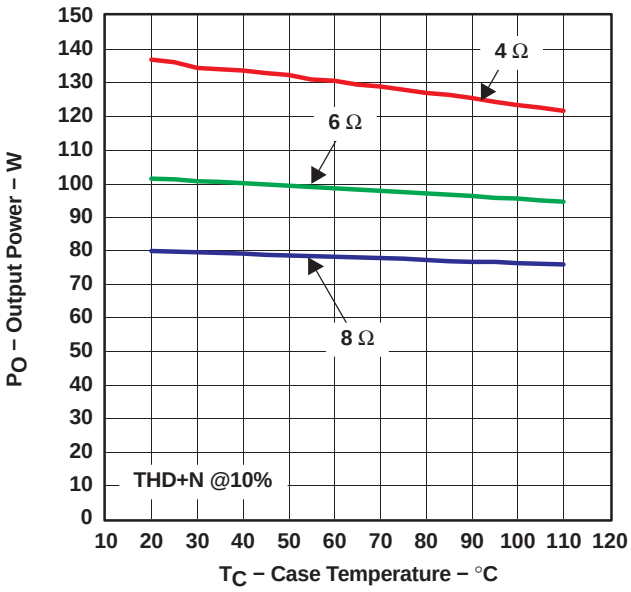


Figure 6

NOISE AMPLITUDE
vs
FREQUENCY

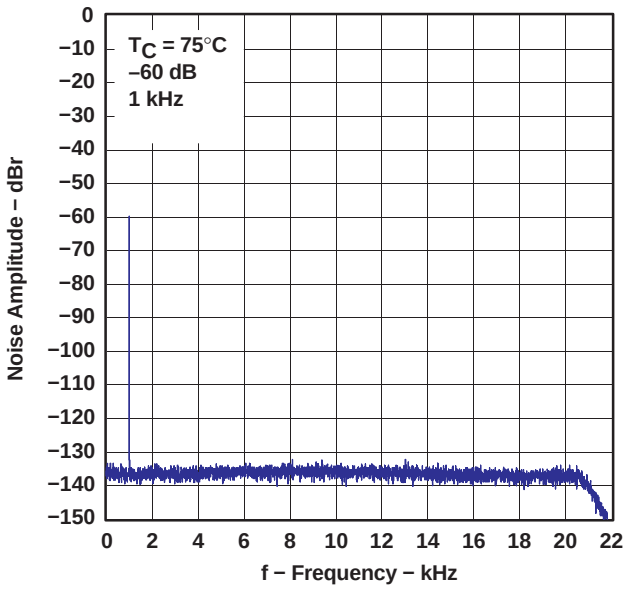


Figure 7

TYPICAL CHARACTERISTICS, SE CONFIGURATION

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

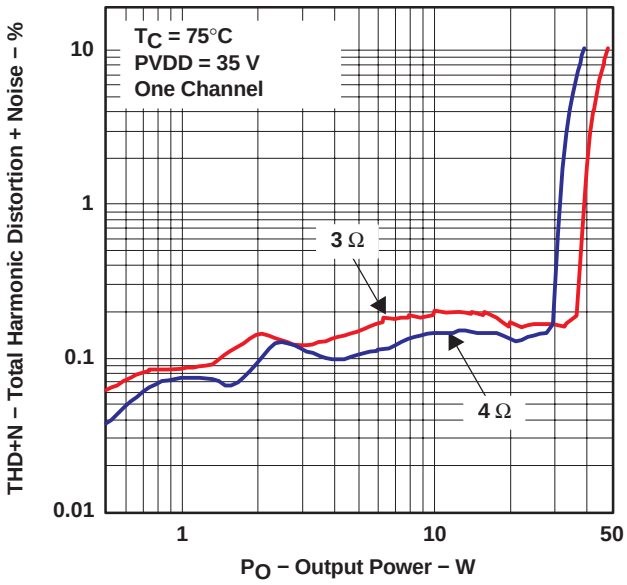


Figure 8

OUTPUT POWER
vs
SUPPLY VOLTAGE

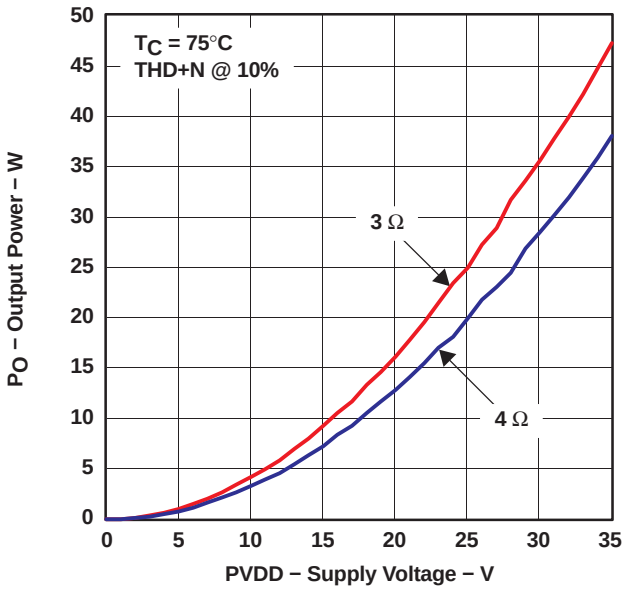


Figure 9

OUTPUT POWER
vs
CASE TEMPERATURE

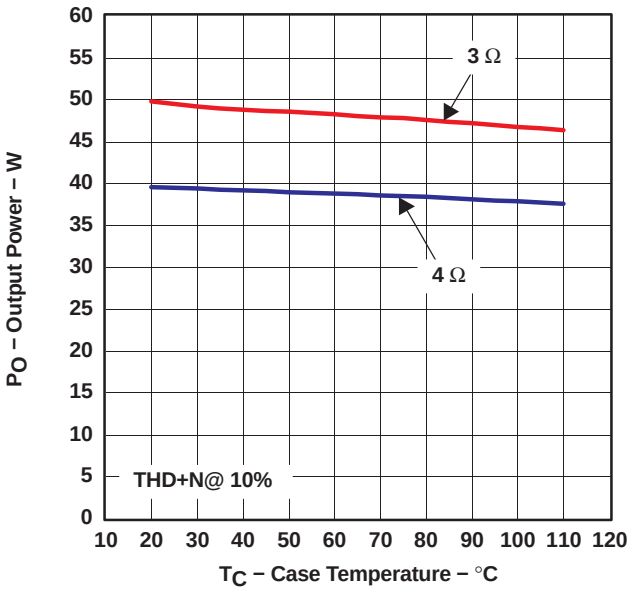


Figure 10

TYPICAL CHARACTERISTICS, PBTL CONFIGURATION

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

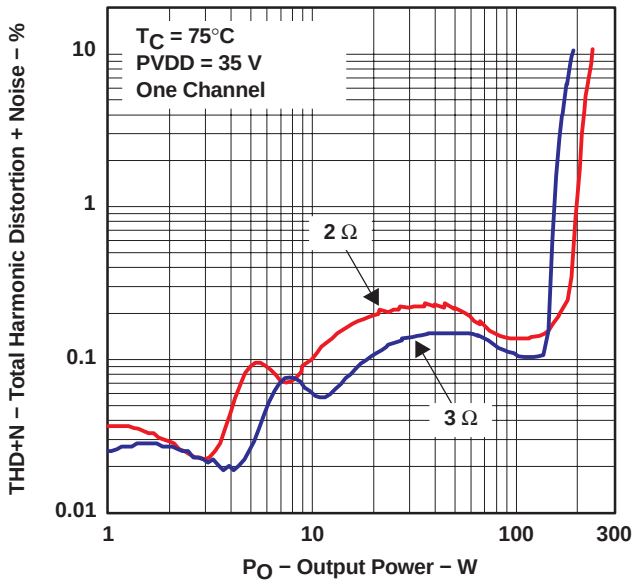


Figure 11

OUTPUT POWER
vs
SUPPLY VOLTAGE

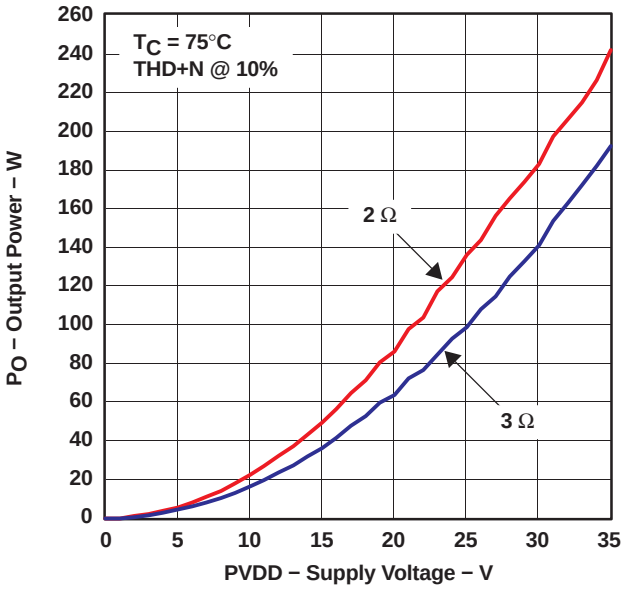


Figure 12

SYSTEM OUTPUT POWER
vs
CASE TEMPERATURE

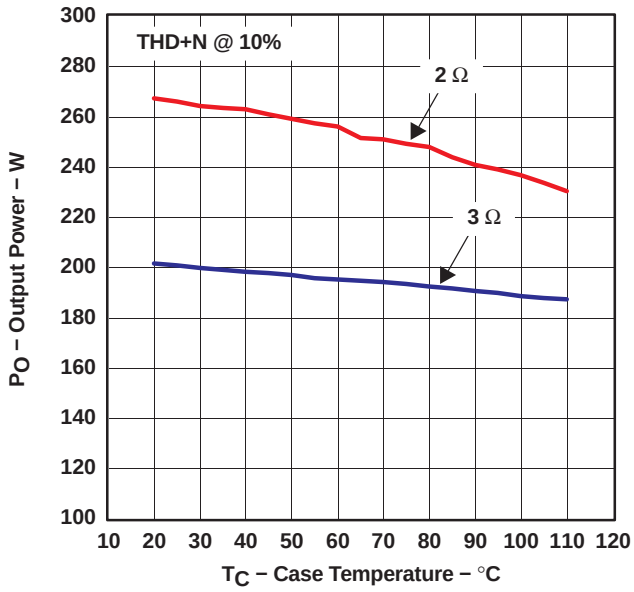


Figure 13

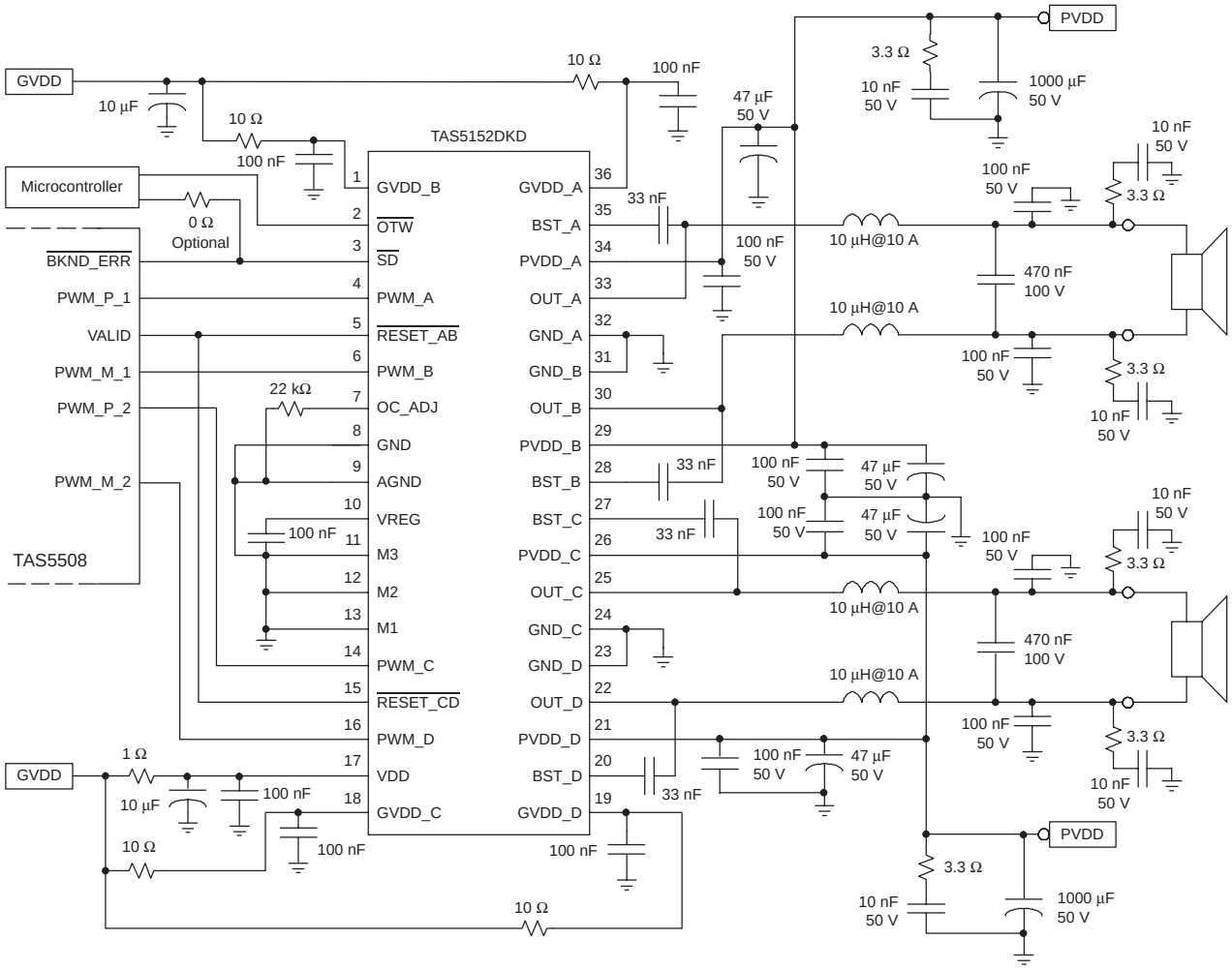


Figure 14. Typical Differential (2N) BTL Application With AD Modulation Filters

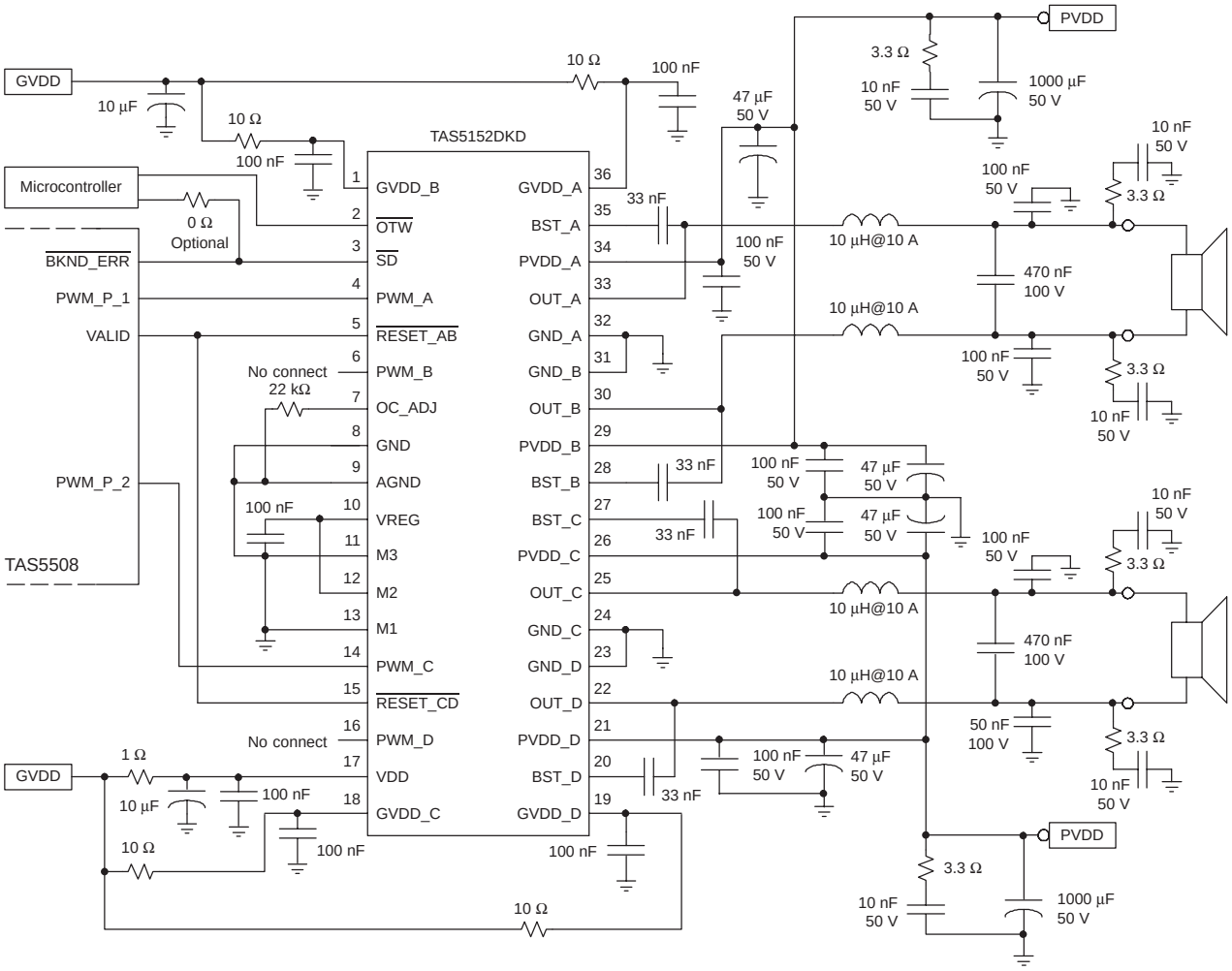


Figure 15. Typical Non-Differential (1N) BTL Application With AD Modulation Filters

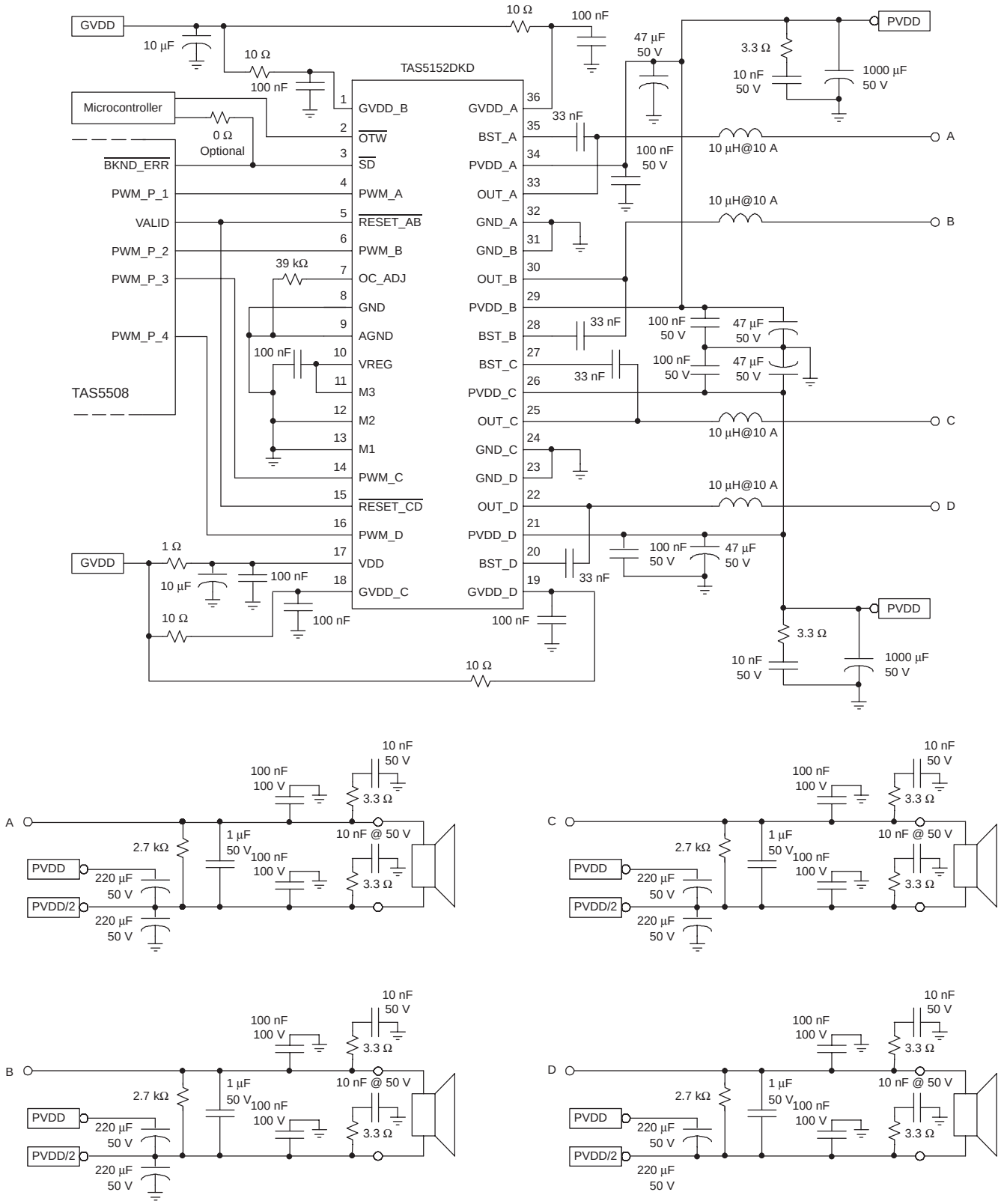


Figure 16. Typical SE Application

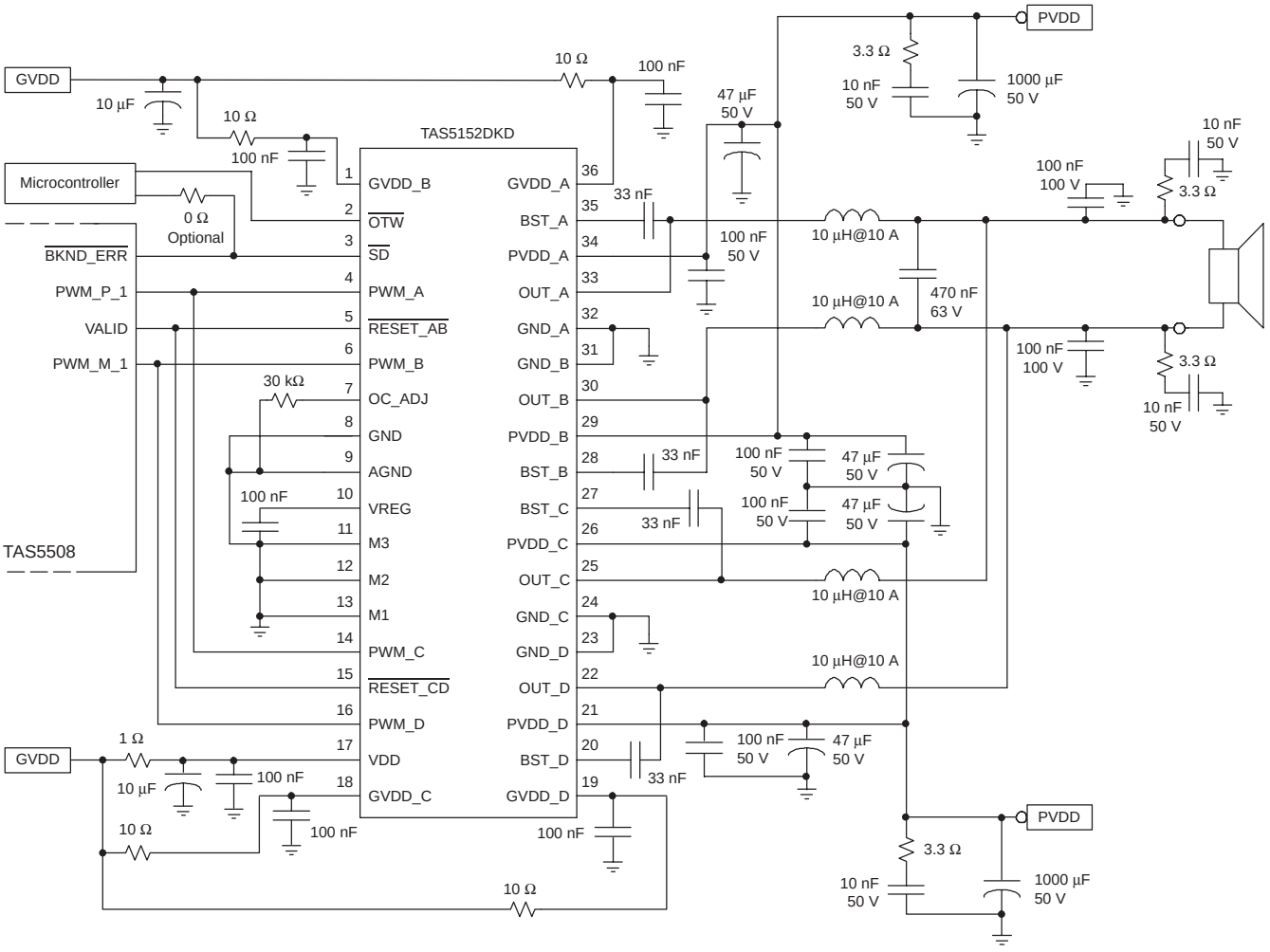


Figure 17. Typical Differential (2N) PBTL Application With AD Modulation Filters

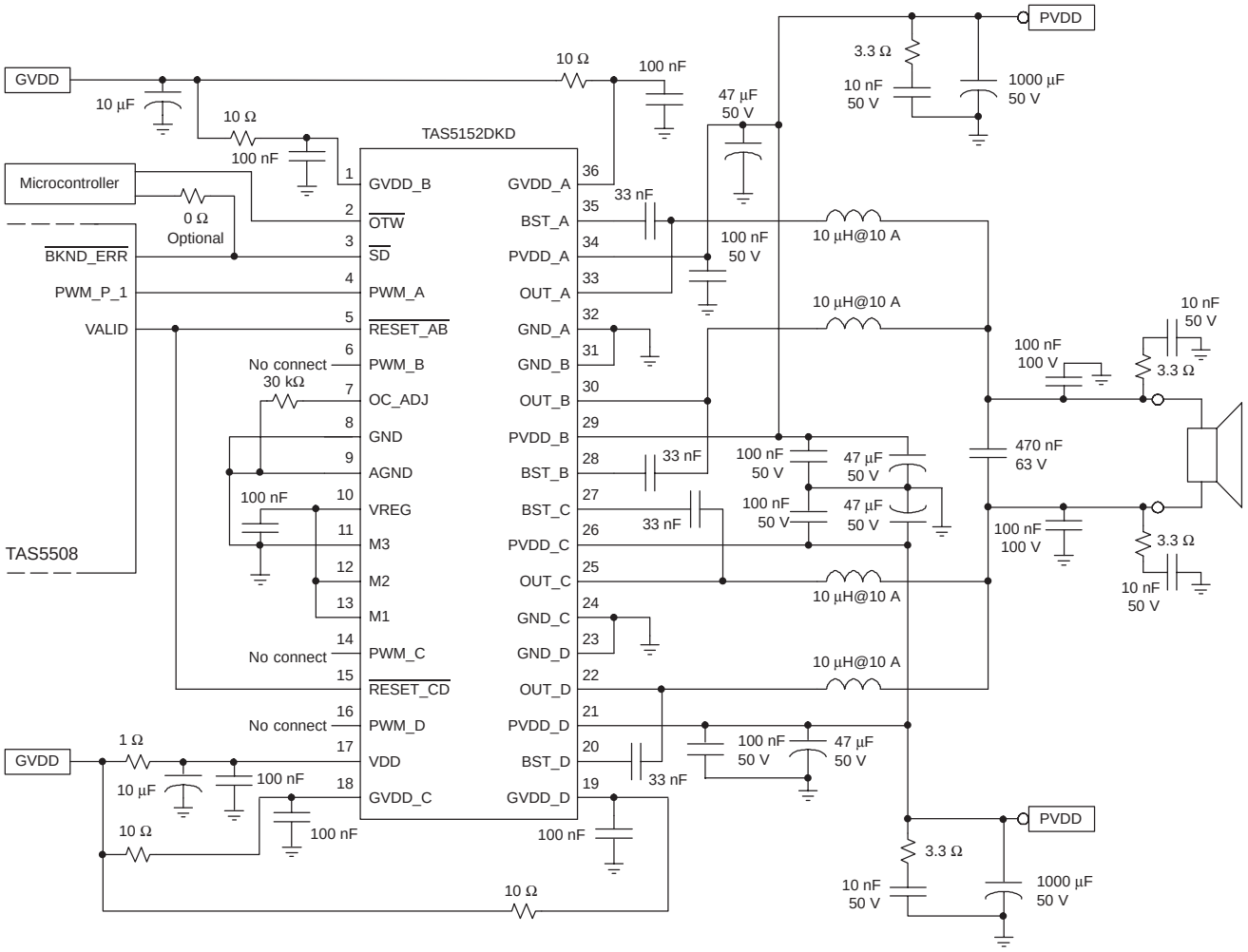


Figure 18. Typical Non-Differential (1N) PBTL Application

THEORY OF OPERATION

POWER SUPPLIES

To facilitate system design, the TAS5152 needs only a 12-V supply in addition to the (typically) 35-V power-stage supply. An internal voltage regulator provides suitable voltage levels for the digital and low-voltage analog circuitry. Additionally, all circuitry requiring a floating voltage supply, e.g., the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only a few external capacitors.

In order to provide outstanding electrical and acoustical characteristics, the PWM signal path including gate drive and output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate gate drive supply (GVDD_X), bootstrap pins (BST_X), and power-stage supply pins (PVDD_X). Furthermore, an additional pin (VDD) is provided as supply for all common circuits. Although supplied from the same 12-V source, it is highly recommended to separate GVDD_A, GVDD_B, GVDD_C, GVDD_D, and VDD on the printed-circuit board (PCB) by RC filters (see application diagram for details). These RC filters provide the recommended high-frequency isolation. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power supply pins and decoupling capacitors must be avoided. (See reference board documentation for additional information.)

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_X) to the power-stage output pin (OUT_X). When the power−stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD_X) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range 352 kHz to 384 kHz, it is recommended to use 33-nF ceramic capacitors, size 0603 or 0805, for the bootstrap supply. These 33-nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle. In an application running at a reduced switching frequency, generally 192 kHz, the bootstrap capacitor might need to be increased in value.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement and routing. As indicated, each half-bridge has independent power-stage supply pins (PVDD_X). For optimal electrical performance, EMI compliance, and system reliability it is important that each PVDD_X pin is decoupled with a 100-nF ceramic capacitor placed as close as possible to each supply pin. It is recommended to follow the PCB layout of the TAS5152 reference design. For additional information on recommended power supply and required components, see the application diagrams given previously in this data sheet.

The 12-V supply should be from a low-noise, low-output-impedance voltage regulator. Likewise, the 35-V power-stage supply is assumed to have low output impedance and low noise. The power-supply sequence is not critical as facilitated by the internal power-on-reset circuit. Moreover, the TAS5152 is fully protected against erroneous power-stage turnon due to parasitic gate charging. Thus, voltage-supply ramp rates (dV/dt) are non-critical within the specified range (see the *Recommended Operating Conditions* section of this data sheet).

SYSTEM POWER-UP/POWER-DOWN SEQUENCE

Powering Up

The TAS5152 does not require a power-up sequence. The outputs of the H−bridges remain in a high-impedance state until the gate-drive supply voltage (GVDD_X) and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the *Electrical Characteristics* section of this data sheet). Although not specifically required, it is recommended to hold $\overline{\text{RESET\_AB}}$ and $\overline{\text{RESET\_CD}}$ in a low state while powering up the device. This allows an internal circuit to charge the external bootstrap capacitors by enabling a weak pulldown of the half-bridge output.

When the TAS5152 is being used with TI PWM modulators such as the TAS5508, no special attention to the state of $\overline{\text{RESET\_AB}}$ and $\overline{\text{RESET\_CD}}$ is required, provided that the chipset is configured as recommended.

Powering Down

The TAS5152 does not require a power-down sequence. The device remains fully operational as long as the gate-drive supply (GVDD_X) voltage and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the *Electrical Characteristics* section of this data sheet). Although not specifically required, it is a good practice to hold $\overline{\text{RESET\_AB}}$ and $\overline{\text{RESET\_CD}}$ low during power down, thus preventing audible artifacts including pops or clicks.

When the TAS5152 is being used with TI PWM modulators such as the TAS5508, no special attention to the state of $\overline{\text{RESET\_AB}}$ and $\overline{\text{RESET\_CD}}$ is required, provided that the chipset is configured as recommended.

ERROR REPORTING

The $\overline{SD}$ and $\overline{OTW}$ pins are both active-low, open-drain outputs. Their function is for protection-mode signaling to a PWM controller or other system-control device.

Any fault resulting in device shutdown is signaled by the $\overline{SD}$ pin going low. Likewise, $\overline{OTW}$ goes low when the device junction temperature exceeds 125°C (see the following table).

$\overline{SD}$	$\overline{OTW}$	DESCRIPTION
0	0	Overtemperature (OTE) or overload (OLP) or undervoltage (UVP)
0	1	Overload (OLP) or undervoltage (UVP)
1	0	Junction temperature higher than 125°C (overtemperature warning)
1	1	Junction temperature lower than 125°C and no OLP or UVP faults (normal operation)

Note that asserting either $\overline{RESET\_AB}$ or $\overline{RESET\_CD}$ low forces the $\overline{SD}$ signal high, independent of faults being present. TI recommends to monitoring the $\overline{OTW}$ signal using the system microcontroller and responding to an overtemperature warning signal by, e.g., turning down the volume to prevent further heating of the device resulting in device shutdown (OTE).

To reduce external component count, an internal pullup resistor to 3.3V is provided on both $\overline{SD}$ and $\overline{OTW}$ outputs. Level compliance for 5-V logic can be obtained by adding external pullup resistors to 5 V (see the *Electrical Characteristics* section of this data sheet for further specifications).

DEVICE PROTECTION SYSTEM

TAS5152 contains advanced protection circuitry carefully designed to facilitate system integration and ease of use, as well as to safeguard the device from permanent failure due to a wide range of fault conditions such as short circuits, overload, overtemperature, and undervoltage. The TAS5152 responds to a fault by immediately setting the power stage in a high-impedance state (Hi-Z) and asserting the $\overline{SD}$ pin low. In situations other than overload, the device automatically recovers when the fault condition has been removed, i.e., the junction temperature has dropped or the voltage supply has increased. For highest possible reliability, recovering from an overload fault requires external reset of the device (see the *Device Reset* section of this data sheet) no sooner than 1 second after the shutdown.

Use of TAS5152 in High-Modulation-Index Capable Systems

This device requires at least 50 ns of low time on the output per 384-kHz PWM frame rate in order to keep the bootstrap capacitors charged. As an example, if the modulation index is set to 99.2% in the TAS5508, this setting allows PWM pulse durations down to 20 ns. This signal, which does not meet the 50-ns requirement, is sent to the PWM_x pin and this low-state pulse time does not allow the bootstrap capacitor to stay charged. In this situation, the low voltage across the bootstrap capacitor can cause a failure of the high-side MOSFET transistor, especially when driving a low-impedance load. The TAS5152 device requires limiting the TAS5508 modulation index to 96.1% to keep the bootstrap capacitor charged under all signals and loads.

Therefore, TI strongly recommends using a TI PWM processor, such as TAS5508 or TAS5086, with the modulation index set at 96.1% to interface with TAS5152.

Overcurrent (OC) Protection With Current Limiting and Overload Detection

The device has independent, fast-reacting current detectors with programmable trip threshold (OC threshold) on all high-side and low-side power-stage FETs. See the following table for OC-adjust resistor values. The detector outputs are closely monitored by two protection systems. The first protection system controls the power stage in order to prevent the output current from further increasing, i.e., it performs a current-limiting function rather than prematurely shutting down during combinations of high-level music transients and extreme speaker load impedance drops. If the high-current situation persists, i.e., the power stage is being overloaded, a second protection system triggers a latching shutdown, resulting in the power stage being set in the high-impedance (Hi-Z) state. Current limiting and overload protection are independent for the half-bridges A and B and, respectively, C and D. That is, if the bridge-tied load between half-bridges A and B causes an overload fault, only half-bridges A and B are shut down.

- For the lowest-cost bill of materials in terms of component selection, the OC threshold measure should be limited, considering the power output requirement and minimum load impedance. Higher-impedance loads require a lower OC threshold.
- The demodulation-filter inductor must retain at least 3 µH of inductance at twice the OC threshold setting.

Unfortunately, most inductors have decreasing inductance with increasing temperature and increasing current (saturation). To some degree, an increase in temperature naturally occurs when operating at high output currents, due to core losses and the DC resistance of the inductor's copper winding. A thorough analysis of inductor saturation and thermal properties is strongly recommended.

Setting the OC threshold too low might cause issues such as lack of enough output power and/or unexpected shutdowns due to too-sensitive overload detection.

In general, it is recommended to follow closely the external component selection and PCB layout as given in the *Application* section.

For added flexibility, the OC threshold is programmable within a limited range using a single external resistor connected between the OC_ADJ pin and AGND. (See the *Electrical Characteristics* section of this data sheet for information on the correlation between programming-resistor value and the OC threshold.) It should be noted that a properly functioning overcurrent detector assumes the presence of a properly designed demodulation filter at the power-stage output. Short-circuit protection is not provided directly at the output pins of the power stage but only on the speaker terminals (after the demodulation filter). It is required to follow certain guidelines when selecting the OC threshold and an appropriate demodulation inductor:

OC-Adjust Resistor Values (kΩ)	Max. Current Before OC Occurs (A)
15	10.8
22	9.4
27	8.6
39	6.4
47	6
69	4.7

Overtemperature Protection

The TAS5152 has a two-level temperature-protection system that asserts an active-low warning signal ($\overline{\text{OTW}}$) when the device junction temperature exceeds 125°C (nominal) and, if the device junction temperature exceeds 155°C (nominal), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance state (Hi-Z) and $\overline{\text{SD}}$ being asserted low. OTE is latched in this case. To clear the OTE latch, both $\overline{\text{RESET\_AB}}$ and $\overline{\text{RESET\_CD}}$ must be asserted. Thereafter, the device resumes normal operation.

Undervoltage Protection (UVP) and Power-On Reset (POR)

The UVP and POR circuits of the TAS5152 fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit resets the overload circuit (OLP) and ensures that all circuits are fully operational when the GVDD_X and VDD supply voltages reach 9.8 V (typical). Although GVDD_X and VDD are independently monitored, a supply voltage drop below the UVP threshold on any VDD or GVDD_X pin results in all half-bridge outputs immediately being set in the high-impedance state (Hi-Z) and $\overline{\text{SD}}$ being asserted low. The device automatically resumes operation when all supply voltages have increased above the UVP threshold.

DEVICE RESET

Two reset pins are provided for independent control of half-bridges A/B and C/D. When $\overline{\text{RESET\_AB}}$ is asserted low, all four power-stage FETs in half-bridges A and B are forced into a high-impedance state (Hi-Z). Likewise, asserting $\overline{\text{RESET\_CD}}$ low forces all four power-stage FETs in half-bridges C and D into a high-impedance state. Thus, both reset pins are well suited for hard-muting the power stage if needed.

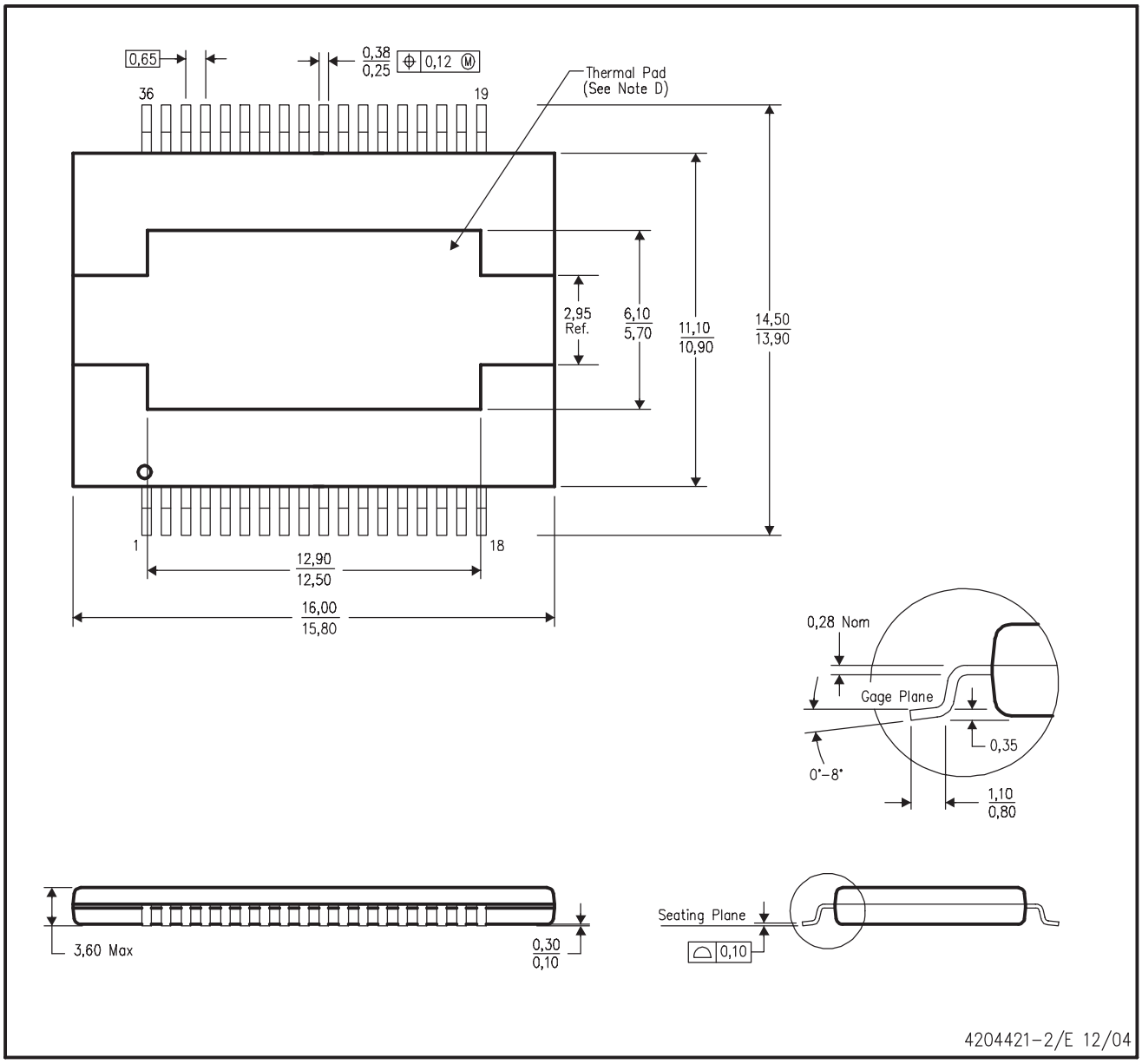
In BTL modes, to accommodate bootstrap charging prior to switching start, asserting the reset inputs low enables weak pulldown of the half-bridge outputs. In the SE mode, the weak pulldowns are not enabled, and it is therefore recommended to ensure bootstrap capacitor charging by providing a low pulse on the PWM inputs when reset is asserted high.

Asserting either reset input low removes any fault information to be signalled on the $\overline{\text{SD}}$ output, i.e., $\overline{\text{SD}}$ is forced high.

A rising-edge transition on either reset input allows the device to resume operation after an overload fault.

MECHANICAL DATA

DKD (R–PDSO–G36) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance is optimized for conductive cooling with attachment to an external heat sink. See the product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–166 Variation AE.

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