STN4NF20L

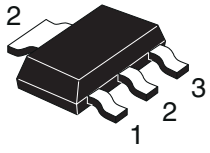
N-channel 200 V, 1.1 Ω, 1 A SOT-223 low gate charge STripFET™ II Power MOSFET

Preliminary data

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STN4NF20L	200 V	< 1.5 Ω	1 A

- 100% avalanche tested
- Low gate charge
- Exceptional dv/dt capability



SOT-223

Application

- Switching applications

Description

This Power MOSFET series realized with STMicroelectronics unique STripFET™ process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high efficiency isolated DC-DC converters.

Figure 1. Internal schematic diagram

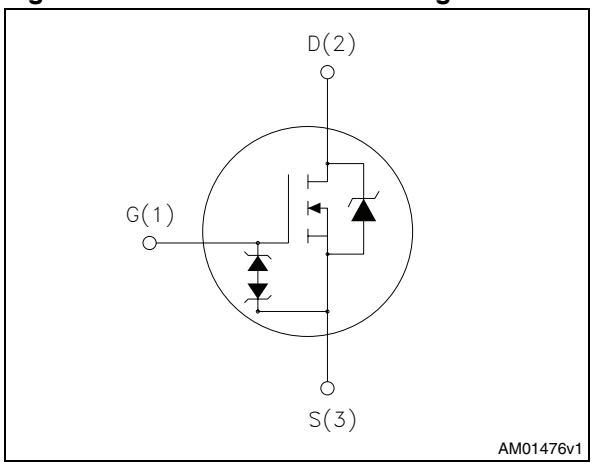


Table 1. Device summary

Order code	Marking	Package	Packaging
STN4NF20L	4NF20L	SOT-223	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current continuous T_C = 25 °C	1	A
I_D	Drain current continuous T_C = 100 °C	0.6	A
I_{DM} (1)	Drain current pulsed	4	A
P_{TOT}	Total dissipation at T_C = 25 °C	TBD	W
dv/dt (2)	Peak diode recovery voltage slope	TBD	V/ns
T_j T_{stg}	Operating junction temperature Storage temperature	- 55 to 150	°C

1. Pulse width limited by safe operating area.
2. Isd ≤ TBD A, di/dt ≤ TBD A/µs, V_{DD} ≤ 80% $V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction to case	62.50	°C/W

Table 4. Thermal data

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetetive or not repetetive(1)	TBD	A
E_{AS}	Single pulse avalanche energy (2)	TBD	mJ

1. Pulse width limited by T_{JMAX}.
2. Starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V.

2 Electrical characteristics

(Tcase = 25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	200			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, T_C=125 °C			1 50	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V, V_{DS}=0			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{GS} = V_{DS}, I_D = 250 µA	1	2	3	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 0.5 A		1.1	1.5	Ω
		V_{GS} = 5 V, I_D = 0.5 A		1.13	1.55	

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	150 30 4	-	pF pF pF
$C_{oss(tr)}$(1)	Equivalent output capacitance energy related	V_{DS}=0 to 160 V V_{GS}=0	-	TBD	-	pF
$C_{oss(er)}$(2)	Equivalent output capacitance time related	V_{DS}=0 to 160 V V_{GS}=0	-	TBD	-	pF
R_g	Instrinsic gate resistance	f=1 MHz open drain	-	TBD	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 160 V, I_D = 1 A, V_{GS} = 10 V (see *Figure 3*)	-	3 TBD TBD	-	nC nC nC

1. Is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. Is defined as a constant equivalent capacitance giving the same storage energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(v)}$ t_r t_f $t_{c(off)}$	Voltage delay time Voltage rise time Current fall time Crossing time	V_{DD} = 100 V, I_D = TBD, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 2*)	-	TBD TBD TBD TBD	-	ns ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		1 4	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 1 A, V_{GS} = 0	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 1 A, di/dt = 100 A/µs V_{DD} = 20 V (see *Figure 4*)	-	TBD TBD TBD		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 1 A, di/dt = 100 A/µs V_{DD} = 20 V, T_j = 150 °C (see *Figure 4*)	-	TBD TBD TBD		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

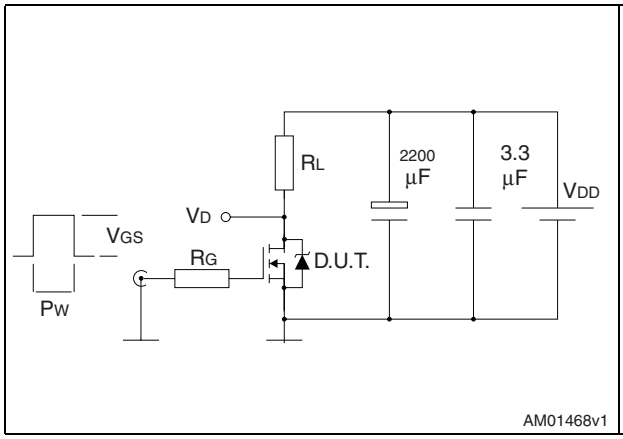


Figure 3. Gate charge test circuit

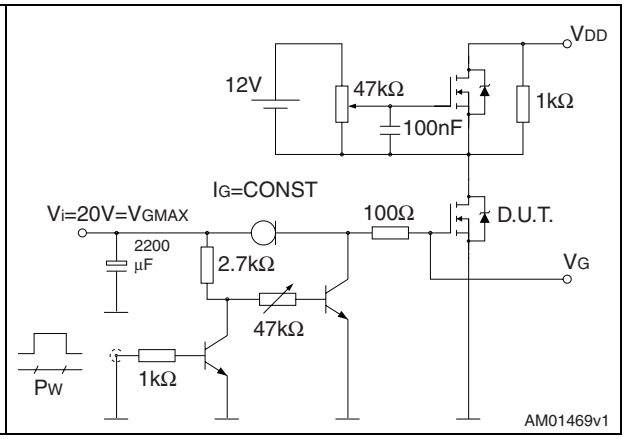


Figure 4. Test circuit for inductive load switching and diode recovery times

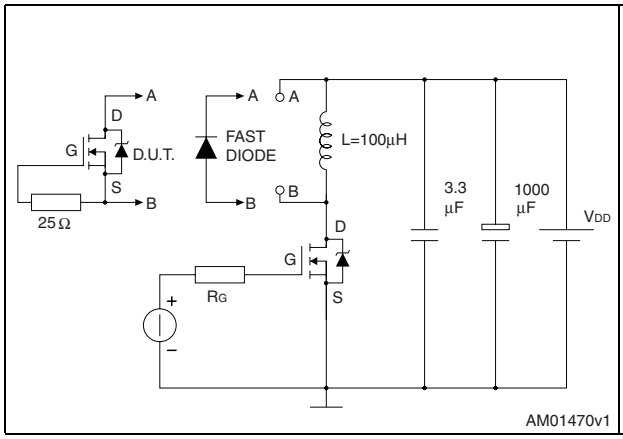


Figure 5. Unclamped inductive load test circuit

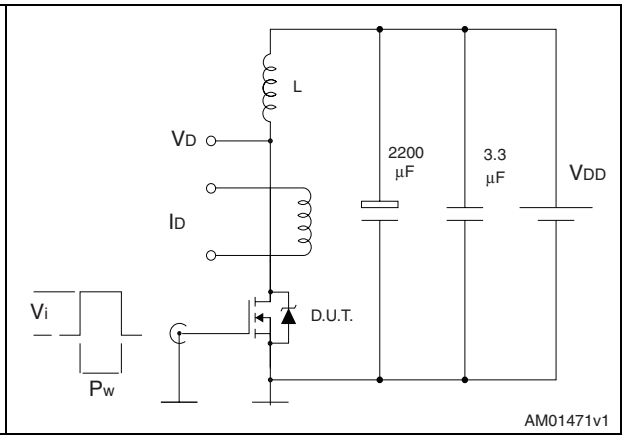


Figure 6. Unclamped inductive waveform

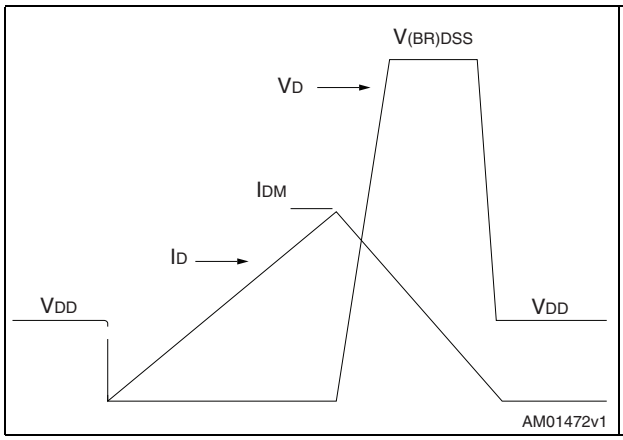
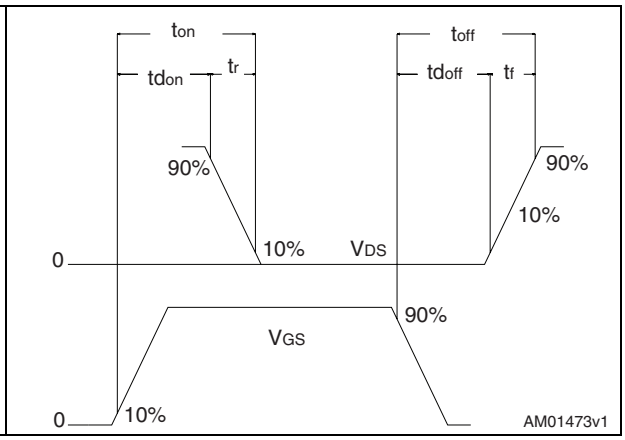


Figure 7. Switching time waveform

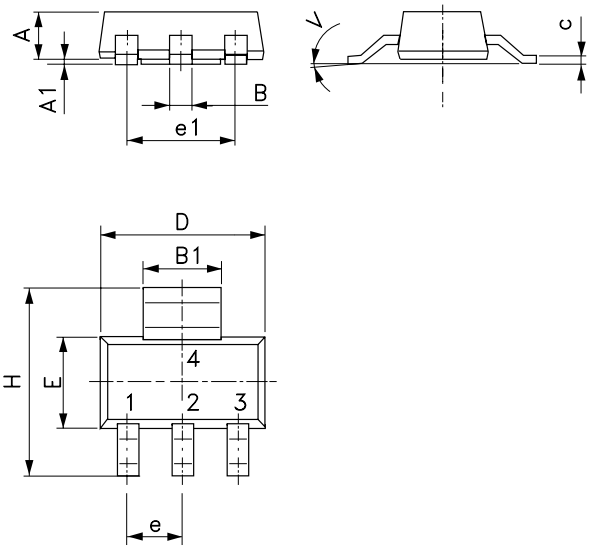


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

SOT-223 mechanical data

DIM.	mm.		
	min.	typ	max.
A			1.80
A1	0.02		0.1
B	0.60	0.70	0.85
B1	2.90	3.00	3.15
c	0.24	0.26	0.35
D	6.30	6.50	6.70
e		2.30	
e1		4.60	
E	3.30	3.50	3.70
H	6.70	7.00	7.30
V			10 °



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
29-Apr-2010	1	First release.

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