



STP25NM60N - STF25NM60N STB25NM60N/-1 - STW25NM60N

N-CHANNEL 650 @Tjmax-0.140Ω-20A TO-220/FP/D²/I²PAK/TO-247
SECOND GENERATION MDmesh™ MOSFET

PRODUCT PREVIEW

Table 1: General Features

TYPE	V _{DSS} (@T _{jmax})	R _{DS(on)}	I _D
STB25NM60N-1	650 V	< 0.170 Ω	20 A
STF25NM60N	650 V	< 0.170 Ω	20(*) A
STP25NM60N	650 V	< 0.170 Ω	20 A
STW25NM60N	650 V	< 0.170 Ω	20 A
STB25NM60NT4	650 V	< 0.170 Ω	20 A

- WORLD'S LOWEST ON RESISTANCE
- TYPICAL R_{DS(on)} = 0.140 Ω
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- 100% AVALANCHE TESTED
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE

DESCRIPTION

The **STP25NM60N** is realized with the second generation of MDmesh Technology. This revolutionary MOSFET associates a new vertical structure to the Company's strip layout to yield the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters

APPLICATIONS

The MDmesh™ II family is very suitable for increase the power density of high voltage converters allowing system miniaturization and higher efficiencies.

Figure 1: Package

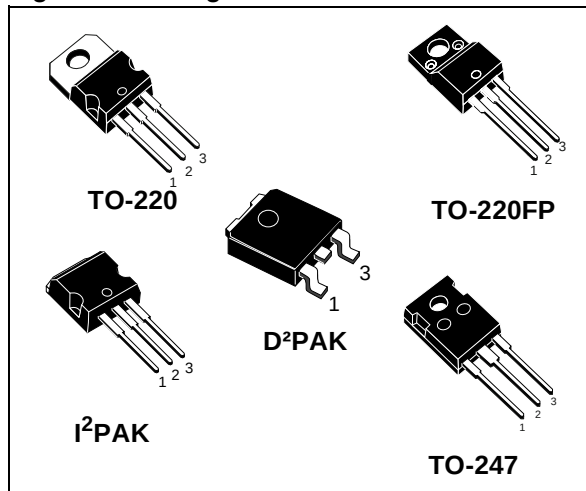


Figure 2: Internal Schematic Diagram

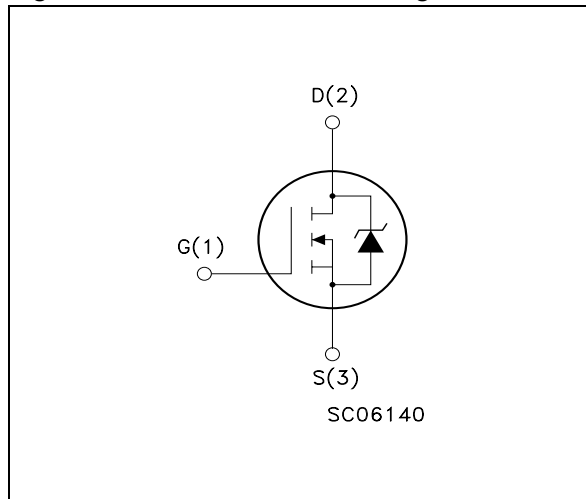


Table 2: Order Code

SALES TYPE	MARKING	PACKAGE	PACKAGING
STB25NM60N-1	B25NM60N	I ² PAK	TUBE
STF25NM60N	F25NM60N	TO-220FP	TUBE
STP25NM60N	P25NM60N	TO-220	TUBE
STW25NM60N	W25NM60N	TO-247	TUBE
STB25NM60NT4	B25NM60N	D ² PAK	TAPE & REEL

Rev. 1

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value		Unit
		TO-220/I ² PAK TO-247/D ² PAK	TO-220FP	
V _{GS}	Gate- source Voltage	± 30		V
I _D	Drain Current (continuous) at T _C = 25°C	20	20 (*)	A
I _D	Drain Current (continuous) at T _C = 100°C	12.8	12.8 (*)	A
I _{DM} (1)	Drain Current (pulsed)	80	80 (*)	A
P _{TOT}	Total Dissipation at T _C = 25°C	160	40	W
	Derating Factor	1.28	0.32	W/°C
dv/dt (2)	Peak Diode Recovery voltage slope	TBD		V/ns
T _{stg}	Storage Temperature	– 55 to 150		°C
T _j	Max. Operating Junction Temperature	150		°C

(*) Limited only by maximum temperature allowed

(1) Pulse width limited by safe operating area

(2) I_{SD} ≤ 20 A, di/dt ≤ 400 A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}.

Table 4: Thermal Data

		TO-220/I ² PAK TO-247/D ² PAK	TO-220FP	
R _{thj-case}	Thermal Resistance Junction-case Max	0.78	3.1	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient Max	62.5		°C/W
T _I	Maximum Lead Temperature For Soldering Purpose	300		°C

Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	TBD	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	TBD	mJ

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25°C UNLESS OTHERWISE SPECIFIED)

Table 6: On /Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 1 mA, V _{GS} = 0	600			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125°C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 30 V			± 100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	2	3	4	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V, I _D = 10 A		0.140	0.170	Ω

ELECTRICAL CHARACTERISTICS (CONTINUED)**Table 7: Dynamic**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	$V_{DS} = 15V$, $I_D = 10A$		17		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V$, $f = 1MHz$, $V_{GS} = 0$		TBD TBD TBD		pF pF pF
$C_{oss\ eq}$ (3)	Equivalent Output Capacitance	$V_{GS} = 0V$, $V_{DS} = 0$ to $480V$		TBD		pF
R_G	Gate Input Resistance	$f = 1MHz$ Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		2		Ω
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-off-Delay Time Fall Time	$V_{DD} = 480V$, $I_D = 12.5A$, $R_G = 4.7\Omega$, $V_{GS} = 10V$ (see Figure 4)		TBD TBD TBD TBD		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 480V$, $I_D = 25A$, $V_{GS} = 10V$ (see Figure 7)		TBD TBD TBD		nC nC nC

Table 8: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				20 80	A A
V_{SD} (1)	Forward On Voltage	$I_{SD} = 20A$, $V_{GS} = 0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 25A$, $di/dt = 100A/\mu s$ $V_{DD} = 100V$ (see Figure 5)		TBD TBD TBD		ns μC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 25A$, $di/dt = 100A/\mu s$ $V_{DD} = 100V$, $T_j = 150^\circ C$ (see Figure 5)		TBD TBD TBD		ns μC A

(1) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

(2) Pulse width limited by safe operating area.

(3) $C_{oss\ eq}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Figure 3: Unclamped Inductive Load Test Circuit

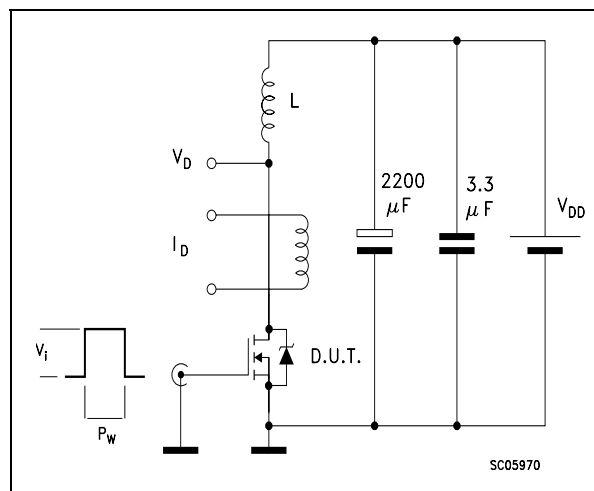


Figure 4: Switching Times Test Circuit For Resistive Load

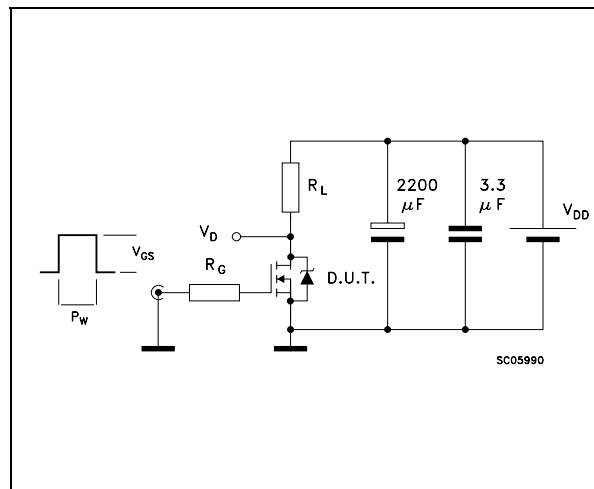


Figure 5: Test Circuit For Inductive Load Switching and Diode Recovery Times

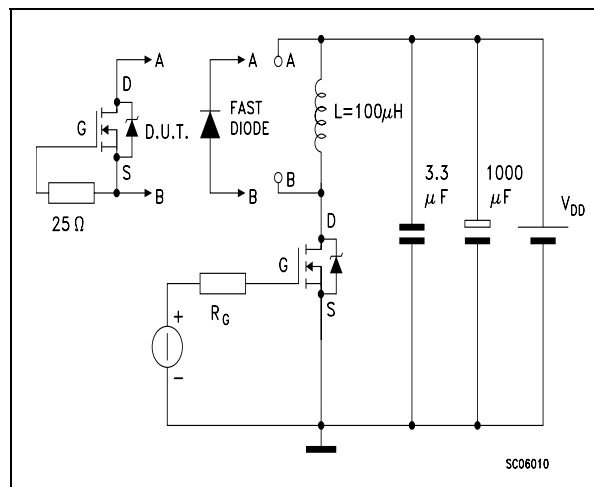


Figure 6: Unclamped Inductive Wafeform

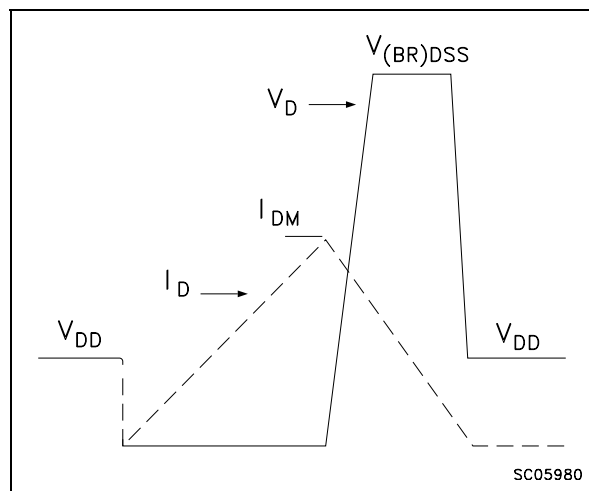
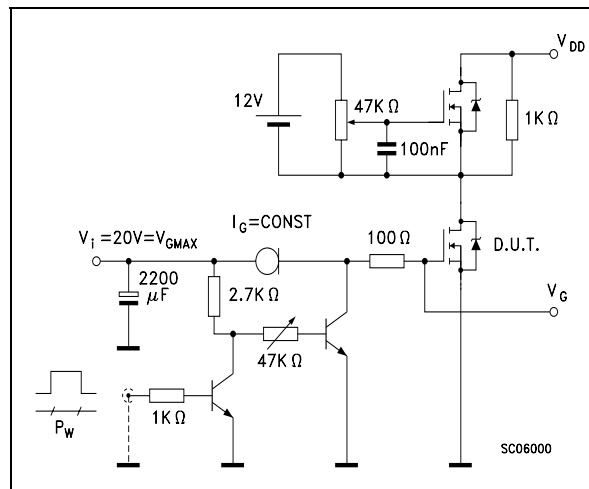
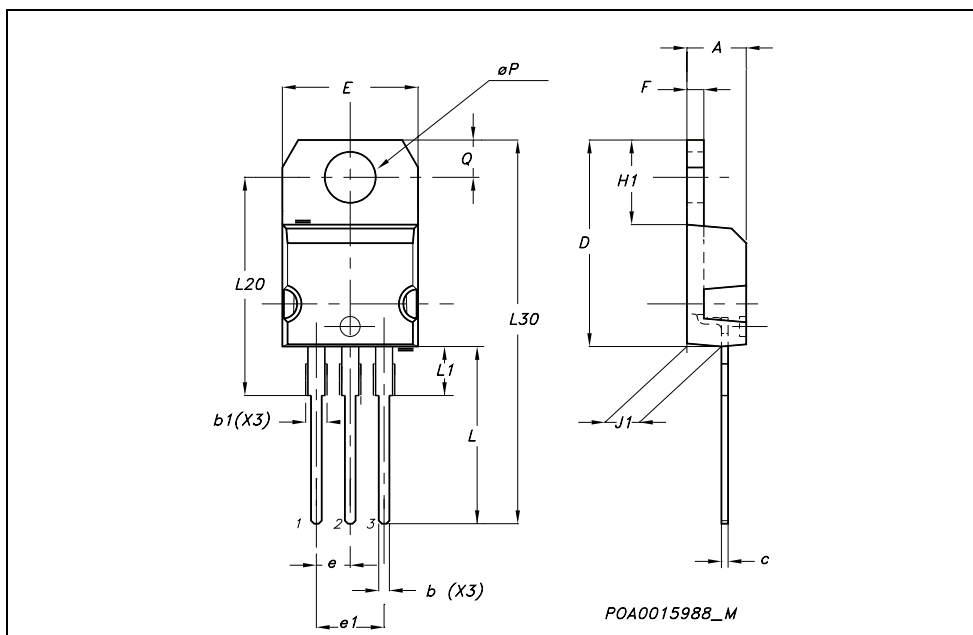


Figure 7: Gate Charge Test Circuit



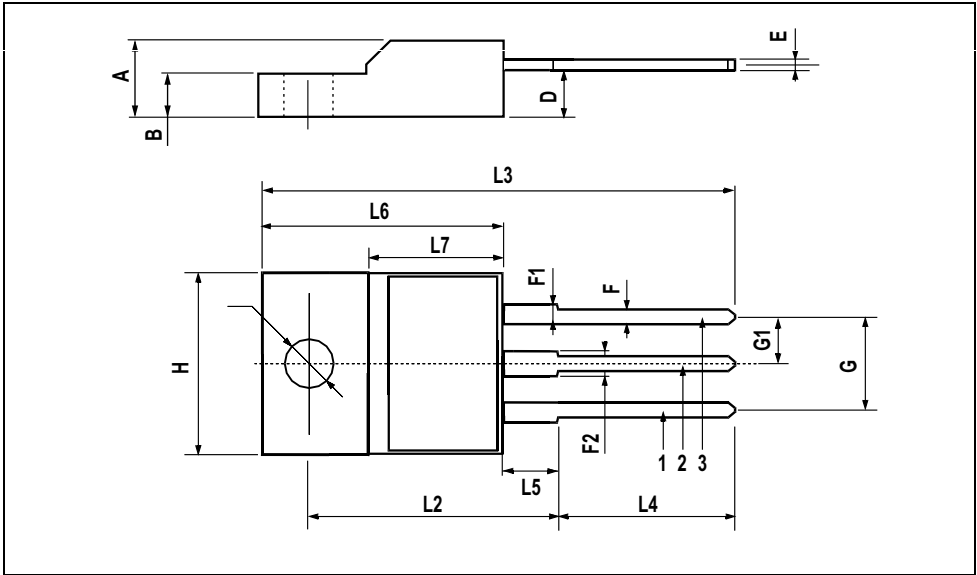
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



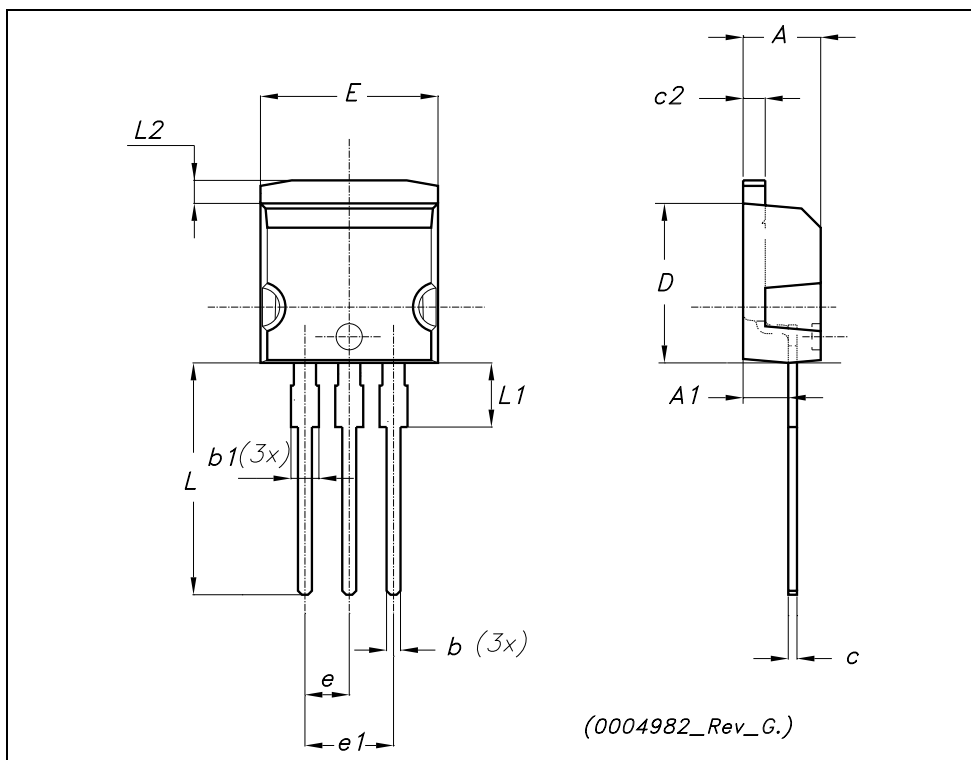
TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



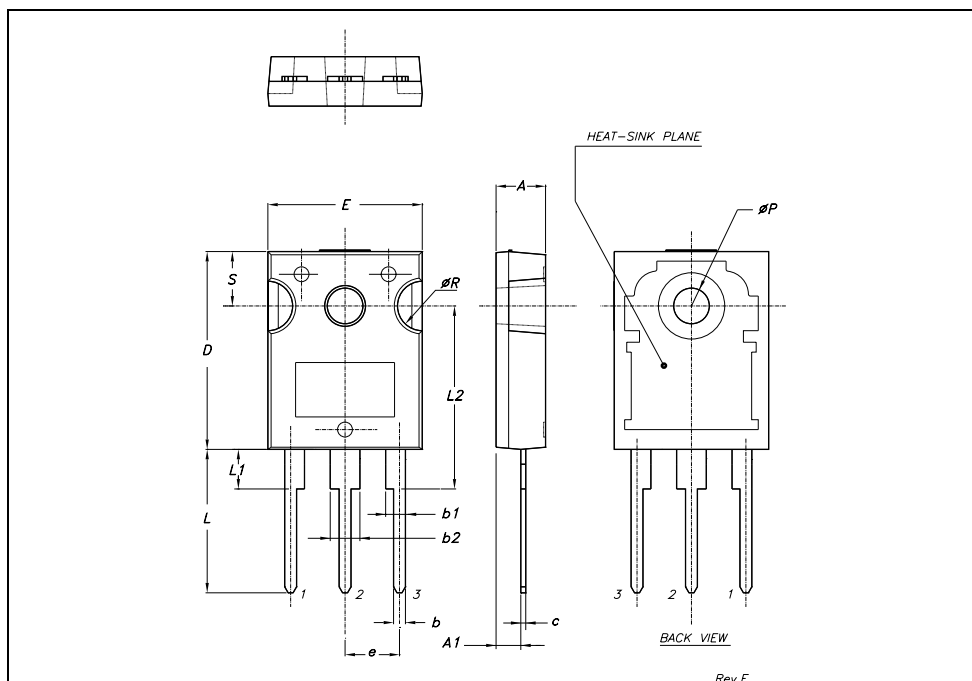
TO-262 (I²PAK) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
A1	2.40		2.72	0.094		0.107
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
c2	1.23		1.32	0.048		0.052
D	8.95		9.35	0.352		0.368
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
E	10		10.40	0.393		0.410
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L2	1.27		1.40	0.050		0.055



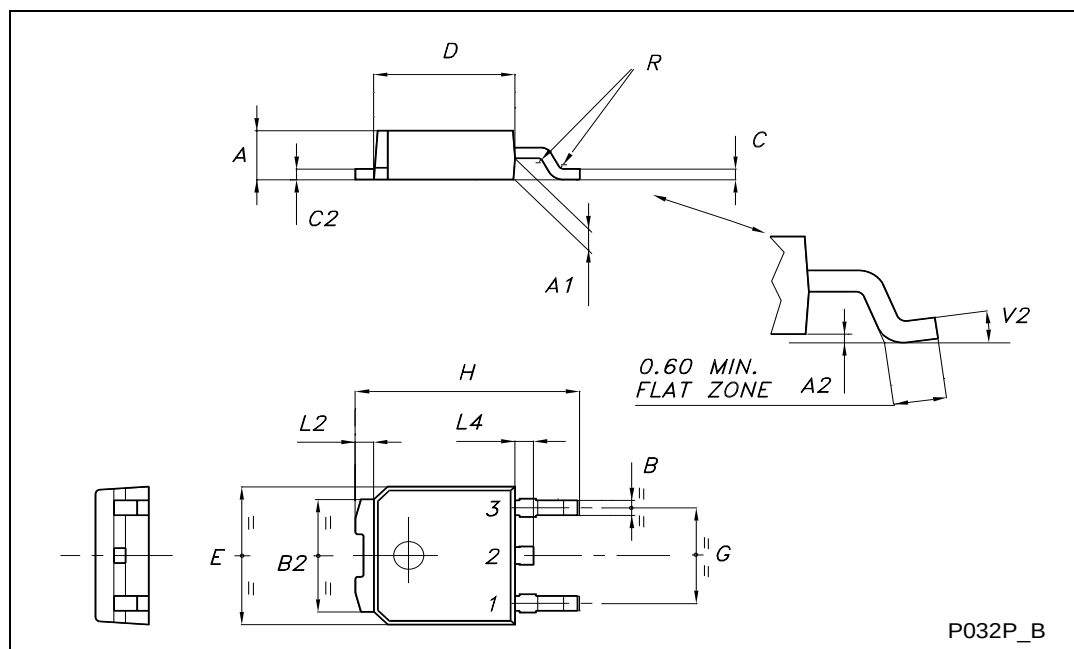
TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
ØP	3.55		3.65	0.140		0.143
ØR	4.50		5.50	0.177		0.216
S		5.50			0.216	

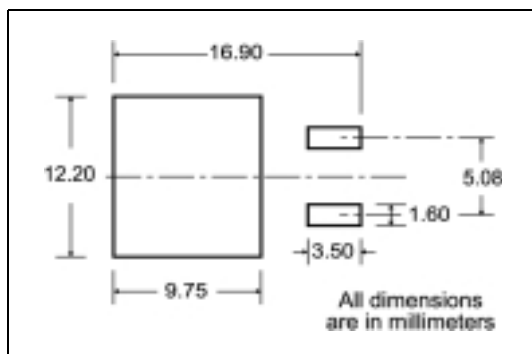


TO-252 (DPAK) MECHANICAL DATA

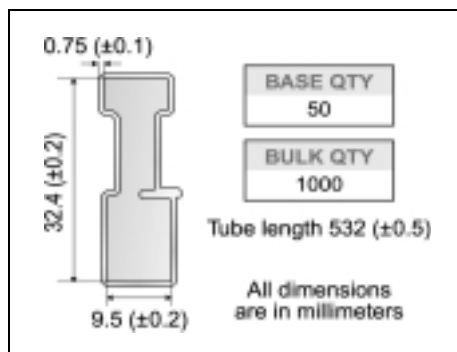
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°



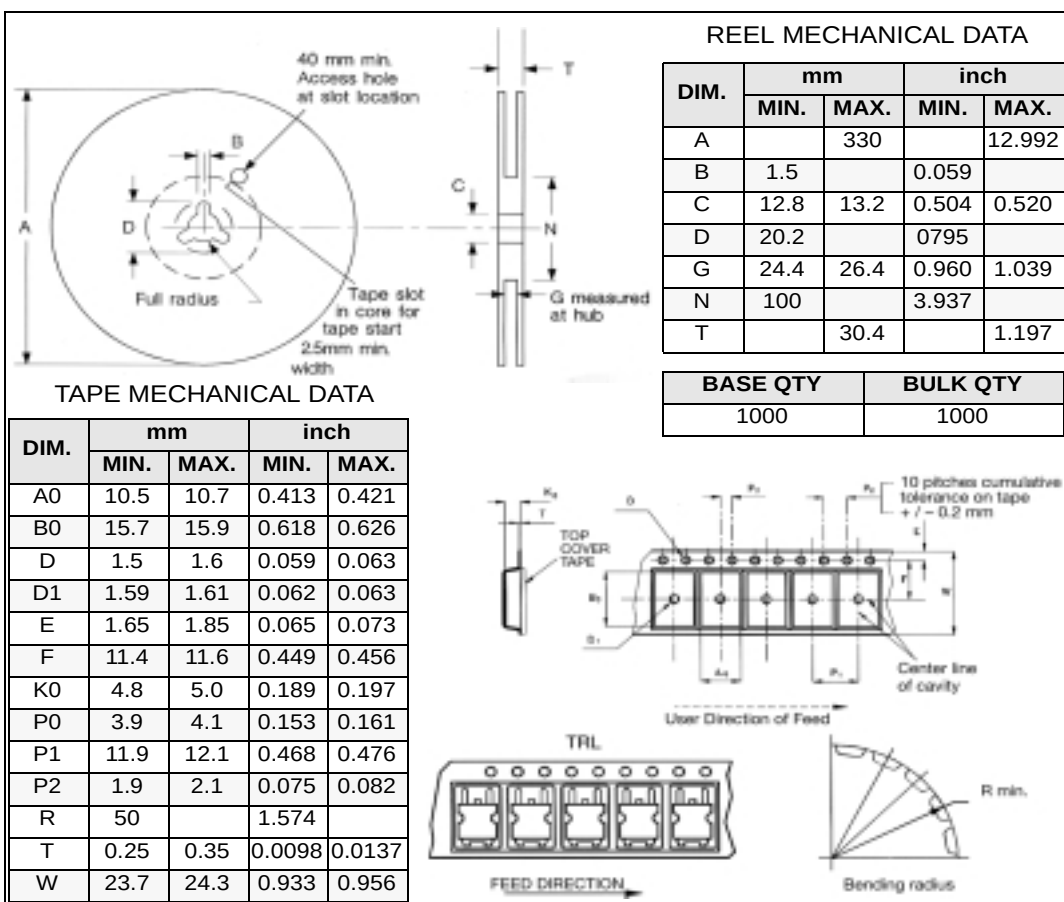
D²PAK FOOTPRINT



TUBE SHIPMENT (no suffix)*



TAPE AND REEL SHIPMENT (suffix "T4")*



* on sales type

Table 9: Revision History

Date	Revision	Description of Changes
30-Nov-2004	1	First Release.

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