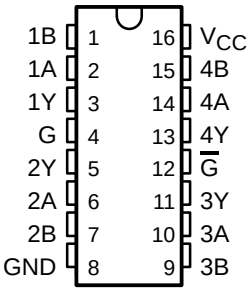
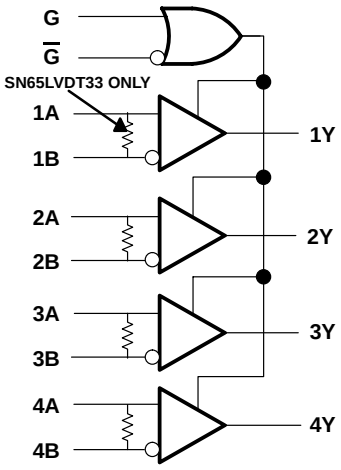
- **400-Mbps Signaling Rate[1] and 200-Mxfr/s Data Transfer Rate**
- **Operates With a Single 3.3-V Supply**
- **–4-V to 5-V Common-Mode Input Voltage Range**
- **Differential Input Thresholds <±50 mV With 50 mV of Hysteresis Over Entire Common-Mode Input Voltage Range**
- **Integrated 110-Ω Line Termination Resistors On LVDT Products**
- **TSSOP Packaging (33 Only)**
- **Complies With TIA/EIA-644 (LVDS)**
- **Active Failsafe Assures a High-Level Output With No Input**
- **Bus-Pin ESD Protection Exceeds 15 kV HBM**
- **Input Remains High-Impedance on Power Down**
- **TTL Inputs Are 5-V Tolerant**
- **Pin-Compatible With the AM26LS32, SN65LVDS32B, μA9637, SN65LVDS9637B**

SN65LVDS33D
SN65LVDT33D
SN65LVDS33PW
SN65LVDT33PW

D OR PW PACKAGE
(TOP VIEW)

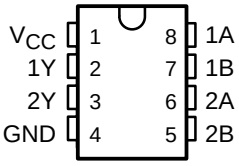


logic diagram (positive logic)

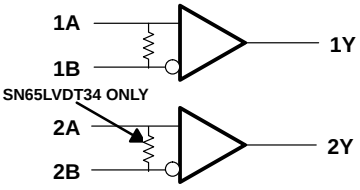


SN65LVDS34D
SN65LVDT34D

D PACKAGE
(TOP VIEW)



logic diagram (positive logic)



description

This family of four LVDS data line receivers offers the widest common-mode input voltage range in the industry. These receivers provide an input voltage range specification compatible with a 5-V PECL signal as well as an overall increased ground-noise tolerance. They are in industry standard footprints with integrated termination as an option.

Precise control of the differential input voltage thresholds allows for inclusion of 50 mV of input voltage hysteresis to improve noise rejection on slowly changing input signals. The input thresholds are still no more than ±50 mV over the full input common-mode voltage range.

The high-speed switching of LVDS signals usually necessitates the use of a line impedance matching resistor at the receiving-end of the cable or transmission media. The SN65LVDT series of receivers eliminates this external resistor by integrating it with the receiver. The nonterminated SN65LVDS series is also available for multidrop or other termination circuits.

AVAILABLE OPTIONS

PART NUMBER†	NUMBER OF RECEIVERS	TERMINATION RESISTOR	SYMBOLIZATION
SN65LVDS33D	4	No	LVDS33
SN65LVDS33PW	4	No	LVDS33
SN65LVDT33D	4	Yes	LVDT33
SN65LVDT33PW	4	Yes	LVDT33
SN65LVDS34D	2	No	LVDS34
SN65LVDT34D	2	Yes	LVDT34

† Add the suffix R for taped and reeled carrier.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

[1]The signalling rate of a line, is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

description (continued)

The receivers can withstand ±15 kV human-body model (HBM) and ±600 V machine model (MM) electrostatic discharges to the receiver input pins with respect to ground without damage. This provides reliability in cabled and other connections where potentially damaging noise is always a threat.

The receivers also include a (patent pending) failsafe circuit that will provide a high-level output within 600 ns after loss of the input signal. The most common causes of signal loss are disconnected cables, shorted lines, or powered-down transmitters. The failsafe circuit prevents noise from being received as valid data under these fault conditions. This feature may also be used for Wired-Or bus signaling. See *The Active Failsafe Feature of the SN65LVDS32B* application note.

The intended application and signaling technique of these devices is point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The SN65LVDS33, SN65LVDT33, SN65LVDS34 and SN65LVDT34 are characterized for operation from –40°C to 85°C.

Function Tables

SN65LVDS33 and SN65LVDT33

DIFFERENTIAL INPUT	ENABLES		OUTPUT
$V_{ID} = V_A - V_B$	G	$\overline{G}$	Y
$V_{ID} \geq$ -32 mV	H	X	H
	X	L	H
–100 mV < $V_{ID} \leq$ –32 mV	H	X	?
	X	L	?
$V_{ID} \leq$ –100 mV	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

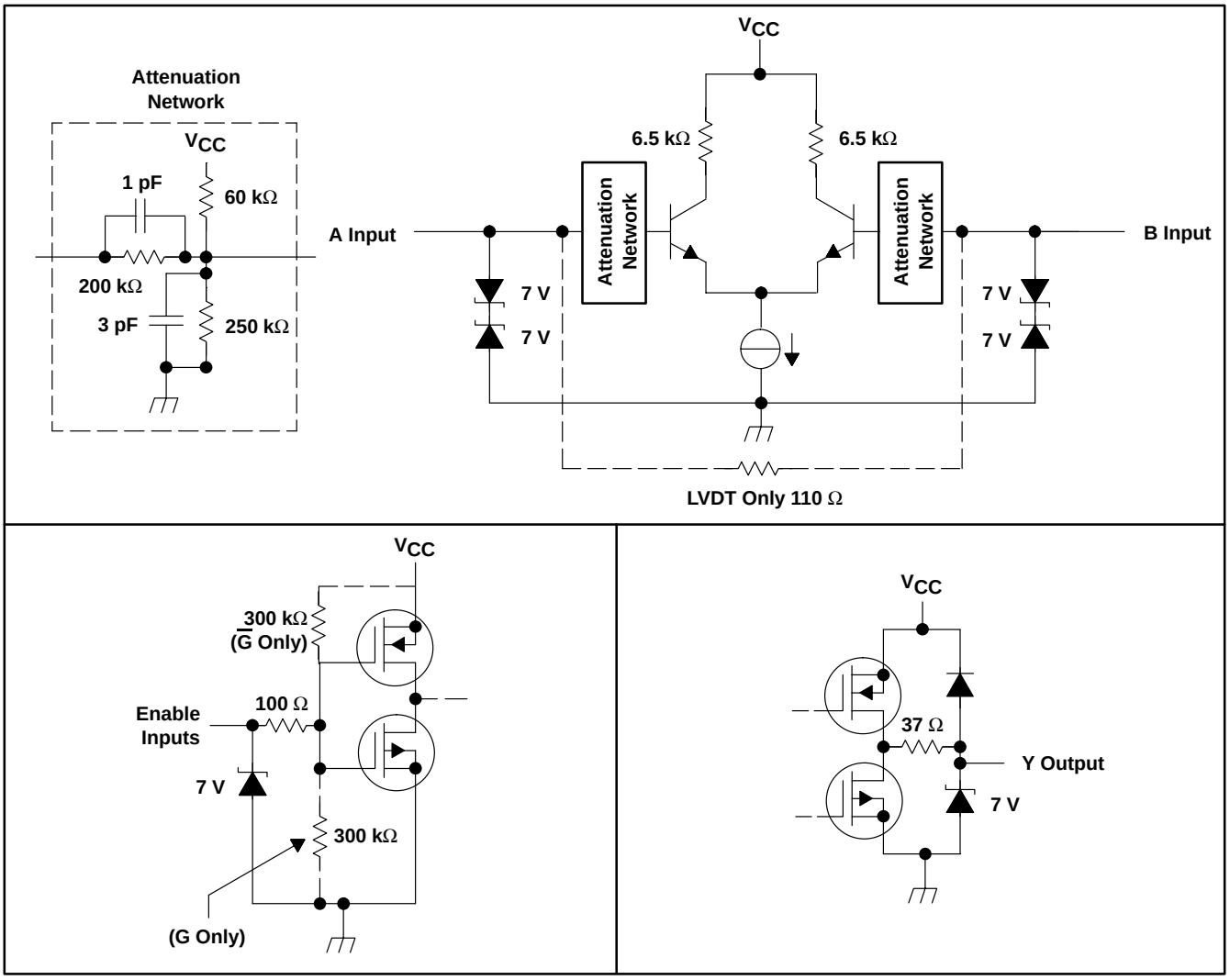
H = high level, L = low level, X = irrelevant,
Z = high impedance (off), ? = indeterminate

SN65LVDS34 and SN65LVDT34

DIFFERENTIAL INPUT	OUTPUT
$V_{ID} = V_A - V_B$	Y
$V_{ID} \geq$ -32 mV	H
–100 mV < $V_{ID} \leq$ –32 mV	?
$V_{ID} \leq$ -100 mV	L
Open	H

H = high level, L = low level,
? = indeterminate

equivalent input and output schematic diagrams



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 4 V
Voltage range: Enables or Y . . . . . –1 V to 6 V
A or B . . . . . –5 V to 6 V
$|V_A – V_B|$ (LVDT) . . . . . 1 V
Electrostatic discharge: A, B, and GND (see Note 2) . . . . . Class 3, A: 15 kV, B: 600 V
Charged-device mode: All pins (see Note 3) . . . . . ±500 V
Continuous power dissipation . . . . . See Dissipation Rating Table
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
2. Tested in accordance with JEDEC Standard 22, Test Method A114-A.
3. Tested in accordance with JEDEC Standard 22, Test Method C101.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D8	725 mW	5.8 mW/°C	377 mW
PW16	774 mW	6.2 mW/°C	402 mW
D16	950 mW	7.6 mW/°C	494 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
High-level input voltage, V_{IH}	Enables	2		5	V
Low-level input voltage, V_{IL}	Enables	0		0.8	V
Magnitude of differential input voltage, $\|V_{ID}\|$	LVDS	0.1		3	V
	LVDT			0.8	
Voltage at any bus terminal (separately or common-mode), V_I or V_{IC}		–4		5	V
Operating free-air temperature, T_A		–40		85	°C

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT1}	Positive-going differential input voltage threshold		V_{IB} = –4 V or 5 V, See Figures 1 and 2			50	mV
V_{IT2}	Negative-going differential input voltage threshold			–50			
V_{IT3}	Differential input failsafe voltage threshold		See Table 1 and Figure 5	–32		–100	mV
$V_{ID(HYS)}$	Differential input voltage hysteresis, $V_{IT1} – V_{IT2}$				50		mV
V_{OH}	High-level output voltage		I_{OH} = –4 mA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 4 mA			0.4	V
I_{CC}	Supply current	SN65LVDx33	G at V_{CC}, No load, Steady-state		16	23	mA
			G at GND		1.1	5	
		SN65LVDx34	No load, Steady-state		8	12	
I_I	Input current (A or B inputs)	SN65LVDS	V_I = 0 V, Other input open			±20	µA
			V_I = 2.4 V, Other input open			±20	
			V_I = –4 V, Other input open			±75	
			V_I = 5 V, Other input open			±40	
		SN65LVDT	V_I = 0 V, Other input open			±40	µA
			V_I = 2.4 V, Other input open			±40	
			V_I = –4 V, Other input open			±150	
			V_I = 5 V, Other input open			±80	
I_{ID}	Differential input current ($I_{IA} – I_{IB}$)	SN65LVDS	V_{ID} = 100 mV, V_{IC}= –4 V or 5 V			±3	µA
		SN65LVDT	V_{ID} = 200 mV, V_{IC}= –4 V or 5 V	1.55		2.22	mA
$I_{I(OFF)}$	Power-off input current (A or B inputs)	SN65LVDS	V_A or V_B = 0 V or 2.4 V, V_{CC} = 0 V			±20	µA
			V_A or V_B = –4 or 5 V, V_{CC} = 0 V			±50	
		SN65LVDT	V_A or V_B =0 V or 2.4 V, V_{CC} = 0 V			±30	
			V_A or V_B = –4 V or 5 V, V_{CC} = 0 V			±100	
I_{IH}	High-level input current (enables)		V_{IH} = 2 V			10	µA
I_{IL}	Low-level input current (enables)		V_{IL} = 0.8 V			10	µA
I_{OZ}	High-impedance output current			–10		10	µA
C_I	Input capacitance, A or B input to GND		V_I = 0.4 sin (4E6πt) + 0.5 V		5		pF

† All typical values are at 25°C and with a 3.3 V supply.

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{PLH(1)}$	Propagation delay time, low-to-high-level output	See Figure 3	2.5	4	6	ns
$t_{PHL(1)}$	Propagation delay time, high-to-low-level output		2.5	4	6	ns
t_{d1}	Delay time, failsafe deactivate time	C_L = 10 pF, See Figures 3 and 6			9	ns
t_{d2}	Delay time, failsafe activate time		0.3		1.5	µs
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL(1)} - t_{PLH(1)} \rvert$)	See Figure 3		200		ps
$t_{sk(o)}$	Output skew‡			150		ps
$t_{sk(pp)}$	Part-to-part skew§				1	ns
t_r	Output signal rise time			0.8		ns
t_f	Output signal fall time			0.8		ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	See Figure 4		5.5	9	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			4.4	9	ns
t_{PZH}	Propagation delay time, high-impedance -to-high-level output			3.8	9	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			7	9	ns

† All typical values are at 25°C and with a 3.3-V supply.
‡ $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} or t_{PHL} of all receivers of a single device with all of their inputs driven together.
§ $t_{sk(pp)}$ is the magnitude of the time difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

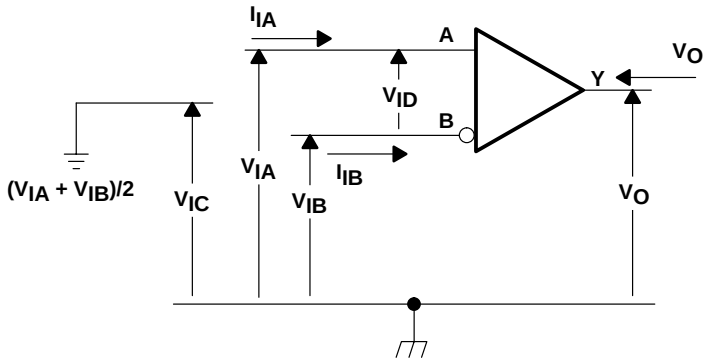
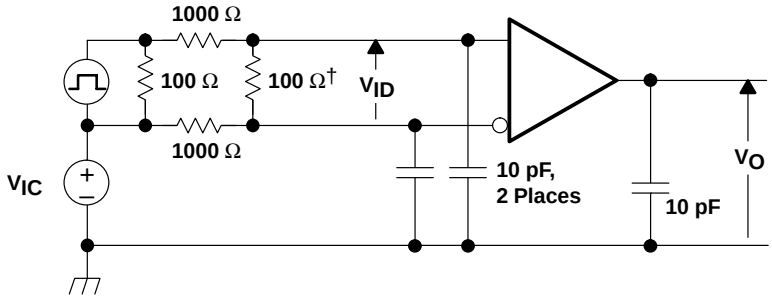
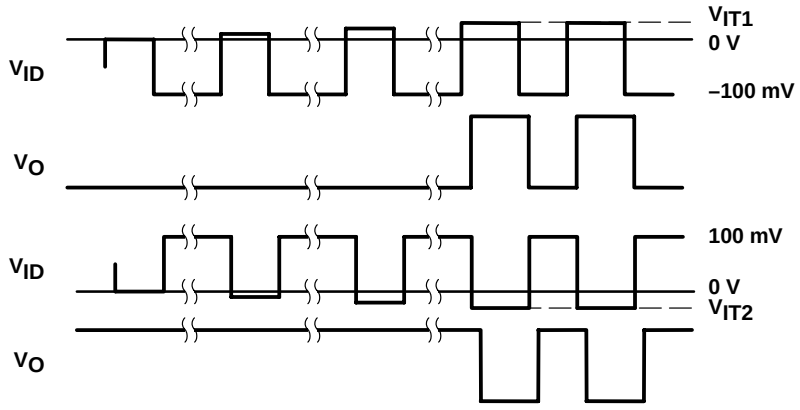


Figure 1. Voltage and Current Definitions



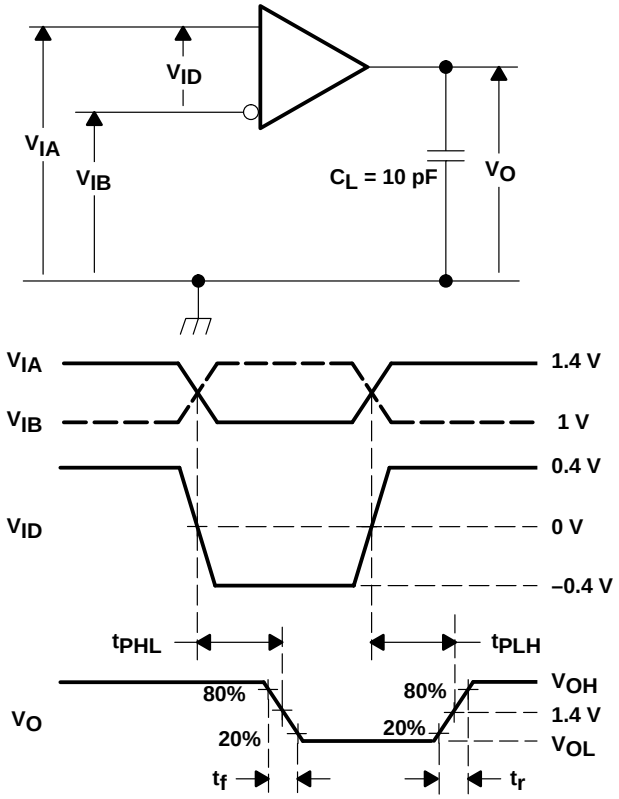
† Remove for testing LVDT device.



NOTE: Input signal of 3 Mpps, duration of 167 ns, and transition time of <1 ns.

Figure 2. V_{IT1} and V_{IT2} Input Voltage Threshold Test Circuit and Definitions

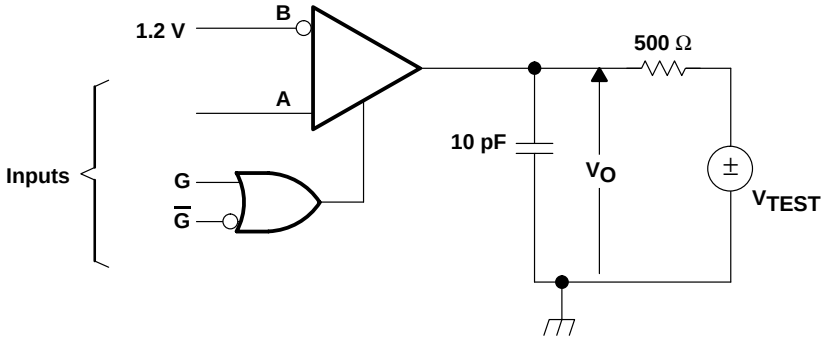
PARAMETER MEASUREMENT INFORMATION



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulsewidth = 10 ±0.2 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 3. Timing Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulsewidth = 500 ±10 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

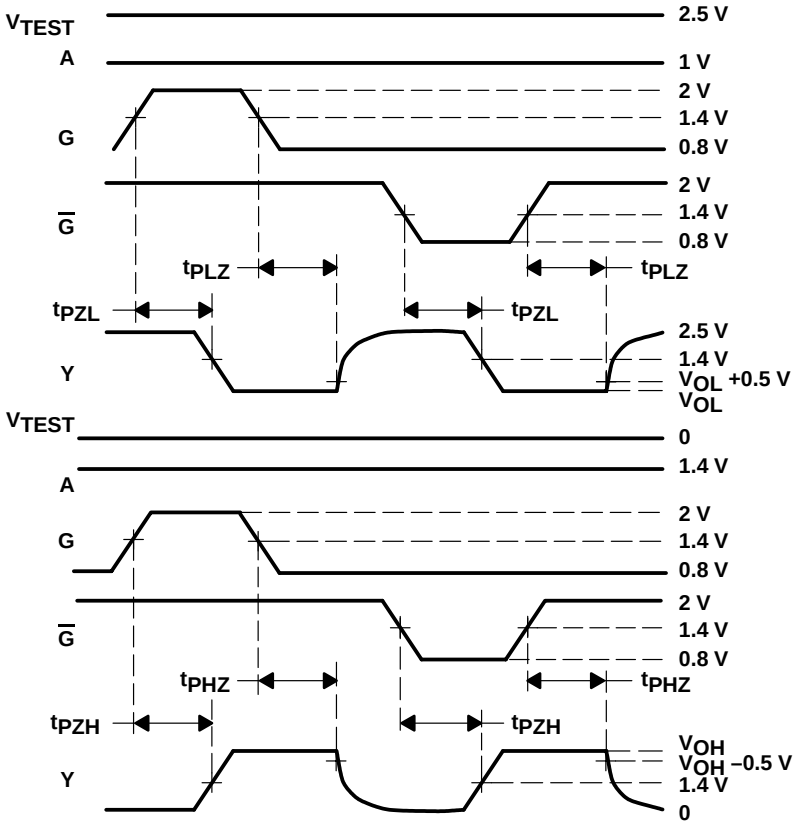


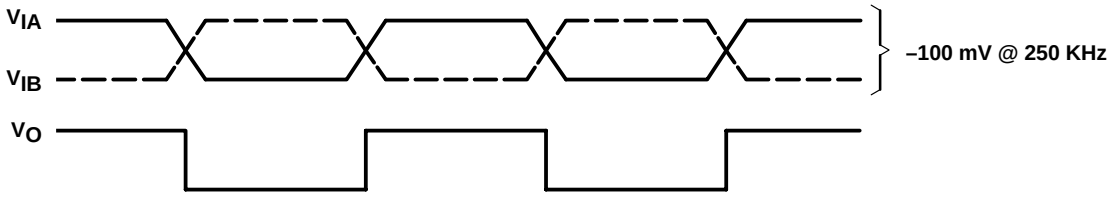
Figure 4. Enable/Disable Time Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION

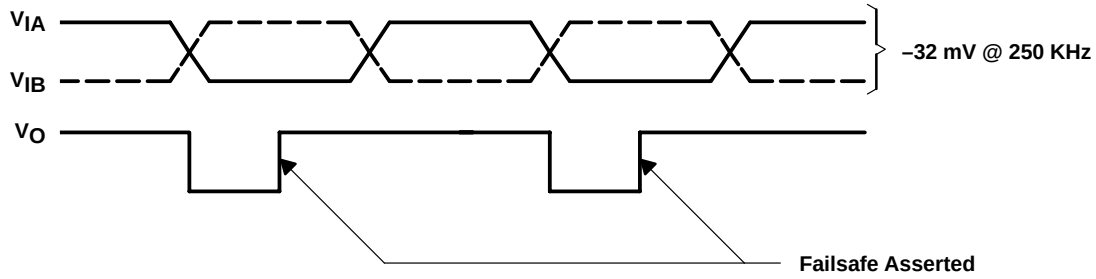
Table 1. Receiver Minimum and Maximum V_{IT3} Input Threshold Test Voltages

APPLIED VOLTAGES†		RESULTANT INPUTS		
V_{IA} (mV)	V_{IB} (mV)	V_{ID} (mV)	V_{IC} (mV)	Output
–4000	–3900	–100	–3950	L
–4000	–3968	–32	–3984	H
4900	5000	–100	4950	L
4968	5000	–32	4984	H

† These voltages are applied for a minimum of 1.5 µs.



a) No Failsafe



b) Failsafe Asserted

Figure 5. V_{IT3} Failsafe Threshold Test

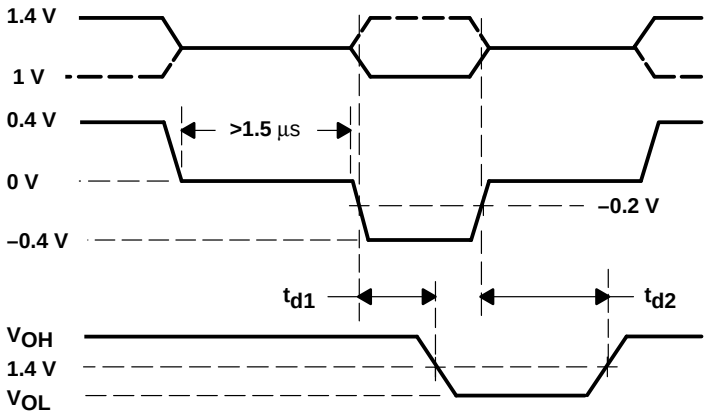


Figure 6. Waveforms for Failsafe Activate and Deactivate

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

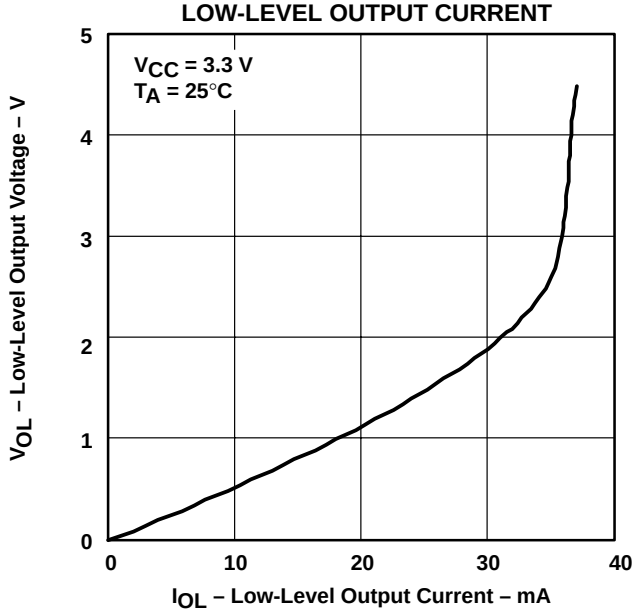


Figure 7

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

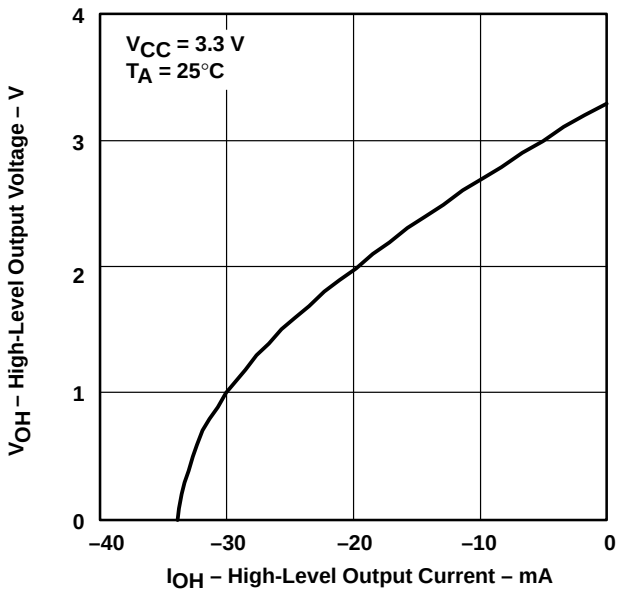


Figure 8

LOW-TO-HIGH PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

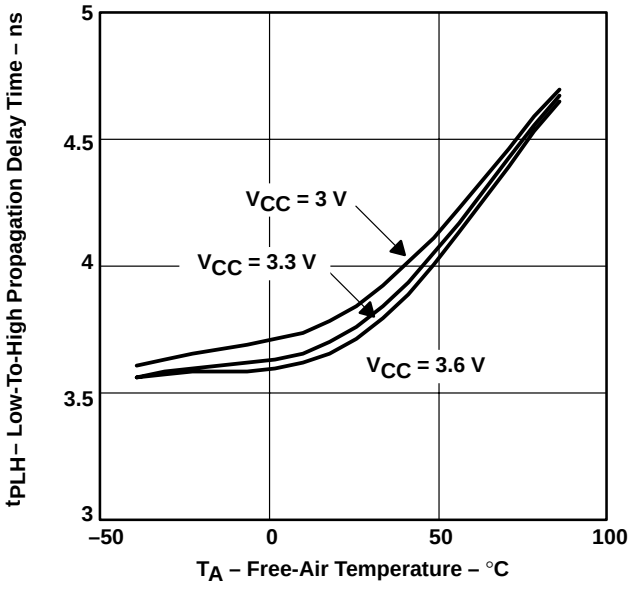


Figure 9

HIGH-TO-LOW PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

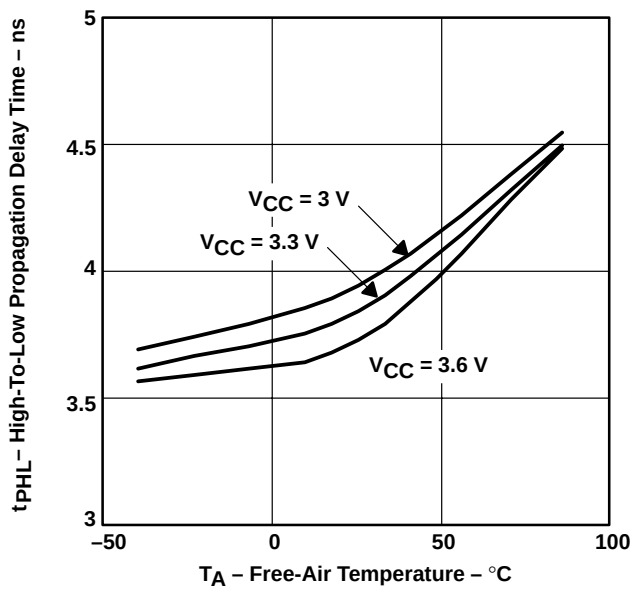


Figure 10

TYPICAL CHARACTERISTICS

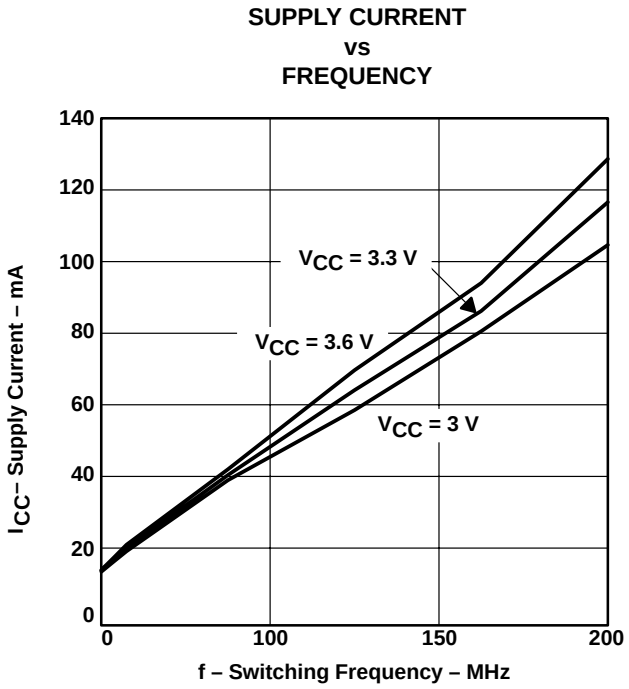
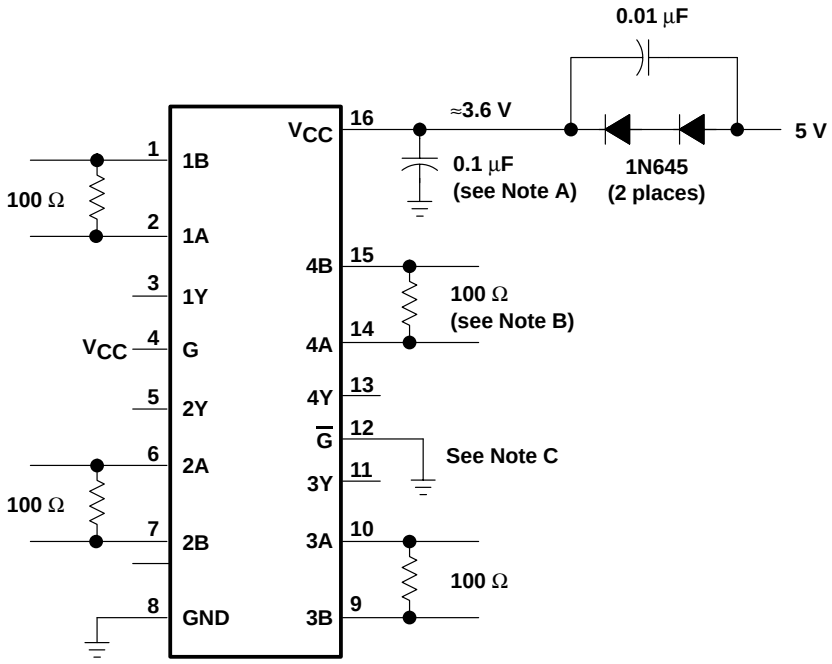


Figure 11

APPLICATION INFORMATION



NOTES: A. Place a 0.1-μF Z5U ceramic, mica or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitor should be located as close as possible to the device terminals.
B. The termination resistance value should match the nominal characteristic impedance of the transmission media with ±10%.
C. Unused enable inputs should be tied to V_{CC} or GND as appropriate.

Figure 12. Operation With 5-V Supply

related information

IBIS modeling is available for this device. Please contact the local TI sales office or the TI Web site at *www.ti.com* for more information.

For more application guidelines, please see the following documents:

- *Low-Voltage Differential Signalling Design Notes* (TI literature number SLLA014)
- *Interface Circuits for TIA/EIA-644* (LVDS) (SLLA038)
- *Reducing EMI With LVDS* (SLLA030)
- *Slew Rate Control of LVDS Circuits* (SLLA034)
- *Using an LVDS Receiver With RS-422 Data* (SLLA031)
- *Evaluating the LVDS EVM* (SLLA033)

APPLICATION INFORMATION

active failsafe feature

A differential line receiver commonly has a failsafe circuit to prevent it from switching on input noise. Current LVDS failsafe solutions require either external components with subsequent reductions in signal quality or integrated solutions with limited application. This family of receivers has a new integrated failsafe that solves the limitations seen in present solutions. A detailed theory of operation is presented in application note *The Active Failsafe Feature of the SN65LVDS32B,* literature number SLLA082A.

The following figure shows one receiver channel with active failsafe. It consists of a main receiver that can respond to a high-speed input differential signal. Also connected to the input pair are two failsafe receivers that form a window comparator. The window comparator has a much slower response than the main receiver and it detects when the input differential falls below 80 mV. A 600-ns failsafe timer filters the window comparator outputs. When failsafe is asserted, the failsafe logic drives the main receiver output to logic high.

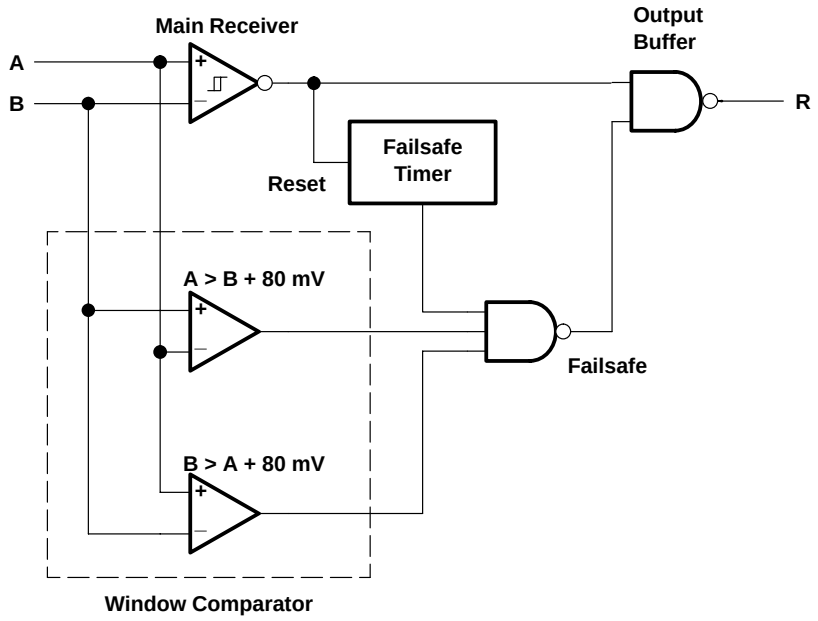


Figure 13. Receiver With Active Failsafe

APPLICATION INFORMATION

ECL/PECL-to-LVTTL conversion with TI's LVDS receiver

The various versions of emitter-coupled logic (i.e. ECL, PECL and LVPECL) are often the physical layer of choice for system designers. Designers know of the established technology and that it is capable of high-speed data transmission. In the past, system requirements often forced the selection of ECL. Now technologies like LVDS provide designers with another alternative. While the total exchange of ECL for LVDS may not be a design option, designers have been able to take advantage of LVDS by implementing a small resistor divider network at the input of the LVDS receiver. TI has taken the next step by introducing a wide common-mode LVDS receiver (no divider network required) which can be connected directly to an ECL driver with only the termination bias voltage required for ECL termination (V_{CC} – 2 V).

Figures 14 and 15 show the use of an LV/PECL driver driving 5 meters of CAT–5 cable and being received by TI's wide common-mode receiver and the resulting eye-pattern. The values for R3 are required in order to provide a resistor path to ground for the LV/PECL driver. With no resistor divider, R1 simply needs to match the characteristic load impedance of 50 Ω. The R2 resistor is a small value and is intended to minimize any possible common-mode current reflections.

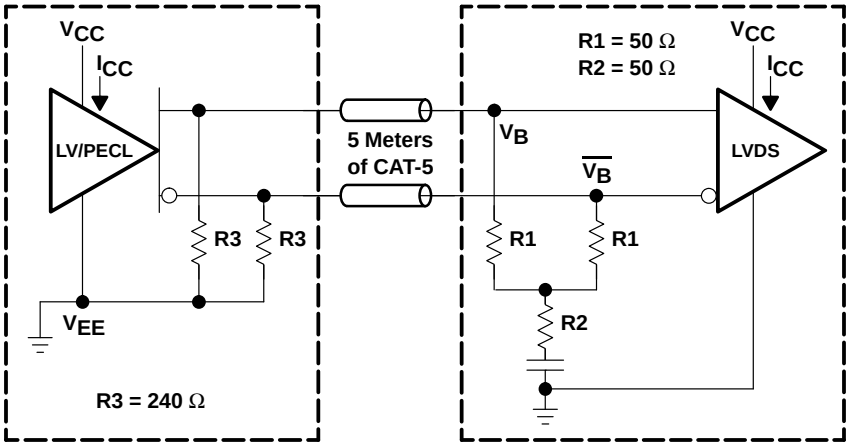


Figure 14. LVPECL or PECL to Remote Wide Common-Mode LVDS Receiver

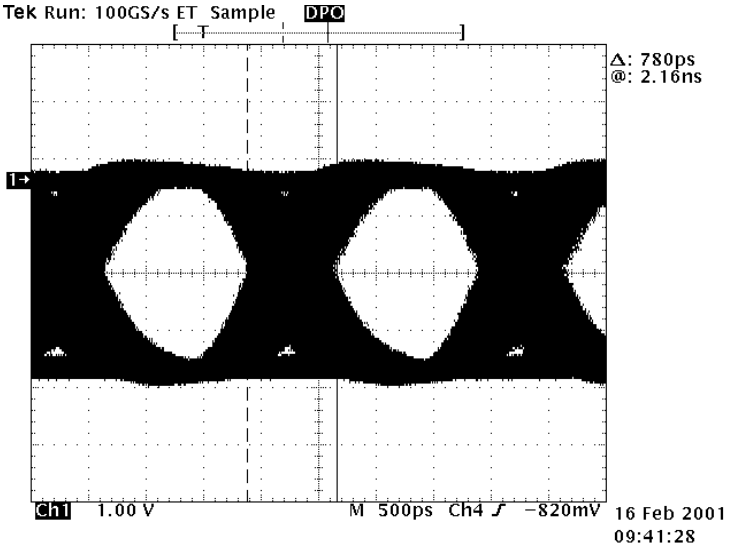


Figure 15. LV/PECL to Remote SN65LVDS33 at 500 Mbps Receiver Output (CH1)

APPLICATION INFORMATION

test conditions

- V_{CC} = 3.3 V
- T_A = 25°C (ambient temperature)
- All four channels switching simultaneously with NRZ data. Scope is pulse-triggered simultaneously with NRZ data.

equipment

- Tektronix PS25216 programmable power supply
- Tektronix HFS 9003 stimulus system
- Tektronix TDS 784D 4-channel digital phosphor oscilloscope – DPO

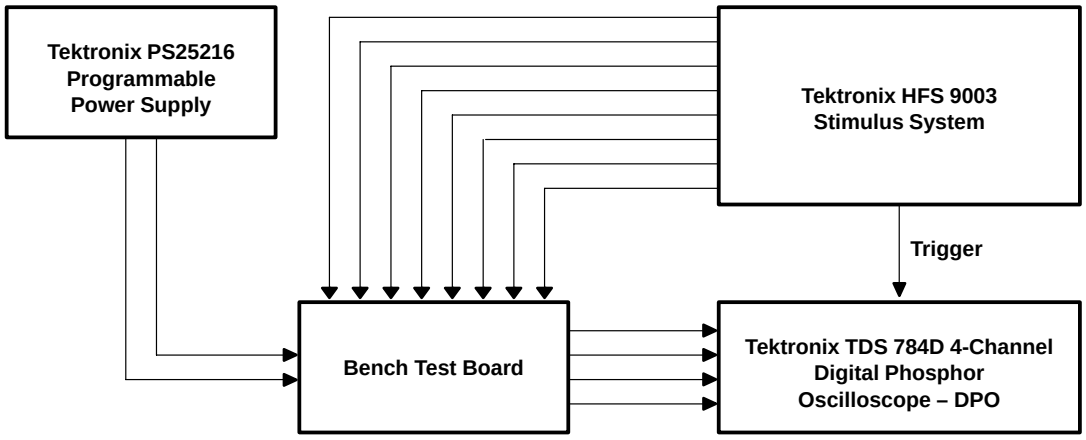
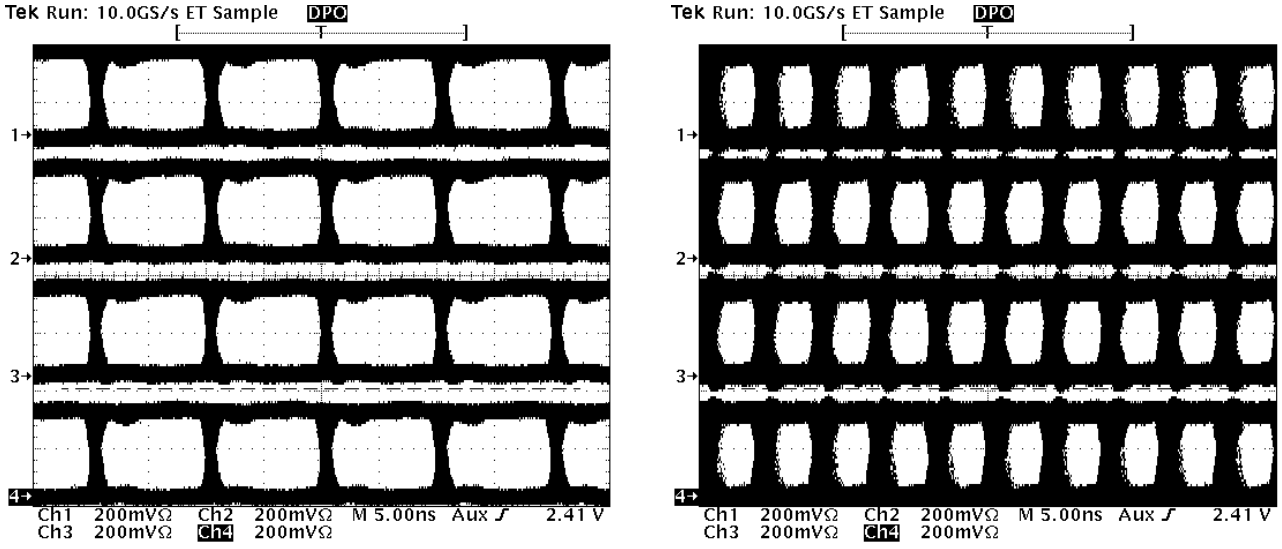


Figure 16. Equipment Setup



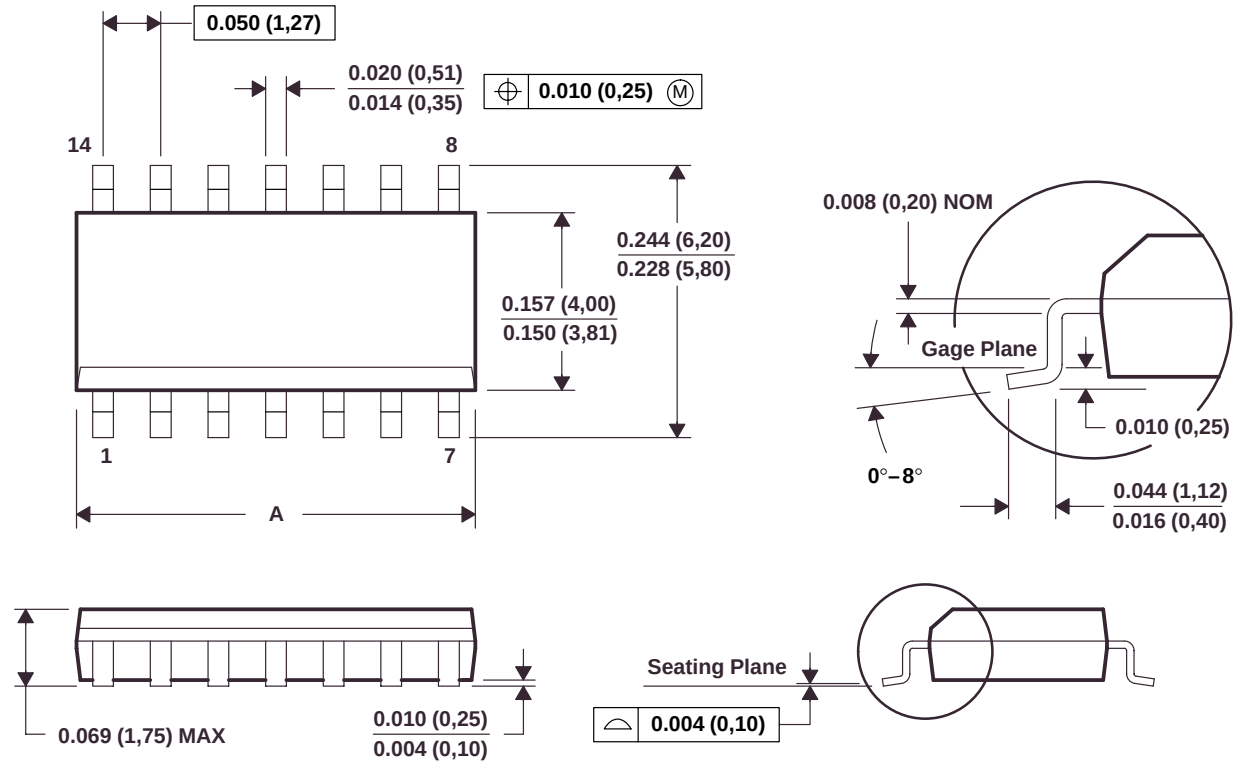
100 Mbit/s **200 Mbit/s**

Figure 17. Typical Eye Pattern SN65LVDS33

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

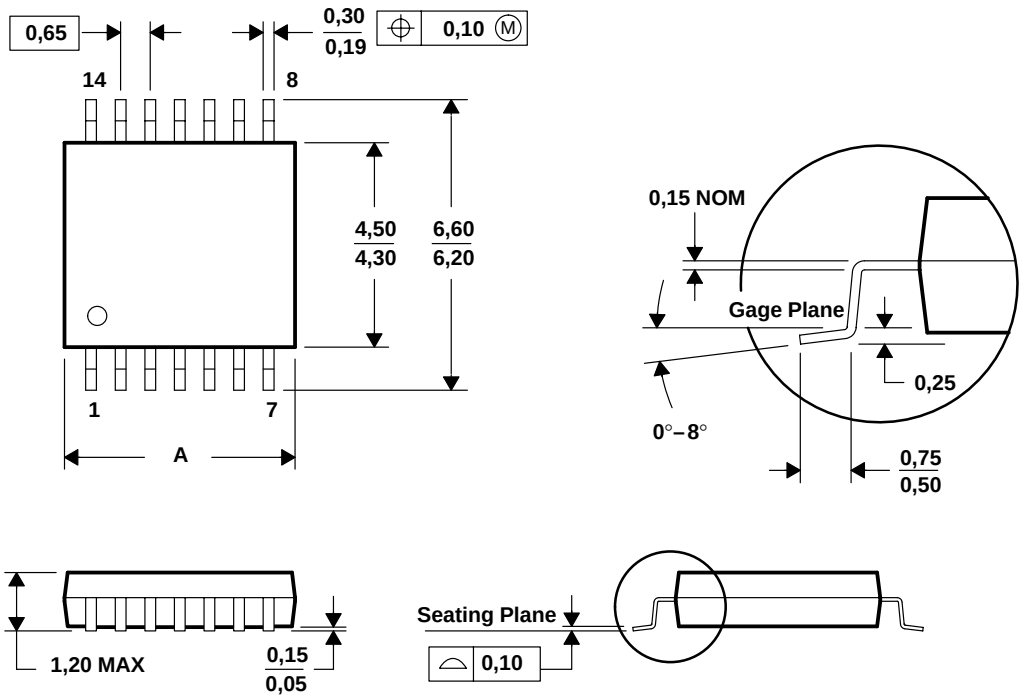
4040047/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, license, warranty or endorsement thereof.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations and notices. Representation or reproduction of this information with alteration voids all warranties provided for an associated TI product or service, is an unfair and deceptive business practice, and TI is not responsible nor liable for any such use.

Resale of TI's products or services with *statements different from or beyond the parameters* stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service, is an unfair and deceptive business practice, and TI is not responsible nor liable for any such use.

Also see: Standard Terms and Conditions of Sale for Semiconductor Products. www.ti.com/sc/docs/stdterms.htm

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265