SN54ACT374, SN74ACT374
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS
WITH 3-STATE OUTPUTS

- **Inputs Are TTL-Voltage Compatible**
- *EPIC*™ **(Enhanced-Performance Implanted CMOS) 1-μm Process**
- **Package Options Include Plastic Small-Outline (DW) Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic (N) and Ceramic (J) DIPs**

SN54ACT374 . . . J OR W PACKAGE
SN74ACT374 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)

$\overline{OE}$	1	20	V_{CC}
1Q	2	19	8Q
1D	3	18	8D
2D	4	17	7D
2Q	5	16	7Q
3Q	6	15	6Q
3D	7	14	6D
4D	8	13	5D
4Q	9	12	5Q
GND	10	11	CLK

SN54ACT374 . . . FK PACKAGE
(TOP VIEW)

Top pins: 1D, 1Q, $\overline{OE}$, V_{CC}, 8Q (pins 3, 2, 1, 20, 19)

Left pins: 2D (4), 2Q (5), 3Q (6), 3D (7), 4D (8)

Right pins: 8D (18), 7D (17), 7Q (16), 6Q (15), 6D (14)

Bottom pins: 4Q (9), GND (10), CLK (11), 5Q (12), 5D (13)

description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.
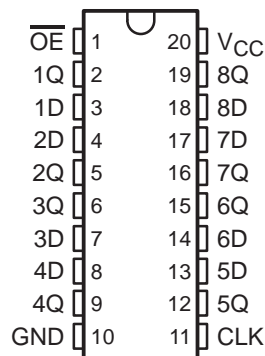
The eight flip-flops of the 'ACT374 devices are D-type edge-triggered flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines in bus-organized systems without need for interface or pullup components.
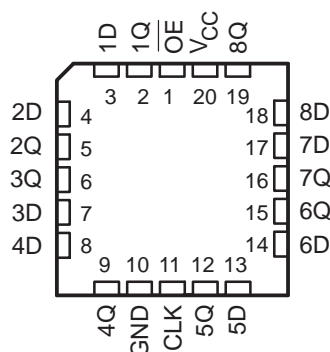
$\overline{OE}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ACT374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ACT374 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

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TEXAS INSTRUMENTS

logic symbol†

logic diagram (positive logic)

To Seven Other Channels

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and
IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . ±200 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package . . . . 70°C/W
DW package . . . . 58°C/W
N package . . . . 69°C/W
PW package . . . . 83°C/W
Storage temperature range, T_{stg} . . . . –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

TEXAS INSTRUMENTS

recommended operating conditions (see Note 3)

		SN54ACT374		SN74ACT374		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−24	mA
I_{OL}	Low-level output current		24		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	8	0	8	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25°C$			SN54ACT374		SN74ACT374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50$ µA	4.5 V	4.4	4.49		4.4		4.4		V
		5.5 V	5.4	5.49		5.4		5.4		
	$I_{OH} = -24$ mA	4.5 V	3.86			3.7		3.76		
		5.5 V	4.86			4.7		4.76		
	$I_{OH} = -50$ mA[†]	5.5 V				3.85				
	$I_{OH} = -75$ mA[†]	5.5 V						3.85		
V_{OL}	$I_{OL} = 50$ µA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	$I_{OL} = 24$ mA	4.5 V			0.36		0.44		0.44	
		5.5 V			0.36		0.5		0.44	
	$I_{OL} = 50$ mA[†]	5.5 V					1.65			
	$I_{OL} = 75$ mA[†]	5.5 V							1.65	
I_{OZ}	$V_O = V_{CC}$ or GND	5.5 V			±0.25		±5		±2.5	µA
I_I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	µA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		80		40	µA
ΔI_{CC}[‡]	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V		0.6			1.6		1.5	mA
C_i	$V_I = V_{CC}$ or GND	5 V		4.5						pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.
[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5$ V ± 0.5 V (unless otherwise noted) (see Figure 1)

		$T_A = 25°C$		SN54ACT374		SN74ACT374		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, CLK high or low	5		5		5		ns
t_{su}	Setup time, data before CLK↑	5		5.5		5.5		ns
t_h	Hold time, data after CLK↑	1.5		1.5		1.5		ns

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**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			SN54ACT374		SN74ACT374		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	160		70		90		MHz
t_{PLH}	CLK	Q	2	8.5	10	1.5	12	2	11.5	ns
t_{PHL}			2	8	9.5	1.5	11.5	1.5	11	
t_{PZH}	$\overline{OE}$	Q	2	8	9.5	1.5	11.5	1.5	10.5	ns
t_{PZL}			1.5	8	9	1.5	11.5	1.5	10.5	
t_{PHZ}	$\overline{OE}$	Q	1.5	8.5	11.5	1.5	13	1	12.5	ns
t_{PLZ}			1.5	7	8.5	1.5	11	1	10	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

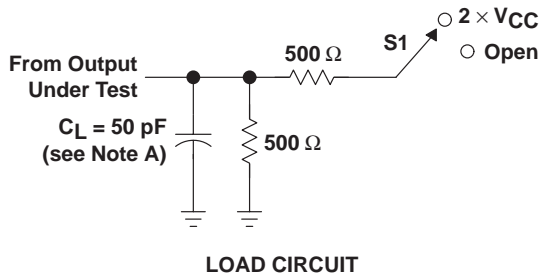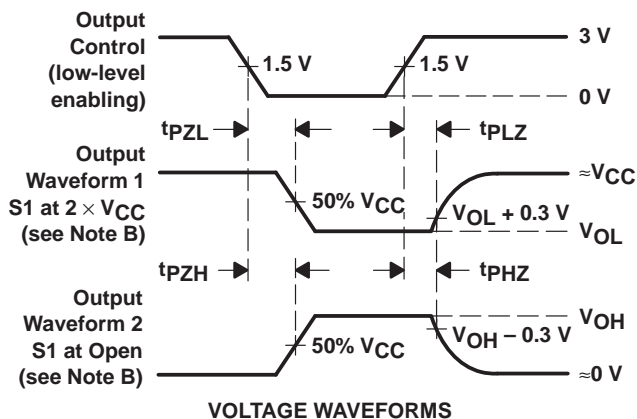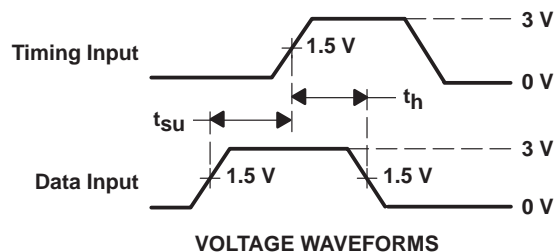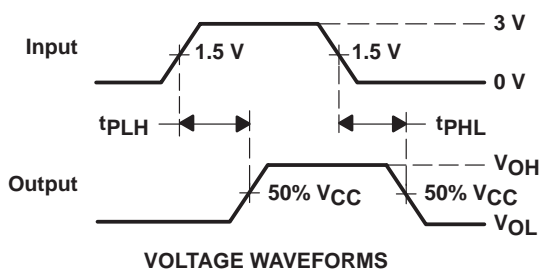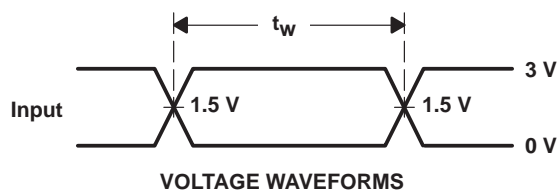| PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	40	pF

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PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open

VOLTAGE WAVEFORMS

VOLTAGE WAVEFORMS

VOLTAGE WAVEFORMS

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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