SN54AC74, SN74AC74
DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS
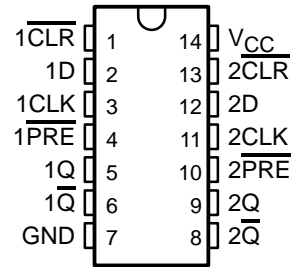## WITH CLEAR AND PRESET

- **2-V to 6-V V_{CC} Operation**
- **Inputs Accept Voltages to 6 V**
- **Max t_{pd} of 10 ns at 5 V**

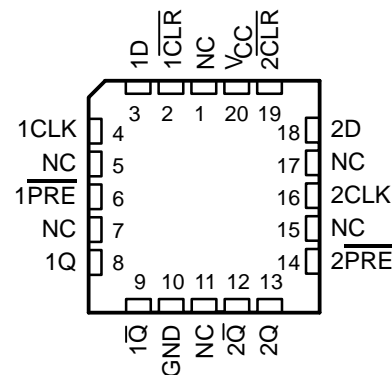## description/ordering information

The 'AC74 devices are dual positive-edge-triggered D-type flip-flops.

A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) input sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at D can be changed without affecting the levels at the outputs.

SN54AC74 . . . J OR W PACKAGE
SN74AC74 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)

$1\overline{CLR}$	1	14	V_{CC}
1D	2	13	$2\overline{CLR}$
1CLK	3	12	2D
$1\overline{PRE}$	4	11	2CLK
1Q	5	10	$2\overline{PRE}$
$1\overline{Q}$	6	9	2Q
GND	7	8	$2\overline{Q}$

SN54AC74 . . . FK PACKAGE
(TOP VIEW)

Top pins: 1D (3), $1\overline{CLR}$ (2), NC (1), V_{CC} (20), $2\overline{CLR}$ (19)

Left	Pin	Pin	Right
1CLK	4	18	2D
NC	5	17	NC
$1\overline{PRE}$	6	16	2CLK
NC	7	15	NC
1Q	8	14	$2\overline{PRE}$

Bottom pins: $1\overline{Q}$ (9), GND (10), NC (11), $2\overline{Q}$ (12), 2Q (13)

NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP – N	Tube	SN74AC74N	SN74AC74N
	SOIC – D	Tube	SN74AC74D	AC74
		Tape and reel	SN74AC74DR	
	SOP – NS	Tape and reel	SN74AC74NSR	AC74
	SSOP – DB	Tape and reel	SN74AC74DBR	AC74
	TSSOP – PW	Tape and reel	SN74AC74PWR	AC74
−55°C to 125°C	CDIP – J	Tube	SNJ54AC74J	SNJ54AC74J
	CFP – W	Tube	SNJ54AC74W	SNJ54AC74W
	LCCC – FK	Tube	SNJ54AC74FK	SNJ54AC74FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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TEXAS INSTRUMENTS

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† This configuration is unstable; that is, it does not persist when either $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

logic diagram, each flip-flop (positive logic)

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) .... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) .... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±50 mA
Continuous current through V_{CC} or GND .... ±200 mA
Package thermal impedance, θ_{JA} (see Note 2): D package .... 86°C/W
DB package .... 96°C/W
N package .... 80°C/W
NS package .... 76°C/W
PW package .... 113°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
       2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54AC74		SN74AC74		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	6	2	6	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1		2.1		V
		V_{CC} = 4.5 V	3.15		3.15		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 3 V		0.9		0.9	V
		V_{CC} = 4.5 V		1.35		1.35	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V		−12		−12	mA
		V_{CC} = 4.5 V		−24		−24	
		V_{CC} = 5.5 V		−24		−24	
I_{OL}	Low-level output current	V_{CC} = 3 V		12		12	mA
		V_{CC} = 4.5 V		24		24	
		V_{CC} = 5.5 V		24		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			8		8	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report,
Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	$T_A = 25°C$ MIN	$T_A = 25°C$ TYP	$T_A = 25°C$ MAX	SN54AC74 MIN	SN54AC74 MAX	SN74AC74 MIN	SN74AC74 MAX	UNIT
V_{OH}		$I_{OH} = -50\ \mu A$	3 V	2.9	4.49		2.9		2.9		V
			4.5 V	4.4	5.49		4.4		4.4		
			5.5 V	5.4	5.49		5.4		5.4		
		$I_{OH} = -12\ mA$	3 V	2.56			2.4		2.46		
		$I_{OH} = -24\ mA$	4.5 V	3.86			3.7		3.76		
			5.5 V	4.86			4.7		4.76		
		$I_{OH} = -50\ mA$†	5.5 V				3.85				
		$I_{OH} = -75\ mA$†	5.5 V						3.85		
V_{OL}		$I_{OL} = 50\ \mu A$	3 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			5.5 V		0.001	0.1		0.1		0.1	
		$I_{OL} = 12\ mA$	3 V			0.36		0.5		0.44	
		$I_{OL} = 24\ mA$	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		$I_{OL} = 50\ mA$†	5.5 V					1.65			
		$I_{OL} = 75\ mA$†	5.5 V							1.65	
I_I	Data pins	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	µA
	Control pins					±0.1		±1		±1	
I_{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		40		20	µA
C_i		$V_I = V_{CC}$ or GND	5 V		3						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

timing requirements over recommended operating free-air temperature range,
$V_{CC} = 3.3\ V \pm 0.3\ V$ (unless otherwise noted) (see Figure 1)

			$T_A = 25°C$ MIN	$T_A = 25°C$ MAX	SN54AC74 MIN	SN54AC74 MAX	SN74AC74 MIN	SN74AC74 MAX	UNIT
f_{clock}	Clock frequency		0	100	0	100	0	100	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	5.5		8		7		ns
		CLK	5.5		8		7		
t_{su}	Setup time, data before CLK↑	Data	4		5		4.5		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	0		0.5		0		
t_h	Hold time, data after CLK↑		0.5		0.5		0.5		ns

timing requirements over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			$T_A = 25°C$		SN54AC74		SN74AC74		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	140	0	140	0	140	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	4.5		5.5		5		ns
		CLK	4.5		5.5		5		
t_{su}	Setup time, data before CLK↑	Data	3		4		3		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	0		0.5		0		
t_h	Hold time, data after CLK↑		0.5		0.5		0.5		ns

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25°C$			SN54AC74		SN74AC74		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	125		70		95		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3.5	8	12	1	13	2.5	13	ns
t_{PHL}			4	10.5	12	1	14	3.5	13.5	
t_{PLH}	CLK	Q or $\overline{Q}$	4.5	8	13.5	1	17.5	4	16	ns
t_{PHL}			3.5	8	14	1	13.5	3.5	14.5	

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25°C$			SN54AC74		SN74AC74		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			140	160		95		125		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2.5	6	9	1	9.5	2	10	ns
t_{PHL}			3	8	9.5	1	10.5	2.5	10.5	
t_{PLH}	CLK	Q or $\overline{Q}$	3.5	6	10	1	12	3	10.5	ns
t_{PHL}			2.5	6	10	1	10	2.5	10.5	

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TYP	UNIT
C_{pd} Power dissipation capacitance	C_L = 50 pF,	f = 1 MHz	45	pF

PARAMETER MEASUREMENT INFORMATION
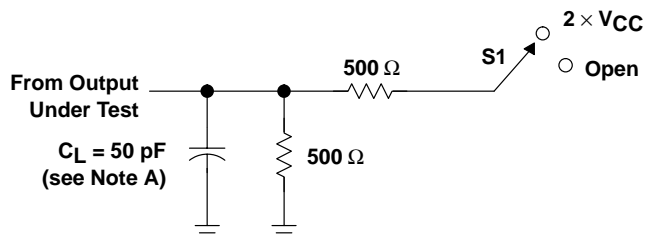
TEST	S1
t_{PLH}/t_{PHL}	Open

2 × V$_{CC}$

S1

○ **Open**

From Output Under Test

500 Ω

C$_L$ = 50 pF (see Note A)

500 Ω

LOAD CIRCUIT

Input

t$_w$

50% V$_{CC}$ **50% V$_{CC}$**

V$_{CC}$

0 V

VOLTAGE WAVEFORMS

Input

50% V$_{CC}$ **50% V$_{CC}$**

V$_{CC}$

0 V

t$_{PLH}$ **t$_{PHL}$**

In-Phase Output

50% V$_{CC}$ **50% V$_{CC}$**

V$_{OH}$

V$_{OL}$

t$_{PHL}$ **t$_{PLH}$**

Out-of-Phase Output

50% V$_{CC}$ **50% V$_{CC}$**

V$_{OH}$

V$_{OL}$

VOLTAGE WAVEFORMS

Timing Input

50% V$_{CC}$

V$_{CC}$

0 V

t$_{su}$ **t$_h$**

Data Input

50% V$_{CC}$ **50% V$_{CC}$**

V$_{CC}$

0 V
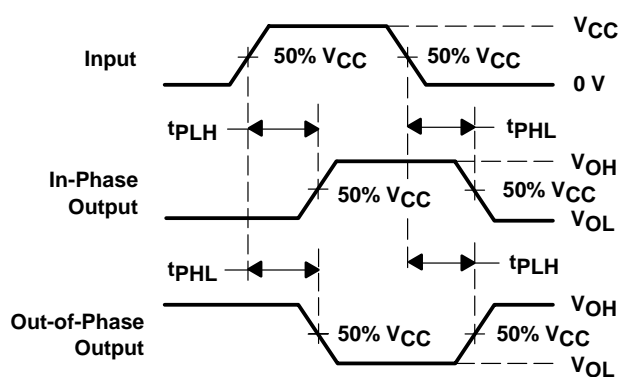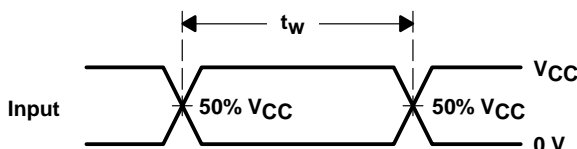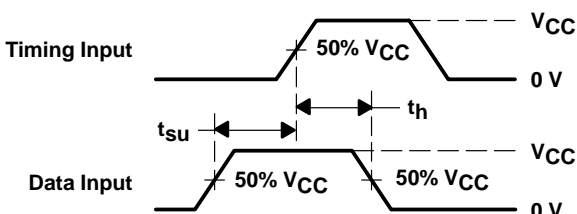
VOLTAGE WAVEFORMS

NOTES: A. C$_L$ includes probe and jig capacitance.
       B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z$_O$ = 50 Ω, t$_r$ ≤ 2.5 ns, t$_f$ ≤ 2.5 ns.
       C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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