

# DATA SHEET



## **SAF7129AH** Digital video encoder

Product specification  
Supersedes data of 2003 Jun 13

2004 Mar 16

**Digital video encoder****SAF7129AH****CONTENTS**

|      |                                |      |                                                                                |
|------|--------------------------------|------|--------------------------------------------------------------------------------|
| 1    | FEATURES                       | 8    | LIMITING VALUES                                                                |
| 2    | GENERAL DESCRIPTION            | 9    | THERMAL CHARACTERISTICS                                                        |
| 3    | ORDERING INFORMATION           | 10   | CHARACTERISTICS                                                                |
| 4    | QUICK REFERENCE DATA           | 10.1 | Explanation of RTCI data bits                                                  |
| 5    | BLOCK DIAGRAM                  | 10.2 | Teletext timing                                                                |
| 6    | PINNING                        | 11   | APPLICATION INFORMATION                                                        |
| 7    | FUNCTIONAL DESCRIPTION         | 11.1 | Digital output signals                                                         |
| 7.1  | Versatile fader                | 12   | PACKAGE OUTLINE                                                                |
| 7.2  | Data manager                   | 13   | SOLDERING                                                                      |
| 7.3  | Encoder                        | 13.1 | Introduction to soldering surface mount packages                               |
| 7.4  | RGB processor                  | 13.2 | Reflow soldering                                                               |
| 7.5  | SECAM processor                | 13.3 | Wave soldering                                                                 |
| 7.6  | Output interface/DACs          | 13.4 | Manual soldering                                                               |
| 7.7  | Synchronization                | 13.5 | Suitability of surface mount IC packages for wave and reflow soldering methods |
| 7.8  | Clock                          | 14   | DATA SHEET STATUS                                                              |
| 7.9  | I <sup>2</sup> C-bus interface | 15   | DEFINITIONS                                                                    |
| 7.10 | Input levels and formats       | 16   | DISCLAIMERS                                                                    |
| 7.11 | Bit allocation map             | 17   | PURCHASE OF PHILIPS I <sup>2</sup> C COMPONENTS                                |
| 7.12 | I <sup>2</sup> C-bus format    |      |                                                                                |
| 7.13 | Slave receiver                 |      |                                                                                |
| 7.14 | Slave transmitter              |      |                                                                                |

## Digital video encoder

## SAF7129AH

**1 FEATURES**

- Monolithic CMOS 3.3 V device, 5 V I<sup>2</sup>C-bus optional
- Digital PAL/NTSC/SECAM encoder
- System pixel frequency 13.5 MHz
- 54 MHz double-speed multiplexed D1 interface capable of splitting data into two separate channels (encoded and baseband)
- Three Digital-to-Analog Converters (DACs) for CVBS (CSYNC), VBS (CVBS) and C (CVBS) two times oversampled with 10-bit resolution (signals in brackets optional)
- Three DACs for RED (C<sub>R</sub>), GREEN (Y) and BLUE (C<sub>B</sub>) two times oversampled with 9-bit resolution (signals in brackets optional)
- Alternatively, an advanced composite sync is available on the CVBS output for RGB display centring
- Real-time control of subcarrier
- Cross-colour reduction filter
- Closed captioning encoding and World Standard Teletext (WST) and North-American Broadcast Text System (NABTS) teletext encoding including sequencer and filter
- Copy Generation Management System (CGMS) encoding (CGMS described by standard CPR-1204 of EIAJ); 20 bits in lines 20/283 (NTSC) can be loaded via I<sup>2</sup>C-bus
- Fast I<sup>2</sup>C-bus control port (400 kHz)
- Line 23 Wide Screen Signalling (WSS) encoding
- Video Programming System (VPS) data encoding in line 16 (50/625 lines counting)
- Encoder can be master or slave
- Programmable horizontal and vertical input synchronization phase
- Programmable horizontal sync output phase
- Internal Colour Bar Generator (CBG)
- Controlled rise/fall times of output syncs and blanking
- On-chip crystal oscillator (3rd-harmonic or fundamental crystal)
- Down mode (low output voltage) or power-save mode of DACs
- QFP44 package.

**2 GENERAL DESCRIPTION**

The SAF7129AH encodes digital C<sub>B</sub>-Y-C<sub>R</sub> video data to an NTSC, PAL or SECAM CVBS or S-video signal. Simultaneously, RGB or bypassed but interpolated C<sub>B</sub>-Y-C<sub>R</sub> signals are available via three additional DACs. Through a 54 MHz multiplexed digital D1 input port, the circuit accepts two ITU-R BT.656 compatible C<sub>B</sub>-Y-C<sub>R</sub> data streams with 720 active pixels per line in 4 : 2 : 2 multiplexed formats. For example, an MPEG decoded data with overlay and MPEG decoded data without overlay, where one data stream is latched at the rising, the other one is latched at the falling clock edge.

It includes a sync/clock generator and on-chip DACs.

**3 ORDERING INFORMATION**

| TYPE NUMBER | PACKAGE |                                                                               |          |
|-------------|---------|-------------------------------------------------------------------------------|----------|
|             | NAME    | DESCRIPTION                                                                   | VERSION  |
| SAF7129AH   | QFP44   | plastic quad flat package; 44 leads (lead length 1.6 mm); body 10 × 10 × 2 mm | SOT803-1 |

## Digital video encoder

## SAF7129AH

## 4 QUICK REFERENCE DATA

| SYMBOL              | PARAMETER                                                                                                                     | MIN.           | TYP. | MAX. | UNIT     |
|---------------------|-------------------------------------------------------------------------------------------------------------------------------|----------------|------|------|----------|
| V <sub>DDA</sub>    | analog supply voltage                                                                                                         | 3.15           | 3.3  | 3.45 | V        |
| V <sub>DDD</sub>    | digital supply voltage                                                                                                        | 3.0            | 3.3  | 3.6  | V        |
| I <sub>DDA</sub>    | analog supply current                                                                                                         | –              | 180  | 190  | mA       |
| I <sub>DDD</sub>    | digital supply current                                                                                                        | –              | 40   | 55   | mA       |
| V <sub>i</sub>      | input signal voltage levels                                                                                                   | TTL compatible |      |      |          |
| V <sub>o(p-p)</sub> | analog CVBS output signal voltage for a <sup>100</sup> / <sub>100</sub> colour bar at 75/2 $\Omega$ load (peak-to-peak value) | –              | 1.23 | –    | V        |
| R <sub>L</sub>      | load resistance                                                                                                               | –              | 37.5 | –    | $\Omega$ |
| LE <sub>lf(i)</sub> | low frequency integral linearity error                                                                                        | –              | –    | ±3   | LSB      |
| LE <sub>lf(d)</sub> | low frequency differential linearity error                                                                                    | –              | –    | ±1   | LSB      |
| T <sub>amb</sub>    | ambient temperature                                                                                                           | –40            | –    | +85  | °C       |

Digital video encoder

SAF7129AH

5 BLOCK DIAGRAM

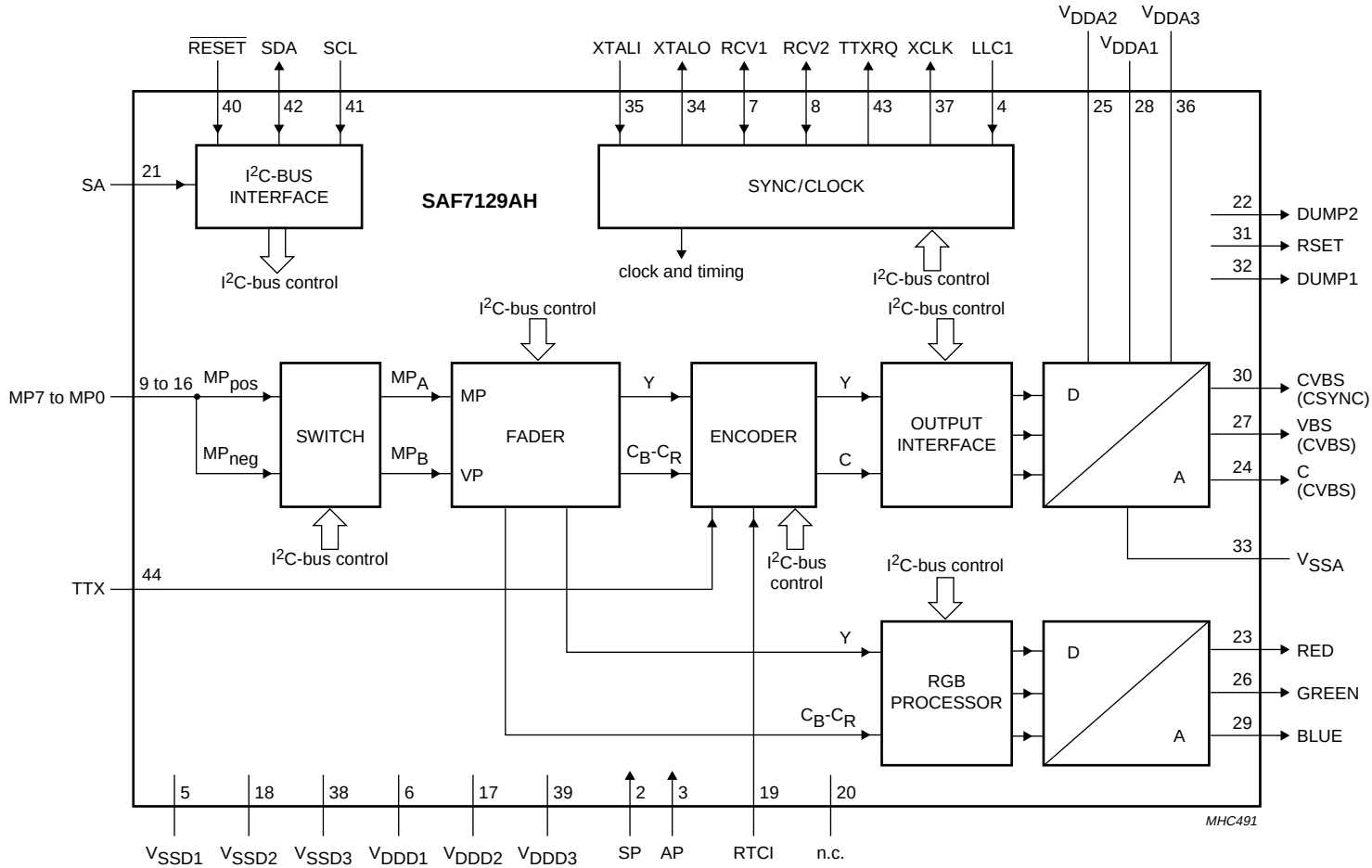


Fig.1 Block diagram.

## Digital video encoder

## SAF7129AH

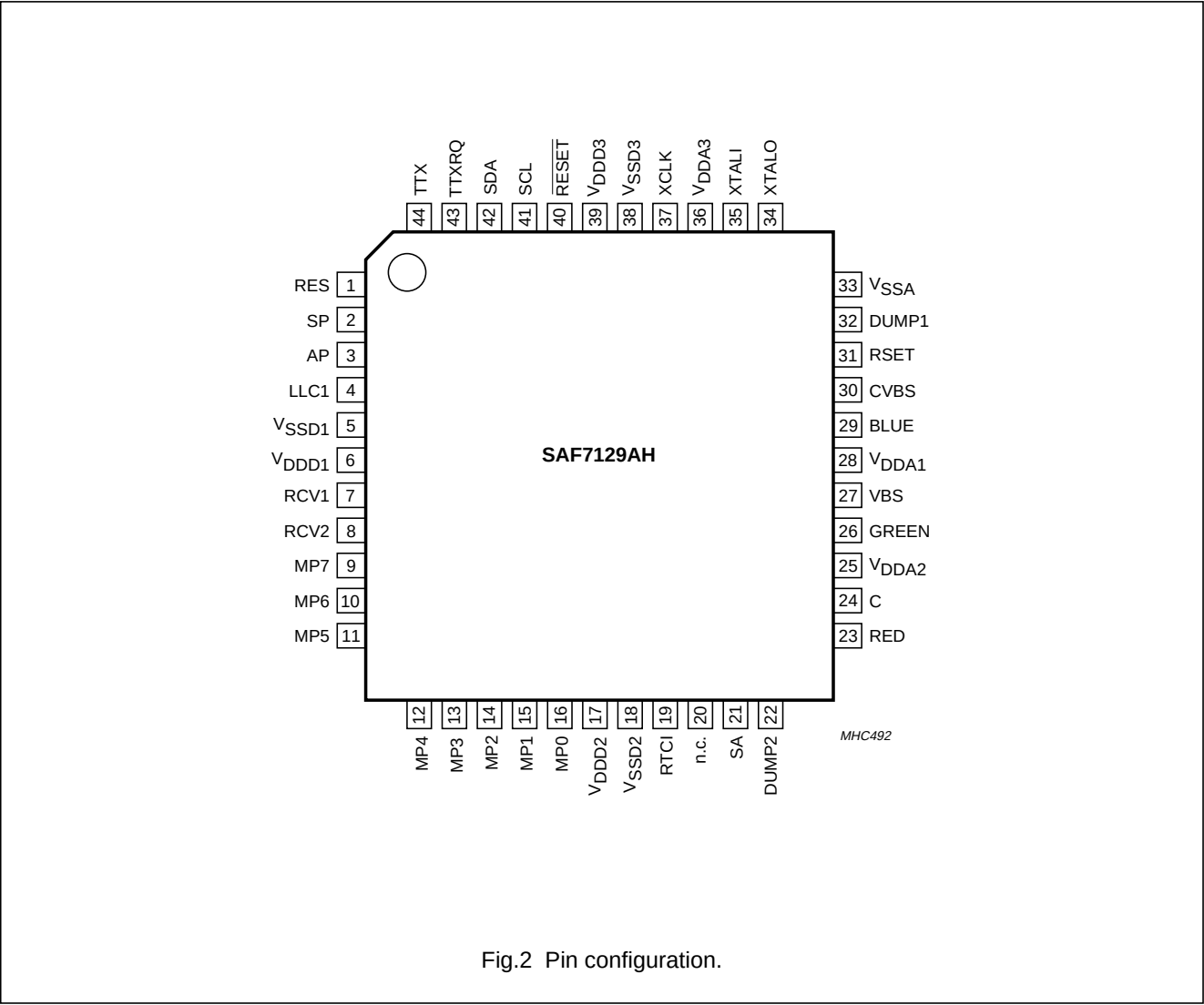
## 6 PINNING

| SYMBOL            | PIN | TYPE   | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                       |
|-------------------|-----|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RES               | 1   | –      | reserved pin; do not connect                                                                                                                                                                                                                                                                                                                                                      |
| SP                | 2   | I      | test pin; connected to digital ground for normal operation                                                                                                                                                                                                                                                                                                                        |
| AP                | 3   | I      | test pin; connected to digital ground for normal operation                                                                                                                                                                                                                                                                                                                        |
| LLC1              | 4   | I      | line-locked clock input; this is the 27 MHz master clock                                                                                                                                                                                                                                                                                                                          |
| V <sub>SSD1</sub> | 5   | supply | digital ground 1                                                                                                                                                                                                                                                                                                                                                                  |
| V <sub>DD1</sub>  | 6   | supply | digital supply voltage 1                                                                                                                                                                                                                                                                                                                                                          |
| RCV1              | 7   | I/O    | raster control 1 for video port; this pin receives/provides a VS/FS/FSEQ signal                                                                                                                                                                                                                                                                                                   |
| RCV2              | 8   | I/O    | raster control 2 for video port; this pin provides an HS pulse of programmable length or receives an HS pulse                                                                                                                                                                                                                                                                     |
| MP7               | 9   | I      | double-speed 54 MHz MPEG port; it is an input for “ITU-R BT.656” style multiplexed C <sub>B</sub> -Y-C <sub>R</sub> data; data is sampled on the rising and falling clock edge; data sampled on the rising edge is then sent to the encoding part of the device; data sampled on the falling edge is sent to the RGB part of the device (or vice versa, depending on programming) |
| MP6               | 10  | I      |                                                                                                                                                                                                                                                                                                                                                                                   |
| MP5               | 11  | I      |                                                                                                                                                                                                                                                                                                                                                                                   |
| MP4               | 12  | I      |                                                                                                                                                                                                                                                                                                                                                                                   |
| MP3               | 13  | I      |                                                                                                                                                                                                                                                                                                                                                                                   |
| MP2               | 14  | I      |                                                                                                                                                                                                                                                                                                                                                                                   |
| MP1               | 15  | I      |                                                                                                                                                                                                                                                                                                                                                                                   |
| MP0               | 16  | I      |                                                                                                                                                                                                                                                                                                                                                                                   |
| V <sub>DD2</sub>  | 17  | supply | digital supply voltage 2                                                                                                                                                                                                                                                                                                                                                          |
| V <sub>SS2</sub>  | 18  | supply | digital ground 2                                                                                                                                                                                                                                                                                                                                                                  |
| RTCI              | 19  | I      | real-time control input; if the LLC1 clock is provided by an SAF7113 or SAF7118, RTCI should be connected to the RTCO pin of the respective decoder to improve the signal quality                                                                                                                                                                                                 |
| n.c.              | 20  | –      | not connected                                                                                                                                                                                                                                                                                                                                                                     |
| SA                | 21  | I      | select I <sup>2</sup> C-bus address; LOW selects slave address 88H, HIGH selects slave address 8CH                                                                                                                                                                                                                                                                                |
| DUMP2             | 22  | O      | current return path 2 for DAC                                                                                                                                                                                                                                                                                                                                                     |
| RED               | 23  | O      | analog output of RED (C <sub>R</sub> ) signal                                                                                                                                                                                                                                                                                                                                     |
| C                 | 24  | O      | analog output of chrominance (CVBS) signal                                                                                                                                                                                                                                                                                                                                        |
| V <sub>DDA2</sub> | 25  | supply | analog supply voltage 2 for analog outputs                                                                                                                                                                                                                                                                                                                                        |
| GREEN             | 26  | O      | analog output of GREEN (Y) signal                                                                                                                                                                                                                                                                                                                                                 |
| VBS               | 27  | O      | analog output of VBS (CVBS) signal                                                                                                                                                                                                                                                                                                                                                |
| V <sub>DDA1</sub> | 28  | supply | analog supply voltage 1 for analog outputs                                                                                                                                                                                                                                                                                                                                        |
| BLUE              | 29  | O      | analog output of BLUE (C <sub>B</sub> ) signal                                                                                                                                                                                                                                                                                                                                    |
| CVBS              | 30  | O      | analog output of CVBS (CSYNC) signal                                                                                                                                                                                                                                                                                                                                              |
| RSET              | 31  | O      | a resistor of 1 k $\Omega$ (R <sub>out</sub> = 37 k $\Omega$ ) connected to V <sub>SSA</sub> sets the full-scale DAC current                                                                                                                                                                                                                                                      |
| DUMP1             | 32  | O      | current return path 1 for DAC                                                                                                                                                                                                                                                                                                                                                     |
| V <sub>SSA</sub>  | 33  | supply | analog ground for the DAC reference ladder and the oscillator                                                                                                                                                                                                                                                                                                                     |
| XTALO             | 34  | O      | crystal oscillator output                                                                                                                                                                                                                                                                                                                                                         |
| XTALI             | 35  | I      | crystal oscillator input; if the oscillator is not used, this pin should be connected to ground                                                                                                                                                                                                                                                                                   |
| V <sub>DDA3</sub> | 36  | supply | analog supply voltage 3 for the DAC reference ladder and the oscillator                                                                                                                                                                                                                                                                                                           |
| XCLK              | 37  | O      | clock output of the crystal oscillator                                                                                                                                                                                                                                                                                                                                            |

Digital video encoder

SAF7129AH

| SYMBOL            | PIN | TYPE   | DESCRIPTION                                                                                                                                                                                                                  |
|-------------------|-----|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| V <sub>SSD3</sub> | 38  | supply | digital ground 3                                                                                                                                                                                                             |
| V <sub>DDD3</sub> | 39  | supply | digital supply voltage 3                                                                                                                                                                                                     |
| RESET             | 40  | I      | Reset input, active LOW. After reset is applied, all digital I/Os are in input mode; PAL black burst on CVBS, VBS and C; RGB outputs set to lowest voltage. The I <sup>2</sup> C-bus receiver waits for the START condition. |
| SCL               | 41  | I      | I <sup>2</sup> C-bus serial clock input                                                                                                                                                                                      |
| SDA               | 42  | I/O    | I <sup>2</sup> C-bus serial data input/output                                                                                                                                                                                |
| TTXRQ             | 43  | O      | teletext request output, indicating when text bits are requested                                                                                                                                                             |
| TTX               | 44  | I      | teletext bit stream input                                                                                                                                                                                                    |



## Digital video encoder

## SAF7129AH

### 7 FUNCTIONAL DESCRIPTION

The digital video encoder encodes digital luminance and colour difference signals into analog CVBS, S-video and simultaneously RGB or  $C_R$ -Y- $C_B$  signals. NTSC-M, PAL-B/G, SECAM and sub-standards are supported.

Both interlaced and non-interlaced operation is possible for all standards.

The basic encoder function consists of subcarrier generation, colour modulation and insertion of synchronization signals. Luminance and chrominance signals are filtered in accordance with the standard requirements of "RS-170-A" and "ITU-R BT.470-3".

For ease of analog post filtering, the signals are twice oversampled with respect to the pixel clock before digital-to-analog conversion.

The total filter transfer characteristics are illustrated in Figs 8 to 13. The DACs for Y, C and CVBS are realized with full 10-bit resolution; 9-bit resolution for RGB output. The  $C_R$ -Y- $C_B$  to RGB dematrix can be bypassed optionally in order to provide the upsampled  $C_R$ -Y- $C_B$  input signals.

The 8-bit multiplexed  $C_B$ -Y- $C_R$  formats are "ITU-R BT.656" (D1 format) compatible, but the SAV and EAV codes can be decoded optionally, when the device is operated in slave mode. Two independent data streams can be processed, one latched by the rising edge of LLC1, the other latched by the falling edge of LLC1. The purpose of that is e.g. to forward one of the data streams containing both video and On-Screen Display (OSD) information to the RGB outputs, and the other stream containing video only to the encoded outputs CVBS and S-video.

For optimum display of RGB signals through a euro-connector TV set, an early composite sync pulse (up to 31 LLC1 clock periods) can be provided on the CVBS output.

As a further alternative, the VBS and C outputs may provide a second and third CVBS signal.

It is also possible to connect a Philips digital video decoder (SAF7113 or SAF7118) to the SAF7129AH. Via the RTCI pin, connected to pin RTCO of a decoder, information concerning actual subcarrier, PAL-ID and definite subcarrier phase can be inserted.

The device synthesizes all necessary internal signals, colour subcarrier frequency and synchronization signals from that clock.

Wide screen signalling data can be loaded via the I<sup>2</sup>C-bus and is inserted into line 23 for standards using 50 Hz field rate.

VPS data for program dependent automatic start and stop of such featured VCR's is loadable via I<sup>2</sup>C-bus.

The IC also contains closed caption and extended data services encoding (line 21). It is also possible to load data for copy generation management system into line 20 of every field (525/60 line counting).

A number of possibilities are provided for setting different video parameters, such as:

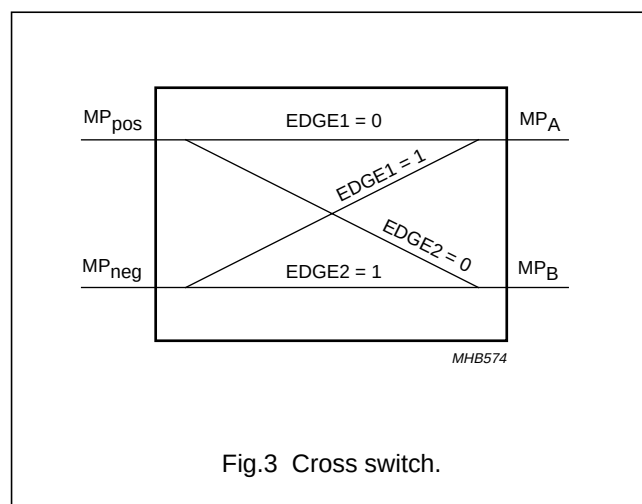
- Black and blanking level control
- Colour subcarrier frequency
- Variable burst amplitude, etc.

During reset ( $\overline{\text{RESET}} = \text{LOW}$ ) and after reset is released, all digital I/O stages are set to input mode and the encoder is set to PAL mode and outputs a 'black burst' signal on CVBS and S-video outputs, while RGB outputs are set to their lowest output voltages. A reset forces the I<sup>2</sup>C-bus interface to abort any running bus transfer.

#### 7.1 Versatile fader

**Important note:** whenever the fader is activated with the SYMP bit set to a logic 1 (enabling the detection of embedded Start of Active Video (SAV) and End of Active Video (EAV)), codes 00H and FFH are not allowed within the actual video data (as prescribed by "ITU-R BT.656", anyway). If SAV (00H) has been detected, the fader automatically passes 100% of the respective signal until SAV will be detected.

Within the digital video encoder, two data streams can be faded against each other; these data streams can be input to the double speed MPEG port, which is able to separate two independent 27 MHz data streams  $MP_A$  and  $MP_B$  via a cross switch controlled by EDGE1 and EDGE2.





Digital video encoder

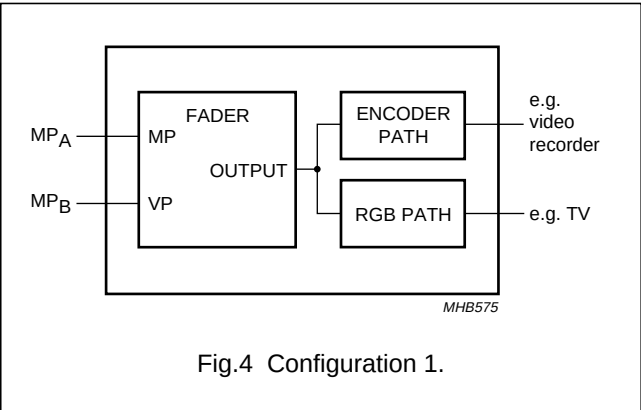
SAF7129AH

7.1.1 CONFIGURATION EXAMPLES

Figs 4 to 7 show examples on how to configure the fader between the input ports and the outputs, separated into the composite (and S-video) encoder and the RGB encoder.

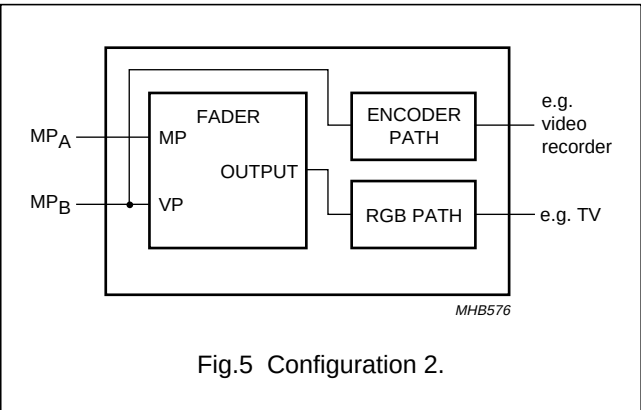
7.1.1.1 Configuration 1

Input MP<sub>A</sub> can be faded into MP<sub>B</sub>. The resulting output of the fader is then encoded simultaneously to composite (and S-video) and RGB output (RGBIN = ENCIN = 1). In this example, either MP<sub>A</sub> or MP<sub>B</sub> could be an overlay (menu) signal to be faded smoothly in and out.



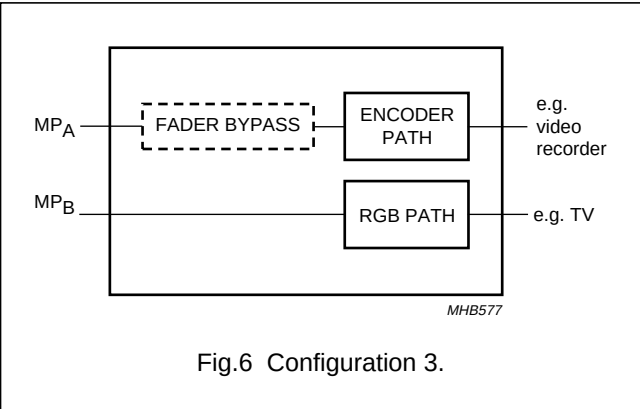
7.1.1.2 Configuration 2

Input MP<sub>A</sub> can be faded into MP<sub>B</sub>. The resulting output of the fader is then encoded to RGB output, while the signal coming from MP<sub>B</sub> is fed directly to composite (and S-video) output (RGBIN = 1, ENCIN = 0). Also in this example, either MP<sub>A</sub> or MP<sub>B</sub> could be an overlay (menu) signal to be faded smoothly in and out, whereas the overlay appears only in the RGB output connected to the TV set.



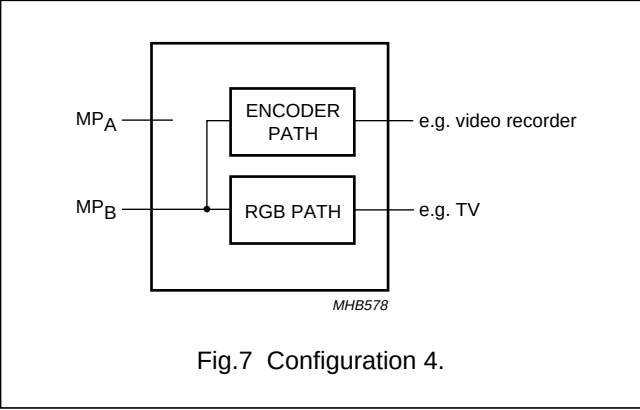
7.1.1.3 Configuration 3

Input MP<sub>B</sub> is passed directly to the RGB output, assuming e.g. it contains video including overlay. MP<sub>A</sub> is equivalently passed through the inactive fader to the composite (and S-video) output, assuming e.g. it contains video excluding overlay (RGBIN = 0, ENCIN = 1).



7.1.1.4 Configuration 4

Only MP<sub>B</sub> input is in use; its signal appears both composite (and S-video) and RGB encoded (RGBIN = ENCIN = 0).



## Digital video encoder

## SAF7129AH

### 7.1.2 PARAMETERS OF THE FADER

Basically, there are three independent fade factors available, allowing for the equation:

$$\text{Output} = (\text{FADEx} \times \text{In1}) + [(1 - \text{FADEx}) \times \text{In2}]$$

Where x = 1, 2 or 3

Factor FADE1 is effective, when a colour in the data stream fed to the MPEG port fader input is recognized as being between KEY1L and KEY1U. That means, the colour is not identified by a single numeric value, but an upper and lower threshold in which a 24-bit YUV colour space can be defined. FADE1 = 00H results in 100% signal at the MPEG port fader input and 0% signal at the fader Video port input. Variation of 63 steps is possible up to FADE1 = 3FH, resulting in 0% signal at the MPEG port fader input and 100% signal at the fader Video port input.

Factor FADE2 is effective, when a colour in the data stream fed to the MPEG port fader input is recognized as being between KEY2L and KEY2U. FADE2 is to be seen in conjunction with a colour that is defined by a 24-bit internal Colour Look-Up Table (CLUT). FADE2 = 00H results in 100% of the internally defined LUT colour and 0% signal at the fader Video port input. Variation of 63 steps is possible up to FADE2 = 3FH, resulting in 0% of the internally defined LUT colour and 100% signal at the fader Video port input.

Finally, factor FADE3 is effective when a colour in the data stream fed to the MPEG port fader input is recognized as neither being between KEY1L and KEY1U nor being between KEY2L and KEY2U. FADE3 = 00H results in 100% signal at the MPEG port fader input and 0% signal at the fader Video port input. Variation of 63 steps is possible up to FADE3 = 3FH, resulting in 0% signal at the MPEG port fader input and 100% signal at the fader Video port input.

Optionally, all upper and lower thresholds can be ignored, enabling to fade signals only against the LUT colour.

If bit CFADM is set HIGH, all data at the MPEG port fader are faded against the LUT colour, if bit CFADV is set HIGH, all data at the Video port fader are faded against the LUT colour.

### 7.2 Data manager

In the data manager, alternatively to the external video data, a pre-defined colour look-up table located in this block can be read out in a pre-defined sequence (8 steps per active video line), achieving a colour bar test pattern generator without the need for an external data source.

### 7.3 Encoder

#### 7.3.1 VIDEO PATH

The encoder generates out of Y, U and V baseband signals luminance and colour subcarrier output signals, suitable for use as CVBS or separate Y and C signals.

Luminance is modified in gain and in offset (latter programmable in a certain range to enable different black level set-ups). A blanking level can be set after insertion of a fixed synchronization pulse tip level in accordance with standard composite synchronization schemes.

In order to enable easy analog post filtering, luminance is interpolated from a 13.5 MHz data rate to a 27 MHz data rate, providing luminance in 10-bit resolution. The transfer characteristics of the luminance interpolation filter are illustrated in Figs 10 and 11. Appropriate transients at start/end of active video and for synchronization pulses are ensured.

Chrominance is modified in gain (programmable separately for U and V), standard dependent burst is inserted, before baseband colour signals are interpolated from a 6.75 MHz data rate to a 27 MHz data rate. One of the interpolation stages can be bypassed, thus providing a higher colour bandwidth, which can be made use of for Y and C output. The transfer characteristics of the chrominance interpolation filter are illustrated in Figs 8 and 9.

The amplitude, beginning and ending of the inserted burst, is programmable in a certain range that is suitable for standard signals and for special effects. Behind the succeeding quadrature modulator, colour in a 10-bit resolution is provided on the subcarrier.

The numeric ratio between Y and C outputs is in accordance with the respective standards.

## Digital video encoder

## SAF7129AH

### 7.3.2 TELETEXT INSERTION AND ENCODING

Pin TTX receives a WST or NABTS teletext bitstream sampled at the LLC clock. Two protocols are provided:

- At each rising edge of output signal (TTXRQ) a single teletext bit has to be provided after a programmable delay at input pin TTX
- The signal TTXRQ performs only a single LOW-to-HIGH transition and remains at HIGH level for 360, 296 or 288 teletext bits, depending on the chosen standard.

Phase variant interpolation is achieved on this bitstream in the internal teletext encoder, providing sufficient small phase jitter on the output text lines.

TTXRQ provides a fully programmable request signal to the teletext source, indicating the insertion period of bitstream at lines which are selectable independently for both fields. The internal insertion window for text is set to 360 (PAL-WST), 296 (NTSC-WST) or 288 (NABTS) teletext bits including clock run-in bits. The protocol and timing are illustrated in Fig.23.

### 7.3.3 VIDEO PROGRAMMING SYSTEM (VPS) ENCODING

Five bytes of VPS information can be loaded via the I<sup>2</sup>C-bus and will be encoded in the appropriate format into line 16.

### 7.3.4 CLOSED CAPTION ENCODER

Using this circuit, data in accordance with the specification of closed caption or extended data service, delivered by the control interface, can be encoded (line 21). Two dedicated pairs of bytes (two bytes per field), each pair preceded by run-in clocks and framing code, are possible.

The actual line number where data is to be encoded in, can be modified in a certain range.

The data clock frequency is in accordance with the definition for NTSC-M standard 32 times horizontal line frequency.

Data LOW at the output of the DACs corresponds to 0 IRE, data HIGH at the output of the DACs corresponds to approximately 50 IRE.

It is also possible to encode closed caption data for 50 Hz field frequencies at 32 times horizontal line frequency.

### 7.4 RGB processor

This block contains a dematrix in order to produce red, green and blue signals to be fed to a SCART plug.

Before Y, C<sub>B</sub> and C<sub>R</sub> signals are de-matrixed, individual gain adjustment for Y and colour difference signals and 2 times oversampling for luminance and 4 times oversampling for colour difference signals is performed. The transfer curves of luminance and colour difference components of RGB are illustrated in Figs 12 and 13.

### 7.5 SECAM processor

SECAM specific pre-processing is achieved by a pre-emphasis of colour difference signals (for gain and phase see Figs 14 and 15).

A baseband frequency modulator with a reference frequency shifted from 4.286 MHz to DC carries out SECAM modulation in accordance with appropriate standard or optionally wide clipping limits.

After the HF pre-emphasis, also applied on a DC reference carrier (anti-Cloche filter; see Figs 16 and 17), line-by-line sequential carriers with black reference of 4.25 MHz (Db) and 4.40625 MHz (Dr) are generated using specified values for FSC programming bytes.

Alternating phase reset in accordance with SECAM standard is carried out automatically. During vertical blanking, the so-called "bottle pulses" are not provided.

### 7.6 Output interface/DACs

In the output interface, encoded Y and C signals are converted from digital-to-analog in a 10-bit resolution. Y and C signals are also combined to a 10-bit CVBS signal.

The CVBS output occurs with the same processing delay (equal to 82 LLC clock periods, measured from MP input to the analog outputs) as the Y, C and RGB outputs. Absolute amplitude at the input of the DAC for CVBS is reduced by  $15\frac{1}{16}$  with respect to Y and C DACs to make maximum use of conversion ranges.

Red, green and blue signals are also converted from digital-to-analog, each providing a 9-bit resolution.

Outputs of the DACs can be set together via software control to minimum output voltage (approximately 0.2 V DC) for either purpose. Alternatively, the buffers can be switched into 3-state output condition; this allows for a 'wired AND' configuration with other 3-state outputs and can also be used as a power-save mode.

## Digital video encoder

## SAF7129AH

### 7.7 Synchronization

The synchronization of the SAF7129AH is able to operate in two modes; slave mode and master mode.

In master mode (see Fig.19), the circuit generates all necessary timings in the video signal itself, and it can provide timing signals at the RCV1 and RCV2 ports. In slave mode, it accepts timing information either from the RCV pins or from the embedded timing data of the ITU-R BT.656 data stream.

For the SAF7129AH, the only difference between master and slave mode is that it ignores the timing information at its inputs in master mode. Thus, if in slave mode, any timing information is missing, the IC will continue running free without a visible effect. But there must not be any additional pulses (with wrong phase) because the circuit will not ignore them.

In slave mode (see Fig.18), an interface circuit decides, which signal is expected at the RCV1 port and which information is taken from its active slope. The polarity can be chosen. If PRCV1 is logic 0, the rising slope will be active.

The signal can be:

- A Vertical Sync (VS) pulse; the active slope sets the vertical phase
- An odd/even signal; the active slope sets the vertical phase, the internal field flag to odd and optionally sets the horizontal phase
- A Field Sequence (FSEQ) signal; it marks the first field of the 4 (NTSC), 8 (PAL) respectively 12 (SECAM) field sequences. In addition to the odd/even signal, it also sets the PAL phase and optionally defines the subcarrier phase.

On the RCV2 port, the IC can provide a horizontal pulse with programmable start and stop phase; this pulse can be inhibited in the vertical blanking period to build up, for example, a composite blanking signal.

The horizontal phase can be set via a separate input RCV2. In the event of VS pulses at RCV1, this is mandatory. It is also possible to set the signal path to blank via this input.

From the ITU-R BT.656 data stream, the SAF7129AH decodes only the start of the first line in the odd field. All other information is ignored and may miss. If this kind of slave mode is active, the RCV pins may be switched to output mode.

In slave mode, the horizontal trigger phase can be programmed to any point in the line, the vertical phase from line 0 to line 15 counted from the first serration pulse in half line steps.

Whenever synchronization information cannot be derived directly from the inputs, the SAF7129AH will calculate it from the internal horizontal, vertical and PAL phase. This gives good flexibility with respect to external synchronization, but the circuit does not suppress illegal settings. In such an event, the odd/even information may vanish as it does in the non-interlaced modes.

In master mode, the line lengths are fixed to 1728 clocks at 50 Hz and 1716 clocks at 60 Hz. To allow non-interlaced frames, the field lengths can be varied by  $\pm 0.5$  lines. In the event of non-interlace, the SAF7129AH does not provide odd/even information and the output signal does not contain the PAL 'Bruch sequence'.

At the RCV1 pin the IC can provide:

- A Vertical Sync (VS) signal with 2.5 (50 Hz) or 3 (60 Hz) lines duration
- An odd/even signal which is LOW in odd fields
- A Field Sequence (FSEQ) signal which is HIGH in the first field of the 4, 8 respectively 12 field sequences.

At the RCV2 pin, there is a horizontal pulse of programmable phase and duration available. This pulse can be suppressed in the programmable inactive part of a field, giving a composite blanking signal.

The directions and polarities of the RCV ports can be chosen independently. Timing references can be found in Tables 52 and 60.

### 7.8 Clock

The input to LLC1 can either be an external clock source or the buffered on-chip clock XCLK. The internal crystal oscillator can be run with either a 3rd-harmonic or a fundamental crystal frequency.

### 7.9 I<sup>2</sup>C-bus interface

The I<sup>2</sup>C-bus interface is a standard slave transceiver, supporting 7-bit slave addresses and 400 kbits/s guaranteed transfer rate. It uses 8-bit subaddressing with an auto-increment function. All registers are write and readable, except one read only status byte.

The I<sup>2</sup>C-bus slave address is defined as 88H with pin 21 (SA) tied LOW and as 8CH with pin 21 (SA) tied HIGH.

## Digital video encoder

## SAF7129AH

**7.10 Input levels and formats**

The SAF7129AH expects digital Y, C<sub>B</sub> and C<sub>R</sub> data with levels (digital codes) in accordance with "ITU-R BT.601".

For C and CVBS outputs, deviating amplitudes of the colour difference signals can be compensated by independent gain control setting, while gain for luminance is set to predefined values, distinguishable for 7.5 IRE set-up or without set-up.

The RGB, respectively C<sub>R</sub>-Y-C<sub>B</sub> path features a gain setting individually for luminance (GY) and colour difference signals (GCD).

Reference levels are measured with a colour bar, 100% white, 100% amplitude and 100% saturation.

**Table 1** "ITU-R BT.601" signal component levels

| COLOUR  | SIGNALS <sup>(1)</sup> |                |                |                  |                  |                  |
|---------|------------------------|----------------|----------------|------------------|------------------|------------------|
|         | Y                      | C <sub>B</sub> | C <sub>R</sub> | R <sup>(2)</sup> | G <sup>(2)</sup> | B <sup>(2)</sup> |
| White   | 235                    | 128            | 128            | 235              | 235              | 235              |
| Yellow  | 210                    | 16             | 146            | 235              | 235              | 16               |
| Cyan    | 170                    | 166            | 16             | 16               | 235              | 235              |
| Green   | 145                    | 54             | 34             | 16               | 235              | 16               |
| Magenta | 106                    | 202            | 222            | 235              | 16               | 235              |
| Red     | 81                     | 90             | 240            | 235              | 16               | 16               |
| Blue    | 41                     | 240            | 110            | 16               | 16               | 235              |
| Black   | 16                     | 128            | 128            | 16               | 16               | 16               |

**Notes**

1. Transformation:

- a)  $R = Y + 1.3707 \times (C_R - 128)$
- b)  $G = Y - 0.3365 \times (C_B - 128) - 0.6982 \times (C_R - 128)$
- c)  $B = Y + 1.7324 \times (C_B - 128)$ .

2. Representation of R, G and B (or C<sub>R</sub>, Y and C<sub>B</sub>) at the output is 9 bits at 27 MHz.

**Table 2** 8-bit multiplexed format (similar to "ITU-R BT.601")

| TIME                   | BITS             |    |                  |    |                  |    |                  |    |
|------------------------|------------------|----|------------------|----|------------------|----|------------------|----|
|                        | 0                | 1  | 2                | 3  | 4                | 5  | 6                | 7  |
| Sample                 | C <sub>B</sub> 0 | Y0 | C <sub>R</sub> 0 | Y1 | C <sub>B</sub> 2 | Y2 | C <sub>R</sub> 2 | Y3 |
| Luminance pixel number | 0                |    | 1                |    | 2                |    | 3                |    |
| Colour pixel number    | 0                |    |                  |    | 2                |    |                  |    |

## Digital video encoder

SAF7129AH

## 7.11 Bit allocation map

**Table 3** Slave receiver (slave address 88H)

| REGISTER FUNCTION               | SUBADDR    | DATA BYTE <sup>(1)</sup> |         |         |         |         |         |         |         |
|---------------------------------|------------|--------------------------|---------|---------|---------|---------|---------|---------|---------|
|                                 |            | D7                       | D6      | D5      | D4      | D3      | D2      | D1      | D0      |
| Status byte (read only)         | 00H        | VER2                     | VER1    | VER0    | CCRDO   | CCRDE   | 0       | FSEQ    | O_E     |
| Null                            | 01H to 25H | 0                        | 0       | 0       | 0       | 0       | 0       | 0       | 0       |
| Wide screen signal              | 26H        | WSS7                     | WSS6    | WSS5    | WSS4    | WSS3    | WSS2    | WSS1    | WSS0    |
| Wide screen signal              | 27H        | WSSON                    | 0       | WSS13   | WSS12   | WSS11   | WSS10   | WSS9    | WSS8    |
| Real-time control, burst start  | 28H        | DECCOL                   | DECFIS  | BS5     | BS4     | BS3     | BS2     | BS1     | BS0     |
| Burst end                       | 29H        | 0                        | 0       | BE5     | BE4     | BE3     | BE2     | BE1     | BE0     |
| Copy generation 0               | 2AH        | CG07                     | CG06    | CG05    | CG04    | CG03    | CG02    | CG01    | CG00    |
| Copy generation 1               | 2BH        | CG15                     | CG14    | CG13    | CG12    | CG11    | CG10    | CG09    | CG08    |
| CG enable, copy generation 2    | 2CH        | CGEN                     | 0       | 0       | 0       | CG19    | CG18    | CG17    | CG16    |
| Output port control             | 2DH        | CVBSEN1                  | CVBSEN0 | CVBSTRI | YTRI    | CTRI    | RTRI    | GTRI    | BTRI    |
| Null                            | 2EH to 37H | 0                        | 0       | 0       | 0       | 0       | 0       | 0       | 0       |
| Gain luminance for RGB          | 38H        | 0                        | 0       | 0       | GY4     | GY3     | GY2     | GY1     | GY0     |
| Gain colour difference for RGB  | 39H        | 0                        | 0       | 0       | GCD4    | GCD3    | GCD2    | GCD1    | GCD0    |
| Input port control 1            | 3AH        | CBENB                    | 0       | 0       | SYMP    | DEMOFF  | CSYNC   | MP2C    | VP2C    |
| Key colour 1 lower limit U      | 42H        | KEY1LU7                  | KEY1LU6 | KEY1LU5 | KEY1LU4 | KEY1LU3 | KEY1LU2 | KEY1LU1 | KEY1LU0 |
| Key colour 1 lower limit V      | 43H        | KEY1LV7                  | KEY1LV6 | KEY1LV5 | KEY1LV4 | KEY1LV3 | KEY1LV2 | KEY1LV1 | KEY1LV0 |
| Key colour 1 lower limit Y      | 44H        | KEY1LY7                  | KEY1LY6 | KEY1LY5 | KEY1LY4 | KEY1LY3 | KEY1LY2 | KEY1LY1 | KEY1LY0 |
| Key colour 2 lower limit U      | 45H        | KEY2LU7                  | KEY2LU6 | KEY2LU5 | KEY2LU4 | KEY2LU3 | KEY2LU2 | KEY2LU1 | KEY2LU0 |
| Key colour 2 lower limit V      | 46H        | KEY2LV7                  | KEY2LV6 | KEY2LV5 | KEY2LV4 | KEY2LV3 | KEY2LV2 | KEY2LV1 | KEY2LV0 |
| Key colour 2 lower limit Y      | 47H        | KEY2LY7                  | KEY2LY6 | KEY2LY5 | KEY2LY4 | KEY2LY3 | KEY2LY2 | KEY2LY1 | KEY2LY0 |
| Key colour 1 upper limit U      | 48H        | KEY1UU7                  | KEY1UU6 | KEY1UU5 | KEY1UU4 | KEY1UU3 | KEY1UU2 | KEY1UU1 | KEY1UU0 |
| Key colour 1 upper limit V      | 49H        | KEY1UV7                  | KEY1UV6 | KEY1UV5 | KEY1UV4 | KEY1UV3 | KEY1UV2 | KEY1UV1 | KEY1UV0 |
| Key colour 1 upper limit Y      | 4AH        | KEY1UY7                  | KEY1UY6 | KEY1UY5 | KEY1UY4 | KEY1UY3 | KEY1UY2 | KEY1UY1 | KEY1UY0 |
| Key colour 2 upper limit U      | 4BH        | KEY2UU7                  | KEY2UU6 | KEY2UU5 | KEY2UU4 | KEY2UU3 | KEY2UU2 | KEY2UU1 | KEY2UU0 |
| Key colour 2 upper limit V      | 4CH        | KEY2UV7                  | KEY2UV6 | KEY2UV5 | KEY2UV4 | KEY2UV3 | KEY2UV2 | KEY2UV1 | KEY2UV0 |
| Key colour 2 upper limit Y      | 4DH        | KEY2UY7                  | KEY2UY6 | KEY2UY5 | KEY2UY4 | KEY2UY3 | KEY2UY2 | KEY2UY1 | KEY2UY0 |
| Fade factor key colour 1        | 4EH        | 0                        | 0       | FADE15  | FADE14  | FADE13  | FADE12  | FADE11  | FADE10  |
| CFade, Fade factor key colour 2 | 4FH        | CFADEM                   | CFADEV  | FADE25  | FADE24  | FADE23  | FADE22  | FADE21  | FADE20  |

## Digital video encoder

SAF7129AH

| REGISTER FUNCTION                             | SUBADDR | DATA BYTE <sup>(1)</sup> |        |        |        |        |        |        |        |
|-----------------------------------------------|---------|--------------------------|--------|--------|--------|--------|--------|--------|--------|
|                                               |         | D7                       | D6     | D5     | D4     | D3     | D2     | D1     | D0     |
| Fade factor other                             | 50H     | 0                        | 0      | FADE35 | FADE34 | FADE33 | FADE32 | FADE31 | FADE30 |
| Look-up table key colour 2 U                  | 51H     | LUTU7                    | LUTU6  | LUTU5  | LUTU4  | LUTU3  | LUTU2  | LUTU1  | LUTU0  |
| Look-up table key colour 2 V                  | 52H     | LUTV7                    | LUTV6  | LUTV5  | LUTV4  | LUTV3  | LUTV2  | LUTV1  | LUTV0  |
| Look-up table key colour 2 Y                  | 53H     | LUTY7                    | LUTY6  | LUTY5  | LUTY4  | LUTY3  | LUTY2  | LUTY1  | LUTY0  |
| VPS enable, input control 2                   | 54H     | VPSEN                    | 0      | ENCIN  | RGBIN  | DELIN  | VPSEL  | EDGE2  | EDGE1  |
| VPS byte 5                                    | 55H     | VPS57                    | VPS56  | VPS55  | VPS54  | VPS53  | VPS52  | VPS51  | VPS50  |
| VPS byte 11                                   | 56H     | VPS117                   | VPS116 | VPS115 | VPS114 | VPS113 | VPS112 | VPS111 | VPS110 |
| VPS byte 12                                   | 57H     | VPS127                   | VPS126 | VPS125 | VPS124 | VPS123 | VPS122 | VPS121 | VPS120 |
| VPS byte 13                                   | 58H     | VPS137                   | VPS136 | VPS135 | VPS134 | VPS133 | VPS132 | VPS131 | VPS130 |
| VPS byte 14                                   | 59H     | VPS147                   | VPS146 | VPS145 | VPS144 | VPS143 | VPS142 | VPS141 | VPS140 |
| Chrominance phase                             | 5AH     | CHPS7                    | CHPS6  | CHPS5  | CHPS4  | CHPS3  | CHPS2  | CHPS1  | CHPS0  |
| Gain U                                        | 5BH     | GAINU7                   | GAINU6 | GAINU5 | GAINU4 | GAINU3 | GAINU2 | GAINU1 | GAINU0 |
| Gain V                                        | 5CH     | GAINV7                   | GAINV6 | GAINV5 | GAINV4 | GAINV3 | GAINV2 | GAINV1 | GAINV0 |
| Gain U MSB, real-time control, black level    | 5DH     | GAINU8                   | DECOE  | BLCKL5 | BLCKL4 | BLCKL3 | BLCKL2 | BLCKL1 | BLCKL0 |
| Gain V MSB, real-time control, blanking level | 5EH     | GAINV8                   | DECPH  | BLNNL5 | BLNNL4 | BLNNL3 | BLNNL2 | BLNNL1 | BLNNL0 |
| CCR, blanking level VBI                       | 5FH     | CCRS1                    | CCRS0  | BLNVB5 | BLNVB4 | BLNVB3 | BLNVB2 | BLNVB1 | BLNVB0 |
| Null                                          | 60H     | 0                        | 0      | 0      | 0      | 0      | 0      | 0      | 0      |
| Standard control                              | 61H     | DOWNB                    | DOWNA  | INPI   | YGS    | SECAM  | SCBW   | PAL    | FISE   |
| RTC enable, burst amplitude                   | 62H     | RTCE                     | BSTA6  | BSTA5  | BSTA4  | BSTA3  | BSTA2  | BSTA1  | BSTA0  |
| Subcarrier 0                                  | 63H     | FSC07                    | FSC06  | FSC05  | FSC04  | FSC03  | FSC02  | FSC01  | FSC00  |
| Subcarrier 1                                  | 64H     | FSC15                    | FSC14  | FSC13  | FSC12  | FSC11  | FSC10  | FSC09  | FSC08  |
| Subcarrier 2                                  | 65H     | FSC23                    | FSC22  | FSC21  | FSC20  | FSC19  | FSC18  | FSC17  | FSC16  |
| Subcarrier 3                                  | 66H     | FSC31                    | FSC30  | FSC29  | FSC28  | FSC27  | FSC26  | FSC25  | FSC24  |
| Line 21 odd 0                                 | 67H     | L21O07                   | L21O06 | L21O05 | L21O04 | L21O03 | L21O02 | L21O01 | L21O00 |
| Line 21 odd 1                                 | 68H     | L21O17                   | L21O16 | L21O15 | L21O14 | L21O13 | L21O12 | L21O11 | L21O10 |
| Line 21 even 0                                | 69H     | L21E07                   | L21E06 | L21E05 | L21E04 | L21E03 | L21E02 | L21E01 | L21E00 |
| Line 21 even 1                                | 6AH     | L21E17                   | L21E16 | L21E15 | L21E14 | L21E13 | L21E12 | L21E11 | L21E10 |
| RCV port control                              | 6BH     | SRCV11                   | SRCV10 | TRCV2  | ORCV1  | PRCV1  | CBLF   | ORCV2  | PRCV2  |
| Trigger control                               | 6CH     | HTRIG7                   | HTRIG6 | HTRIG5 | HTRIG4 | HTRIG3 | HTRIG2 | HTRIG1 | HTRIG0 |

## Digital video encoder

SAF7129AH

| REGISTER FUNCTION               | SUBADDR | DATA BYTE <sup>(1)</sup> |         |         |         |         |         |         |         |
|---------------------------------|---------|--------------------------|---------|---------|---------|---------|---------|---------|---------|
|                                 |         | D7                       | D6      | D5      | D4      | D3      | D2      | D1      | D0      |
| Trigger control                 | 6DH     | HTRIG10                  | HTRIG9  | HTRIG8  | VTRIG4  | VTRIG3  | VTRIG2  | VTRIG1  | VTRIG0  |
| Multi control                   | 6EH     | SBLBN                    | BLCKON  | PHRES1  | PHRES0  | LDEL1   | LDEL0   | FLC1    | FLC0    |
| Closed caption, teletext enable | 6FH     | CCEN1                    | CCEN0   | TTXEN   | SCCLN4  | SCCLN3  | SCCLN2  | SCCLN1  | SCCLN0  |
| RCV2 output start               | 70H     | RCV2S7                   | RCV2S6  | RCV2S5  | RCV2S4  | RCV2S3  | RCV2S2  | RCV2S1  | RCV2S0  |
| RCV2 output end                 | 71H     | RCV2E7                   | RCV2E6  | RCV2E5  | RCV2E4  | RCV2E3  | RCV2E2  | RCV2E1  | RCV2E0  |
| MSBs RCV2 output                | 72H     | 0                        | RCV2E10 | RCV2E9  | RCV2E8  | 0       | RCV2S10 | RCV2S9  | RCV2S8  |
| TTX request H start             | 73H     | TTXHS7                   | TTXHS6  | TTXHS5  | TTXHS4  | TTXHS3  | TTXHS2  | TTXHS1  | TTXHS0  |
| TTX request H delay             | 74H     | TTXHD7                   | TTXHD6  | TTXHD5  | TTXHD4  | TTXHD3  | TTXHD2  | TTXHD1  | TTXHD0  |
| CSYNC advance, Vsync shift      | 75H     | CSYNCA4                  | CSYNCA3 | CSYNCA2 | CSYNCA1 | CSYNCA0 | VS_S2   | VS_S1   | VS_S0   |
| TTX odd request vertical start  | 76H     | TTXOVS7                  | TTXOVS6 | TTXOVS5 | TTXOVS4 | TTXOVS3 | TTXOVS2 | TTXOVS1 | TTXOVS0 |
| TTX odd request vertical end    | 77H     | TTXOVE7                  | TTXOVE6 | TTXOVE5 | TTXOVE4 | TTXOVE3 | TTXOVE2 | TTXOVE1 | TTXOVE0 |
| TTX even request vertical start | 78H     | TTXEVS7                  | TTXEVS6 | TTXEVS5 | TTXEVS4 | TTXEVS3 | TTXEVS2 | TTXEVS1 | TTXEVS0 |
| TTX even request vertical end   | 79H     | TTXEVE7                  | TTXEVE6 | TTXEVE5 | TTXEVE4 | TTXEVE3 | TTXEVE2 | TTXEVE1 | TTXEVE0 |
| First active line               | 7AH     | FAL7                     | FAL6    | FAL5    | FAL4    | FAL3    | FAL2    | FAL1    | FAL0    |
| Last active line                | 7BH     | LAL7                     | LAL6    | LAL5    | LAL4    | LAL3    | LAL2    | LAL1    | LAL0    |
| TTX mode, MSB vertical          | 7CH     | TTX60                    | LAL8    | TTXO    | FAL8    | TTXEVE8 | TTXOVE8 | TTXEVS8 | TTXOVS8 |
| Null                            | 7DH     | 0                        | 0       | 0       | 0       | 0       | 0       | 0       | 0       |
| Disable TTX line                | 7EH     | LINE12                   | LINE11  | LINE10  | LINE9   | LINE8   | LINE7   | LINE6   | LINE5   |
| Disable TTX line                | 7FH     | LINE20                   | LINE19  | LINE18  | LINE17  | LINE16  | LINE15  | LINE14  | LINE13  |

**Note**

1. All bits labelled '0' are reserved. They must be programmed with logic 0.



## Digital video encoder

## SAF7129AH

7.12 I<sup>2</sup>C-bus format**Table 4** I<sup>2</sup>C-bus address; see Table 5

|   |               |     |            |     |        |     |       |        |     |   |
|---|---------------|-----|------------|-----|--------|-----|-------|--------|-----|---|
| S | SLAVE ADDRESS | ACK | SUBADDRESS | ACK | DATA 0 | ACK | ----- | DATA n | ACK | P |
|---|---------------|-----|------------|-----|--------|-----|-------|--------|-----|---|

**Table 5** Explanation of Table 4

| PART               | DESCRIPTION                         |
|--------------------|-------------------------------------|
| S                  | START condition                     |
| SLAVE ADDRESS      | 1000 100X or 1000 110X; note 1      |
| ACK                | acknowledge, generated by the slave |
| SUBADDRESS; note 2 | subaddress byte                     |
| DATA               | data byte                           |
| -----              | continued data bytes and ACKs       |
| P                  | STOP condition                      |

**Notes**

1. X is the read/write control bit; X = logic 0 is order to write; X = logic 1 is order to read.
2. If more than 1 byte DATA is transmitted, then auto-increment of the subaddress is performed.

## 7.13 Slave receiver

**Table 6** Subaddress 26H

| BIT | SYMBOL | DESCRIPTION                                           |
|-----|--------|-------------------------------------------------------|
| 7   | WSS7   | Wide screen signalling bits: enhanced services field. |
| 6   | WSS6   |                                                       |
| 5   | WSS5   |                                                       |
| 4   | WSS4   |                                                       |
| 3   | WSS3   | Wide screen signalling bits: aspect ratio field.      |
| 2   | WSS2   |                                                       |
| 1   | WSS1   |                                                       |
| 0   | WSS0   |                                                       |

**Table 7** Subaddress 27H

| BIT | SYMBOL | DESCRIPTION                                                                                                              |
|-----|--------|--------------------------------------------------------------------------------------------------------------------------|
| 7   | WSSON  | 0 = wide screen signalling output is disabled; default state after reset<br>1 = wide screen signalling output is enabled |
| 6   | –      | This bit is reserved and must be set to logic 0.                                                                         |
| 5   | WSS13  | Wide screen signalling bits: reserved field.                                                                             |
| 4   | WSS12  |                                                                                                                          |
| 3   | WSS11  |                                                                                                                          |
| 2   | WSS10  | Wide screen signalling bits: subtitles field.                                                                            |
| 1   | WSS9   |                                                                                                                          |
| 0   | WSS8   |                                                                                                                          |

## Digital video encoder

## SAF7129AH

**Table 8** Subaddress 28H

| BIT | SYMBOL | DESCRIPTION                                                                                                                                   |
|-----|--------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | DECCOL | 0 = disable colour detection bit of RTCI input<br>1 = enable colour detection bit of RTCI input; bit RTCE must be set to logic 1 (see Fig.22) |
| 6   | DECFIS | 0 = field sequence as FISE in subaddress 61<br>1 = field sequence as FISE bit in RTCI input; bit RTCE must be set to logic 1 (see Fig.22)     |
| 5   | BS5    | starting point of burst in clock cycles<br>PAL: BS[5:0] = 33 (21H); default value after reset<br>NTSC: BS[5:0] = 25 (19H)                     |
| 4   | BS4    |                                                                                                                                               |
| 3   | BS3    |                                                                                                                                               |
| 2   | BS2    |                                                                                                                                               |
| 1   | BS1    |                                                                                                                                               |
| 0   | BS0    |                                                                                                                                               |

**Table 9** Subaddress 29H

| BIT | SYMBOL | DESCRIPTION                                                                                                             |
|-----|--------|-------------------------------------------------------------------------------------------------------------------------|
| 7   | –      | These 2 bits are reserved; each must be set to logic 0.                                                                 |
| 6   | –      |                                                                                                                         |
| 5   | BE5    | ending point of burst in clock cycles<br>PAL: BE[5:0] = 29 (1DH); default value after reset<br>NTSC: BE[5:0] = 29 (1DH) |
| 4   | BE4    |                                                                                                                         |
| 3   | BE3    |                                                                                                                         |
| 2   | BE2    |                                                                                                                         |
| 1   | BE1    |                                                                                                                         |
| 0   | BE0    |                                                                                                                         |

**Table 10** Subaddress 2AH

| BIT    | SYMBOL    | DESCRIPTION                                                                                                                                                                                 |
|--------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7 to 0 | CG[07:00] | LSB of the byte is encoded immediately after run-in, the MSB of the byte has to carry the CRCC bit, in accordance with the definition of copy generation management system encoding format. |

**Table 11** Subaddress 2BH

| BIT    | SYMBOL    | DESCRIPTION                                                                                                                                         |
|--------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 7 to 0 | CG[15:08] | Second byte; the MSB of the byte has to carry the CRCC bit, in accordance with the definition of copy generation management system encoding format. |

## Digital video encoder

## SAF7129AH

Table 12 Subaddress 2CH

| BIT | SYMBOL | DESCRIPTION                                                                                                          |
|-----|--------|----------------------------------------------------------------------------------------------------------------------|
| 7   | CGEN   | 0 = copy generation data output is disabled; default state after reset<br>1 = copy generation data output is enabled |
| 6   | –      | These 3 bits are reserved; each must be set to logic 0.                                                              |
| 5   | –      |                                                                                                                      |
| 4   | –      |                                                                                                                      |
| 3   | CG19   | Remaining bits of copy generation code.                                                                              |
| 2   | CG18   |                                                                                                                      |
| 1   | CG17   |                                                                                                                      |
| 0   | CG16   |                                                                                                                      |

Table 13 Subaddress 2DH

| BIT | SYMBOL  | DESCRIPTION                                                                                                                               |
|-----|---------|-------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | CVBSEN1 | 0 = luminance output signal is switched to Y DAC; default state after reset<br>1 = CVBS output signal is switched to Y DAC                |
| 6   | CVBSEN0 | 0 = chrominance output signal is switched to C DAC; default state after reset<br>1 = CVBS output signal is switched to C DAC              |
| 5   | CVBSTRI | 0 = DAC for CVBS output in 3-state mode (high-impedance)<br>1 = DAC for CVBS output in normal operation mode; default state after reset   |
| 4   | YTRI    | 0 = DAC for Y output in 3-state mode (high-impedance)<br>1 = DAC for Y output in normal operation mode; default state after reset         |
| 3   | CTRI    | 0 = DAC for C output in 3-state mode (high-impedance)<br>1 = DAC for C output in normal operation mode; default state after reset         |
| 2   | RTRI    | 0 = DAC for RED output in 3-state mode (high-impedance)<br>1 = DAC for RED output in normal operation mode; default state after reset     |
| 1   | GTRI    | 0 = DAC for GREEN output in 3-state mode (high-impedance)<br>1 = DAC for GREEN output in normal operation mode; default state after reset |
| 0   | BTRI    | 0 = DAC for BLUE output in 3-state mode (high-impedance)<br>1 = DAC for BLUE output in normal operation mode; default state after reset   |

Table 14 Subaddress 38H

| BIT    | SYMBOL  | DESCRIPTION                                                                                                                                                                     |
|--------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7 to 5 | –       | These 3 bits are reserved; each must be set to logic 0.                                                                                                                         |
| 4 to 0 | GY[4:0] | Gain luminance of RGB ( $C_R$ , Y and $C_B$ ) output, ranging from $(1 - 16/32)$ to $(1 + 15/32)$ . Suggested nominal value = $-6$ (11010b), depending on external application. |

Table 15 Subaddress 39H

| BIT    | SYMBOL   | DESCRIPTION                                                                                                                                                                             |
|--------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7 to 5 | –        | These 3 bits are reserved; each must be set to logic 0.                                                                                                                                 |
| 4 to 0 | GCD[4:0] | Gain colour difference of RGB ( $C_R$ , Y and $C_B$ ) output, ranging from $(1 - 16/32)$ to $(1 + 15/32)$ . Suggested nominal value = $-6$ (11010b), depending on external application. |

## Digital video encoder

## SAF7129AH

**Table 16** Subaddress 3AH

| BIT | SYMBOL | DESCRIPTION                                                                                                                                                                                                  |
|-----|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | CBENB  | 0 = data from input ports is encoded; default state after reset<br>1 = colour bar with fixed colours is encoded                                                                                              |
| 6   | –      | These 2 bits are reserved; each must be set to a logic 0.                                                                                                                                                    |
| 5   | –      |                                                                                                                                                                                                              |
| 4   | SYMP   | 0 = horizontal and vertical trigger is taken from RCV2 and RCV1 respectively; default state after reset<br>1 = horizontal and vertical trigger is decoded out of "ITU-R BT.656" compatible data at MPEG port |
| 3   | DEMOFF | 0 = $YC_B C_R$ -to-RGB dematrix is active; default state after reset<br>1 = $YC_B C_R$ -to-RGB dematrix is bypassed                                                                                          |
| 2   | CSYNC  | 0 = CVBS output signal is switched to CVBS DAC; default state after reset<br>1 = advanced composite sync is switched to CVBS DAC                                                                             |
| 1   | MP2C   | 0 = input data is twos complement from MPEG port fader input<br>1 = input data is straight binary from MPEG port fader input; default state after reset                                                      |
| 0   | VP2C   | 0 = input data is twos complement from Video port fader input<br>1 = input data is straight binary from Video port fader input; default state after reset                                                    |

**Table 17** Subaddresses 42H to 44H and 48H to 4AH

| ADDRESS    | BYTE             | DESCRIPTION                                                                                                                                                                                                                                                                                    |
|------------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 42H<br>48H | KEY1LU<br>KEY1UU | Key colour 1 lower and upper limits for U, V and Y. If MPEG input signal is within the limits of key colour 1 the incoming signals at the Video port and MPEG port are added together according to the equation:<br>$FADE1 \times \text{video signal} + (1 - FADE1) \times \text{MPEG signal}$ |
| 43H<br>49H | KEY1LV<br>KEY1UV |                                                                                                                                                                                                                                                                                                |
| 44H<br>4AH | KEY1LY<br>KEY1UY | Default value of all bytes after reset = 80H.                                                                                                                                                                                                                                                  |

**Table 18** Subaddresses 45H to 47H and 4BH to 4DH

| ADDRESS    | BYTE             | DESCRIPTION                                                                                                                                                                                                                                                                                   |
|------------|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 45H<br>4BH | KEY2LU<br>KEY2UU | Key colour 2 lower and upper limits for U, V and Y. If MPEG input signal is within the limits of key colour 2 the incoming signals at the Video port and MPEG port are added together according to the equation:<br>$FADE2 \times \text{video signal} + (1 - FADE2) \times \text{LUT values}$ |
| 46H<br>4CH | KEY2LV<br>KEY2UV |                                                                                                                                                                                                                                                                                               |
| 47H<br>4DH | KEY2LY<br>KEY2UY | Default value of all bytes after reset = 80H.                                                                                                                                                                                                                                                 |

## Digital video encoder

## SAF7129AH

**Table 19** Subaddress 4EH

| BIT    | SYMBOL     | DESCRIPTION                                                                                                                                                                                                                                                                                                                  |
|--------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7 to 6 | –          | These 2 bits are reserved; each must be set to logic 0.                                                                                                                                                                                                                                                                      |
| 5 to 0 | FADE1[5:0] | <p>These 6 bits form factor FADE1 which determines the ratio between the MPEG and video input signal in the resulting video data stream if the key colour 1 is detected in the MPEG input signal.</p> <p>FADE1 = 00H: 100% MPEG, 0% video</p> <p>FADE1 = 3FH: 100% video, 0% MPEG; this is the default value after reset</p> |

**Table 20** Subaddress 4FH

| BIT    | SYMBOL     | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                         |
|--------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7      | CFADEM     | <p>0 = fader operates in normal mode; default state after reset</p> <p>1 = the entire video input stream is faded with the colour stored in the LUT (subaddresses 51H to 53H) regardless of the MPEG input signal. The colour keys are disabled.</p>                                                                                                                                |
| 6      | CFADEV     | <p>0 = fader operates in normal mode; default state after reset</p> <p>1 = the entire MPEG input stream is faded with the colour stored in the LUT (subaddresses 51H to 53H) regardless of the video input signal. The colour keys are disabled.</p>                                                                                                                                |
| 5 to 0 | FADE2[5:0] | <p>These 6 bits form factor FADE2 which determines the ratio between the LUT colour values (subaddresses 51H to 53H) and the video input signal in the resulting video data stream if the key colour 2 is detected in the MPEG input signal.</p> <p>FADE2 = 00H: 100% LUT colour, 0% video</p> <p>FADE2 = 3FH: 100% video, 0% LUT colour; this is the default value after reset</p> |

**Table 21** Subaddress 50H

| BIT    | SYMBOL     | DESCRIPTION                                                                                                                                                                                                                                                                                                                                               |
|--------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7 to 6 | –          | These 2 bits are reserved; each must be a logic 0.                                                                                                                                                                                                                                                                                                        |
| 5 to 0 | FADE3[5:0] | <p>These 6 bits form factor FADE3 which determines the ratio between the MPEG and video input signal in the resulting video data stream if neither the key colour 1 nor the key colour 2 is detected in the MPEG input signal.</p> <p>FADE3 = 00H: 100% MPEG, 0% video</p> <p>FADE3 = 3FH: 100% video, 0% MPEG; this is the default value after reset</p> |

## Digital video encoder

## SAF7129AH

**Table 22** Subaddress 51H

| BIT    | SYMBOL    | DESCRIPTION                                                                                                                                         |
|--------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 7 to 0 | LUTU[7:0] | LUT for the colour values inserted in case of key colour 2 U detection in the MPEG input data stream.<br>LUTU[7:0] = 80H; default value after reset |

**Table 23** Subaddress 52H

| BIT    | SYMBOL    | DESCRIPTION                                                                                                                                         |
|--------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 7 to 0 | LUTV[7:0] | LUT for the colour values inserted in case of key colour 2 V detection in the MPEG input data stream.<br>LUTV[7:0] = 80H; default value after reset |

**Table 24** Subaddress 53H

| BIT    | SYMBOL    | DESCRIPTION                                                                                                                                         |
|--------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 7 to 0 | LUTY[7:0] | LUT for the colour values inserted in case of key colour 2 Y detection in the MPEG input data stream.<br>LUTY[7:0] = 80H; default value after reset |

**Table 25** Subaddress 54H

| BIT | SYMBOL | DESCRIPTION                                                                                                                                                                   |
|-----|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | VPSEN  | 0 = video programming system data insertion is disabled; default state after reset<br>1 = video programming system data insertion in line 16 is enabled                       |
| 6   | –      | This bit is not used and should be set to logic 0.                                                                                                                            |
| 5   | ENCIN  | 0 = encoder path is fed with MP <sub>B</sub> input data; fader is bypassed; default state after reset<br>1 = encoder path is fed with output signal of fader; see Section 7.1 |
| 4   | RGBIN  | 0 = RGB path is fed with MP <sub>B</sub> input data; fader is bypassed; default state after reset<br>1 = RGB path is fed with output signal of fader; see Section 7.1         |
| 3   | DELIN  | 0 = not supported in current version; do not use<br>1 = recommended value; default state after reset                                                                          |
| 2   | VPSEL  | 0 = not supported in current version; do not use<br>1 = recommended value; default state after reset                                                                          |
| 1   | EDGE2  | 0 = MP <sub>B</sub> data is sampled on the rising clock edge; default state after reset<br>1 = MP <sub>B</sub> data is sampled on the falling clock edge                      |
| 0   | EDGE1  | 0 = MP <sub>A</sub> data is sampled on the rising clock edge; default state after reset<br>1 = MP <sub>A</sub> data is sampled on the falling clock edge                      |

## Digital video encoder

## SAF7129AH

**Table 26** Subaddress 55H

| BIT    | SYMBOL    | DESCRIPTION                                                        |
|--------|-----------|--------------------------------------------------------------------|
| 7 to 0 | VPS5[7:0] | Fifth byte of video programming system data in line 16; LSB first. |

**Table 27** Subaddress 56H

| BIT    | SYMBOL     | DESCRIPTION                                                           |
|--------|------------|-----------------------------------------------------------------------|
| 7 to 0 | VPS11[7:0] | Eleventh byte of video programming system data in line 16; LSB first. |

**Table 28** Subaddress 57H

| BIT    | SYMBOL     | DESCRIPTION                                                          |
|--------|------------|----------------------------------------------------------------------|
| 7 to 0 | VPS12[7:0] | Twelfth byte of video programming system data in line 16; LSB first. |

**Table 29** Subaddress 58H

| BIT    | SYMBOL     | DESCRIPTION                                                             |
|--------|------------|-------------------------------------------------------------------------|
| 7 to 0 | VPS13[7:0] | Thirteenth byte of video programming system data in line 16; LSB first. |

**Table 30** Subaddress 59H

| BIT    | SYMBOL     | DESCRIPTION                                                             |
|--------|------------|-------------------------------------------------------------------------|
| 7 to 0 | VPS14[7:0] | Fourteenth byte of video programming system data in line 16; LSB first. |

**Table 31** Subaddress 5AH

| BIT    | SYMBOL    | DESCRIPTION                                                                                                                                                                                                                                                                                                  |
|--------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7 to 0 | CHPS[7:0] | Phase of encoded colour subcarrier (including burst) relative to horizontal sync; can be adjusted in steps of 360/256 degrees.<br>0FH = PAL-B/G and data from input ports<br>3AH = PAL-B/G and data from look-up table<br>35H = NTSC-M and data from input ports<br>57H = NTSC-M and data from look-up table |

## Digital video encoder

## SAF7129AH

**Table 32** Subaddress 5BH

| BIT    | SYMBOL     | DESCRIPTION                                                                                                                                                                                                        |
|--------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7 to 0 | GAINU[7:0] | These are the 8 LSBs of the 9-bit code that selects the variable gain for the $C_B$ signal; input representation in accordance with "ITU-R BT.601"; see Table 33. The MSB is held in subaddress 5DH; see Table 36. |

**Table 33** GAINU values

| CONDITIONS <sup>(1)</sup> | ENCODING                                                              |
|---------------------------|-----------------------------------------------------------------------|
| white-to-black = 92.5 IRE | $GAINU = -2.17 \times \text{nominal to } +2.16 \times \text{nominal}$ |
| GAINU[8:0] = 0            | output subcarrier of U contribution = 0                               |
| GAINU[8:0] = 118 (76H)    | output subcarrier of U contribution = nominal                         |
| white-to-black = 100 IRE  | $GAINU = -2.05 \times \text{nominal to } +2.04 \times \text{nominal}$ |
| GAINU[8:0] = 0            | output subcarrier of U contribution = 0                               |
| GAINU[8:0] = 125 (7DH)    | output subcarrier of U contribution = nominal                         |
| GAINU[8:0] = 106 (6AH)    | nominal GAINU for SECAM encoding                                      |

**Note**

1. All IRE values are rounded up.

**Table 34** Subaddress 5CH

| BIT    | SYMBOL     | DESCRIPTION                                                                                                                                                                                                        |
|--------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7 to 0 | GAINV[7:0] | These are the 8 LSBs of the 9-bit code that selects the variable gain for the $C_R$ signal; input representation in accordance with "ITU-R BT.601"; see Table 35. The MSB is held in subaddress 5EH; see Table 38. |

**Table 35** GAINV values

| CONDITIONS <sup>(1)</sup> | ENCODING                                                              |
|---------------------------|-----------------------------------------------------------------------|
| white-to-black = 92.5 IRE | $GAINV = -1.55 \times \text{nominal to } +1.55 \times \text{nominal}$ |
| GAINV[8:0] = 0            | output subcarrier of V contribution = 0                               |
| GAINV[8:0] = 165 (A5H)    | output subcarrier of V contribution = nominal                         |
| white-to-black = 100 IRE  | $GAINV = -1.46 \times \text{nominal to } +1.46 \times \text{nominal}$ |
| GAINV[8:0] = 0            | output subcarrier of V contribution = 0                               |
| GAINV[8:0] = 175 (AFH)    | output subcarrier of V contribution = nominal                         |
| GAINV[8:0] = 129 (81H)    | nominal GAINV for SECAM encoding                                      |

**Note**

1. All IRE values are rounded up.



## Digital video encoder

## SAF7129AH

**Table 36** Subaddress 5DH

| BIT    | SYMBOL     | DESCRIPTION                                                                                                                            |
|--------|------------|----------------------------------------------------------------------------------------------------------------------------------------|
| 7      | GAINU8     | MSB of the 9-bit code that sets the variable gain for the C <sub>B</sub> signal; see Table 32.                                         |
| 6      | DECOE      | real-time control:<br>0 = disable odd/even field control bit from RTCI<br>1 = enable odd/even field control bit from RTCI (see Fig.22) |
| 5 to 0 | BLCKL[5:0] | variable black level; input representation in accordance with "ITU-R BT.601"; see Table 37                                             |

**Table 37** BLCKL values

| CONDITIONS <sup>(1)</sup>       | ENCODING <sup>(1)</sup>             |
|---------------------------------|-------------------------------------|
| white-to-sync = 140 IRE; note 2 | recommended value: BLCKL = 58 (3AH) |
| BLCKL = 0; note 2               | output black level = 29 IRE         |
| BLCKL = 63 (3FH); note 2        | output black level = 49 IRE         |
| white-to-sync = 143 IRE; note 3 | recommended value: BLCKL = 51 (33H) |
| BLCKL = 0; note 3               | output black level = 27 IRE         |
| BLCKL = 63 (3FH); note 3        | output black level = 47 IRE         |

**Notes**

1. All IRE values are rounded up.
2. Output black level/IRE =  $BLCKL \times 2/6.29 + 28.9$ .
3. Output black level/IRE =  $BLCKL \times 2/6.18 + 26.5$ .

**Table 38** Subaddress 5EH

| BIT    | SYMBOL     | DESCRIPTION                                                                                                                            |
|--------|------------|----------------------------------------------------------------------------------------------------------------------------------------|
| 7      | GAINV8     | MSB of the 9-bit code that sets the variable gain for the C <sub>R</sub> signal; see Table 34.                                         |
| 6      | DECPH      | real-time control:<br>0 = disable subcarrier phase reset bit from RTCI<br>1 = enable subcarrier phase reset bit from RTCI (see Fig.22) |
| 5 to 0 | BLNNL[5:0] | variable blanking level; see Table 39                                                                                                  |

## Digital video encoder

## SAF7129AH

**Table 39** BLNNL values

| CONDITIONS <sup>(1)</sup>       | ENCODING <sup>(1)</sup>             |
|---------------------------------|-------------------------------------|
| white-to-sync = 140 IRE; note 2 | recommended value: BLNNL = 46 (2EH) |
| BLNNL = 0; note 2               | output blanking level = 25 IRE      |
| BLNNL = 63 (3FH); note 2        | output blanking level = 45 IRE      |
| white-to-sync = 143 IRE; note 3 | recommended value: BLNNL = 53 (35H) |
| BLNNL = 0; note 3               | output blanking level = 26 IRE      |
| BLNNL = 63 (3FH); note 3        | output blanking level = 46 IRE      |

**Notes**

1. All IRE values are rounded up.
2. Output black level/IRE =  $BLNNL \times 2/6.29 + 25.4$ .
3. Output black level/IRE =  $BLNNL \times 2/6.18 + 25.9$ ; default after reset: 35H.

**Table 40** Subaddress 5FH

| BIT | SYMBOL | DESCRIPTION                                                                                                                 |
|-----|--------|-----------------------------------------------------------------------------------------------------------------------------|
| 7   | CCRS1  | These 2 bits select the cross-colour reduction filter in luminance; see Table 41 and Fig.10.                                |
| 6   | CCRS0  |                                                                                                                             |
| 5   | BLNVB5 | These 6 bits select the variable blanking level during vertical blanking interval is typically identical to value of BLNNL. |
| 4   | BLNVB4 |                                                                                                                             |
| 3   | BLNVB3 |                                                                                                                             |
| 2   | BLNVB2 |                                                                                                                             |
| 1   | BLNVB1 |                                                                                                                             |
| 0   | BLNVB0 |                                                                                                                             |

**Table 41** Selection of cross-colour reduction filter

| CCRS1 | CCRS0 | DESCRIPTION                      |
|-------|-------|----------------------------------|
| 0     | 0     | no cross-colour reduction        |
| 0     | 1     | cross-colour reduction #1 active |
| 1     | 0     | cross-colour reduction #2 active |
| 1     | 1     | cross-colour reduction #3 active |

## Digital video encoder

## SAF7129AH

**Table 42** Subaddress 61H

| BIT | SYMBOL | DESCRIPTION                                                                                                                                                                                                                                                                                                                     |
|-----|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | DOWNB  | 0 = DACs for R, G and B in normal operational mode<br>1 = DACs for R, G and B forced to lowest output voltage; default state after reset                                                                                                                                                                                        |
| 6   | DOWNA  | 0 = DACs for CVBS, Y and C in normal operational mode; default state after reset<br>1 = DACs for CVBS, Y and C forced to lowest output voltage                                                                                                                                                                                  |
| 5   | INPI   | 0 = PAL switch phase is nominal; default state after reset<br>1 = PAL switch phase is inverted compared to nominal if RTC is enabled; see Table 43                                                                                                                                                                              |
| 4   | YGS    | 0 = luminance gain for white – black 100 IRE; default state after reset<br>1 = luminance gain for white – black 92.5 IRE including 7.5 IRE set-up of black                                                                                                                                                                      |
| 3   | SECAM  | 0 = no SECAM encoding; default state after reset<br>1 = SECAM encoding activated; bit PAL has to be set to logic 0                                                                                                                                                                                                              |
| 2   | SCBW   | 0 = enlarged bandwidth for chrominance encoding (for overall transfer characteristic of chrominance in baseband representation see Figs 8 and 9)<br>1 = standard bandwidth for chrominance encoding (for overall transfer characteristic of chrominance in baseband representation see Figs 8 and 9); default state after reset |
| 1   | PAL    | 0 = NTSC encoding (non-alternating V component)<br>1 = PAL encoding (alternating V component); default state after reset                                                                                                                                                                                                        |
| 0   | FISE   | 0 = 864 total pixel clocks per line; default state after reset<br>1 = 858 total pixel clocks per line                                                                                                                                                                                                                           |

**Table 43** Subaddress 62H

| BIT    | SYMBOL    | DESCRIPTION                                                                                                                                                                                        |
|--------|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7      | RTCE      | 0 = no real-time control of generated subcarrier frequency; default state after reset<br>1 = real-time control of generated subcarrier frequency through SAF7113 or SAF7118; for timing see Fig.22 |
| 6 to 0 | BSTA[6:0] | amplitude of colour burst; input representation in accordance with "ITU-R BT.601"; see Table 44                                                                                                    |

## Digital video encoder

## SAF7129AH

**Table 44** BSTA values

| CONDITIONS <sup>(1)</sup>                                                                        | ENCODING                                                      |
|--------------------------------------------------------------------------------------------------|---------------------------------------------------------------|
| white-to-black = 92.5 IRE;<br>burst = 40 IRE; NTSC encoding<br>BSTA = 0 to $2.02 \times$ nominal | recommended value: BSTA = 63 (3FH)                            |
| white-to-black = 92.5 IRE;<br>burst = 40 IRE; PAL encoding<br>BSTA = 0 to $2.82 \times$ nominal  | recommended value: BSTA = 45 (2DH)                            |
| white-to-black = 100 IRE;<br>burst = 43 IRE; NTSC encoding<br>BSTA = 0 to $1.90 \times$ nominal  | recommended value: BSTA = 67 (43H)                            |
| white-to-black = 100 IRE;<br>burst = 43 IRE; PAL encoding<br>BSTA = 0 to $3.02 \times$ nominal   | recommended value: BSTA = 47 (2FH); default value after reset |
| fixed burst amplitude with SECAM encoding                                                        |                                                               |

**Note**

1. All IRE values are rounded up.

**Table 45** Subaddresses 63H to 66H

| ADDRESS | BYTE       | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                    |
|---------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 63H     | FSC[07:00] | These 4 bytes are used to program the subcarrier frequency. FSC[31:24] is the most significant byte, FSC[07:00] is the least significant byte.<br>$f_{sc}$ = subcarrier frequency (in multiples of line frequency)<br>$f_{llc}$ = clock frequency (in multiples of line frequency)<br>$FSC = \text{round} \left( \frac{f_{sc}}{f_{llc}} \times 2^{32} \right); \text{ note 1}$ |
| 64H     | FSC[15:08] |                                                                                                                                                                                                                                                                                                                                                                                |
| 65H     | FSC[23:16] |                                                                                                                                                                                                                                                                                                                                                                                |
| 66H     | FSC[31:24] |                                                                                                                                                                                                                                                                                                                                                                                |

**Note**

1. Examples:
  - a) NTSC-M:  $f_{sc} = 227.5$ ,  $f_{llc} = 1716 \rightarrow FSC = 569408543$  (21F07C1FH).
  - b) PAL-B/G:  $f_{sc} = 283.7516$ ,  $f_{llc} = 1728 \rightarrow FSC = 705268427$  (2A098ACBH).
  - c) SECAM:  $f_{sc} = 274.304$ ,  $f_{llc} = 1728 \rightarrow FSC = 681786290$  (28A33BB2H).

## Digital video encoder

## SAF7129AH

**Table 46** Subaddress 67H

| BIT    | SYMBOL      | DESCRIPTION                                                                                                                                                                                                                           |
|--------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7 to 0 | L21O[07:00] | First byte of captioning data, odd field.<br><br>LSB of the byte is encoded immediately after run-in and framing code, the MSB of the byte has to carry the parity bit, in accordance with the definition of line 21 encoding format. |

**Table 47** Subaddress 68H

| BIT    | SYMBOL      | DESCRIPTION                                                                                                                                                      |
|--------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7 to 0 | L21O[17:10] | Second byte of captioning data, odd field.<br><br>The MSB of the byte has to carry the parity bit, in accordance with the definition of line 21 encoding format. |

**Table 48** Subaddress 69H

| BIT    | SYMBOL      | DESCRIPTION                                                                                                                                                                                                                          |
|--------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7 to 0 | L21E[07:00] | First byte of extended data, even field.<br><br>LSB of the byte is encoded immediately after run-in and framing code, the MSB of the byte has to carry the parity bit, in accordance with the definition of line 21 encoding format. |

**Table 49** Subaddress 6AH

| BIT    | SYMBOL      | DESCRIPTION                                                                                                                                                     |
|--------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7 to 0 | L21E[17:10] | Second byte of extended data, even field.<br><br>The MSB of the byte has to carry the parity bit, in accordance with the definition of line 21 encoding format. |

## Digital video encoder

## SAF7129AH

**Table 50** Subaddress 6BH

| BIT | SYMBOL | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | SRCV11 | These 2 bits define signal type on pin RCV1; see Table 51                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 6   | SRCV10 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 5   | TRCV2  | 0 = horizontal synchronization is taken from RCV1 port (at bit SYMP = LOW) or from decoded frame sync of "ITU-R BT.656" input (at bit SYMP = HIGH); default state after reset<br>1 = horizontal synchronization is taken from RCV2 port (at bit SYMP = LOW)                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 4   | ORCV1  | 0 = pin RCV1 is switched to input; default state after reset<br>1 = pin RCV1 is switched to output                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 3   | PRCV1  | 0 = polarity of RCV1 as output is active HIGH, rising edge is taken when input; default state after reset<br>1 = polarity of RCV1 as output is active LOW, falling edge is taken when input                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 2   | CBLF   | When CBLF = 0.<br>If ORCV2 = 1, pin RCV2 provides an HREF signal (horizontal reference pulse that is defined by RCV2S and RCV2E, also during vertical blanking interval); default state after reset.<br>If ORCV2 = 0 and bit SYMP = 0, signal input to RCV2 is used for horizontal synchronization only (if TRCV2 = 1); default state after reset.<br>When CBLF = 1.<br>If ORCV2 = 1, pin RCV2 provides a 'composite-blanking-not' signal, for example a reference pulse that is defined by RCV2S and RCV2E, excluding vertical blanking interval, which is defined by FAL and LAL.<br>If ORCV2 = 0 and bit SYMP = 0, signal input to RCV2 is used for horizontal synchronization (if TRCV2 = 1) and as an internal blanking signal. |
| 1   | ORCV2  | 0 = pin RCV2 is switched to input; default state after reset<br>1 = pin RCV2 is switched to output                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 0   | PRCV2  | 0 = polarity of RCV2 as output is active HIGH, rising edge is taken when input, respectively; default state after reset<br>1 = polarity of RCV2 as output is active LOW, falling edge is taken when input, respectively                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

**Table 51** Selection of the signal type on pin RCV1

| SRCV11 | SRCV10 | RCV1 | FUNCTION                                                                                                        |
|--------|--------|------|-----------------------------------------------------------------------------------------------------------------|
| 0      | 0      | VS   | Vertical Sync each field; default state after reset                                                             |
| 0      | 1      | FS   | Frame Sync (odd/even)                                                                                           |
| 1      | 0      | FSEQ | Field Sequence, vertical sync every fourth field (PAL = 0), eighth field (PAL = 1) or twelfth field (SECAM = 1) |
| 1      | 1      | —    | not applicable                                                                                                  |

## Digital video encoder

## SAF7129AH

**Table 52** Subaddress 6CH

| BIT    | SYMBOL     | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|--------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7 to 0 | HTRIG[7:0] | These are the 8 LSBs of the 11-bit code that sets the horizontal trigger phase related to the signal on RCV1 or RCV2 input. The 3 MSBs are held in subaddress 6DH; see Table 53. Values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed. Increasing HTRIG[10:0] decreases delays of all internally generated timing signals. Reference mark: analog output horizontal sync (leading slope) coincides with active edge of RCV used for triggering at HTRIG[10:0] = 4FH (79). |

**Table 53** Subaddress 6DH

| BIT | SYMBOL  | DESCRIPTION                                                                                                                                                                                                           |
|-----|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | HTRIG10 | These are the 3 MSBs of the horizontal trigger phase code; see Table 52.                                                                                                                                              |
| 6   | HTRIG9  |                                                                                                                                                                                                                       |
| 5   | HTRIG8  |                                                                                                                                                                                                                       |
| 4   | VTRIG4  | Sets the vertical trigger phase related to signal on RCV1 input. Increasing VTRIG decreases delays of all internally generated timing signals, measured in half lines; variation range of VTRIG[4:0] = 0 to 31 (1FH). |
| 3   | VTRIG3  |                                                                                                                                                                                                                       |
| 2   | VTRIG2  |                                                                                                                                                                                                                       |
| 1   | VTRIG1  |                                                                                                                                                                                                                       |
| 0   | VTRIG0  |                                                                                                                                                                                                                       |

**Table 54** Subaddress 6EH

| BIT | SYMBOL | DESCRIPTION                                                                                                                                                                              |
|-----|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | SBLBN  | 0 = vertical blanking is defined by programming of FAL and LAL; default state after reset<br>1 = vertical blanking is forced in accordance with "ITU-R BT.624" (50 Hz) or RS170A (60 Hz) |
| 6   | BLCKON | 0 = encoder in normal operation mode<br>1 = output signal is forced to blanking level; default state after reset                                                                         |
| 5   | PHRES1 | These 2 bits select the phase reset mode of the colour subcarrier generator; see Table 55.                                                                                               |
| 4   | PHRES0 |                                                                                                                                                                                          |
| 3   | LDEL1  | These 2 bits select the delay on luminance path with reference to chrominance path; see Table 56.                                                                                        |
| 2   | LDEL0  |                                                                                                                                                                                          |
| 1   | FLC1   | These 2 bits select field length control; see Table 57.                                                                                                                                  |
| 0   | FLC0   |                                                                                                                                                                                          |

**Table 55** Selection of phase reset mode

| PHRES1 | PHRES0 | DESCRIPTION                                                                                   |
|--------|--------|-----------------------------------------------------------------------------------------------|
| 0      | 0      | no reset or reset via RTCI from SAF7113 or SAF7118 if bit RTCE = 1; default value after reset |
| 0      | 1      | reset every two lines or SECAM specific if bit SECAM = 1                                      |
| 1      | 0      | reset every eight fields                                                                      |
| 1      | 1      | reset every four fields                                                                       |

## Digital video encoder

## SAF7129AH

**Table 56** Selection of luminance path delay

| LDEL1 | LDEL0 | LUMINANCE PATH DELAY                          |
|-------|-------|-----------------------------------------------|
| 0     | 0     | no luminance delay; default value after reset |
| 0     | 1     | 1 LLC luminance delay                         |
| 1     | 0     | 2 LLC luminance delay                         |
| 1     | 1     | 3 LLC luminance delay                         |

**Table 57** Selection of field length control

| FLC1 | FLC0 | DESCRIPTION                                                                                  |
|------|------|----------------------------------------------------------------------------------------------|
| 0    | 0    | interlaced 312.5 lines/field at 50 Hz, 262.5 lines/field at 60 Hz; default value after reset |
| 0    | 1    | non-interlaced 312 lines/field at 50 Hz, 262 lines/field at 60 Hz                            |
| 1    | 0    | non-interlaced 313 lines/field at 50 Hz, 263 lines/field at 60 Hz                            |
| 1    | 1    | non-interlaced 313 lines/field at 50 Hz, 263 lines/field at 60 Hz                            |

**Table 58** Subaddress 6FH

| BIT | SYMBOL | DESCRIPTION                                                                                                                                                                  |
|-----|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | CCEN1  | These 2 bits enable individual line 21 encoding; see Table 59.                                                                                                               |
| 6   | CCEN0  |                                                                                                                                                                              |
| 5   | TTXEN  | 0 = disables teletext insertion; default state after reset<br>1 = enables teletext insertion                                                                                 |
| 4   | SCCLN4 | These 5 bits select the actual line where closed caption or extended data are encoded.<br>line = (SCCLN[4:0] + 4) for M-systems<br>line = (SCCLN[4:0] + 1) for other systems |
| 3   | SCCLN3 |                                                                                                                                                                              |
| 2   | SCCLN2 |                                                                                                                                                                              |
| 1   | SCCLN1 |                                                                                                                                                                              |
| 0   | SCCLN0 |                                                                                                                                                                              |

**Table 59** Selection of line 21 encoding

| CCEN1 | CCEN0 | LINE 21 ENCODING                                |
|-------|-------|-------------------------------------------------|
| 0     | 0     | line 21 encoding off; default value after reset |
| 0     | 1     | enables encoding in field 1 (odd)               |
| 1     | 0     | enables encoding in field 2 (even)              |
| 1     | 1     | enables encoding in both fields                 |

**Table 60** Subaddress 70H

| BIT    | SYMBOL     | DESCRIPTION                                                                                                                                                                                                                                                                                                                                 |
|--------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7 to 0 | RCV2S[7:0] | These are the 8 LSBs of the 11-bit code that determines the start of the output signal on the RCV2 pin; the 3 MSBs of the 11-bit code are held at subaddress 72H; see Table 62. Values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed. Leading sync slope at CVBS output coincides with leading slope of RCV2 out at RCV2S = 49H. |



## Digital video encoder

## SAF7129AH

**Table 61** Subaddress 71H

| BIT    | SYMBOL     | DESCRIPTION                                                                                                                                                                                                                                                                                                                                |
|--------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7 to 0 | RCV2E[7:0] | These are the 8 LSBs of the 11-bit code that determines the end of the output signal on the RCV2 pin; the 3 MSBs of the 11-bit code are held at subaddress 72H; see Table 62. Values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed. Leading sync slope at CVBS output coincides with trailing slope of RCV2 out at RCV2E = 49H. |

**Table 62** Subaddress 72H

| BIT | SYMBOL  | DESCRIPTION                                                        |
|-----|---------|--------------------------------------------------------------------|
| 7   | –       | This bit is reserved and must be set to a logic 0.                 |
| 6   | RCV2E10 | These are the 3 MSBs of end of output signal code; see Table 61.   |
| 5   | RCV2E9  |                                                                    |
| 4   | RCV2E8  |                                                                    |
| 3   | –       | This bit is reserved and must be set to a logic 0.                 |
| 2   | RCV2S10 | These are the 3 MSBs of start of output signal code; see Table 60. |
| 1   | RCV2S9  |                                                                    |
| 0   | RCV2S8  |                                                                    |

**Table 63** Subaddress 73H

| BIT    | SYMBOL     | DESCRIPTION                                                                                  |
|--------|------------|----------------------------------------------------------------------------------------------|
| 7 to 0 | TTXHS[7:0] | Start of signal on pin TTXRQ; see Fig.23.<br>PAL: TTXHS[7:0] = 42H<br>NTSC: TTXHS[7:0] = 54H |

**Table 64** Subaddress 74H

| BIT    | SYMBOL     | DESCRIPTION                                                                                                                         |
|--------|------------|-------------------------------------------------------------------------------------------------------------------------------------|
| 7 to 0 | TTXHD[7:0] | Indicates the delay in clock cycles between rising edge of TTXRQ output and valid data at pin TTX.<br>minimum value: TTXHD[7:0] = 2 |

**Table 65** Subaddress 75H

| BIT | SYMBOL  | DESCRIPTION                                                                                                                                                                                      |
|-----|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | CSYNCA4 | Advanced composite sync against RGB output from 0 to 31 LLC clock periods.                                                                                                                       |
| 6   | CSYNCA3 |                                                                                                                                                                                                  |
| 5   | CSYNCA2 |                                                                                                                                                                                                  |
| 4   | CSYNCA1 |                                                                                                                                                                                                  |
| 3   | CSYNCA0 |                                                                                                                                                                                                  |
| 2   | VS_S2   | Vertical sync shift between RCV1 and RCV2 (switched to output); in master mode it is possible to shift Hsync (RCV2; CBLF = 0) against Vsync (RCV1; SRCV1 = 00).<br>standard value: VS_S[2:0] = 3 |
| 1   | VS_S1   |                                                                                                                                                                                                  |
| 0   | VS_S0   |                                                                                                                                                                                                  |

## Digital video encoder

## SAF7129AH

**Table 66** Subaddress 76H

| BIT    | SYMBOL      | DESCRIPTION                                                                                                                                                                                                                                                       | REMARKS                                  |
|--------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------|
| 7 to 0 | TTXOVS[7:0] | These are the 8 LSBs of the 9-bit code that determines the first line of occurrence of signal on pin TTXRQ in odd field. The MSB is held in subaddress 7CH; see Table 72.<br>line = (TTXOVS[8:0] + 4) for M-systems<br>line = (TTXOVS[8:0] + 1) for other systems | PAL: TTXOVS = 05H;<br>NTSC: TTXOVS = 06H |

**Table 67** Subaddress 77H

| BIT    | SYMBOL      | DESCRIPTION                                                                                                                                                                                                                                                          | REMARKS                                  |
|--------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------|
| 7 to 0 | TTXOVE[7:0] | These are the 8 LSBs of the 9-bit code that determines the last line of occurrence of signal on pin TTXRQ in odd field. The MSB is held in subaddress 7CH; see Table 72.<br>last line = (TTXOVE[8:0] + 3) for M-systems<br>last line = TTXOVE[8:0] for other systems | PAL: TTXOVE = 16H;<br>NTSC: TTXOVE = 10H |

**Table 68** Subaddress 78H

| BIT    | SYMBOL      | DESCRIPTION                                                                                                                                                                                                                                                                    | REMARKS                                  |
|--------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------|
| 7 to 0 | TTXEVS[7:0] | These are the 8 LSBs of the 9-bit code that determines the first line of occurrence of signal on pin TTXRQ in even field. The MSB is held in subaddress 7CH; see Table 72.<br>first line = (TTXEVS[8:0] + 4) for M-systems<br>first line = (TTXEVS[8:0] + 1) for other systems | PAL: TTXEVS = 04H;<br>NTSC: TTXEVS = 05H |

**Table 69** Subaddress 79H

| BIT    | SYMBOL      | DESCRIPTION                                                                                                                                                                                                                                                           | REMARKS                                  |
|--------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------|
| 7 to 0 | TTXEVE[7:0] | These are the 8 LSBs of the 9-bit code that determines the last line of occurrence of signal on pin TTXRQ in even field. The MSB is held in subaddress 7CH; see Table 72.<br>last line = (TTXEVE[8:0] + 3) for M-systems<br>last line = TTXEVE[8:0] for other systems | PAL: TTXEVE = 16H;<br>NTSC: TTXEVE = 10H |

**Table 70** Subaddress 7AH

| BIT    | SYMBOL   | DESCRIPTION                                                                                                                                                                                                                                                                                                   |
|--------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7 to 0 | FAL[7:0] | These are the 8 LSBs of the 9-bit code that determines the first active line. The MSB is held in subaddress 7CH; see Table 72. FAL[8:0] = 0 coincides with the first field synchronization pulse.<br>first active line = (FAL[8:0] + 4) for M-systems<br>first active line = (FAL[8:0] + 1) for other systems |

## Digital video encoder

## SAF7129AH

**Table 71** Subaddress 7BH

| BIT    | SYMBOL   | DESCRIPTION                                                                                                                                                                                                                                                                                          |
|--------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7 to 0 | LAL[7:0] | These are the 8 LSBs of the 9-bit code that determines the last active line. The MSB is held in subaddress 7CH; see Table 72. LAL[8:0] = 0 coincides with the first field synchronization pulse.<br>last active line = (LAL[8:0] + 3) for M-systems<br>last active line = LAL[8:0] for other systems |

**Table 72** Subaddress 7CH

| BIT | SYMBOL  | DESCRIPTION                                                                                                                                                                                                                                                                                                         |
|-----|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | TTX60   | 0 = enables NABTS (FISE = 1) or European teletext (FISE = 0); default state after reset<br>1 = enables World Standard Teletext 60 Hz (FISE = 1)                                                                                                                                                                     |
| 6   | LAL8    | MSB of the last active line code; see Table 71.                                                                                                                                                                                                                                                                     |
| 5   | TTXO    | 0 = new teletext protocol selected: at each rising edge of TTXRQ a single teletext bit is requested (see Fig.23); default state after reset<br>1 = old teletext protocol selected: the encoder provides a window of TTXRQ going HIGH; the length of the window depends on the chosen teletext standard (see Fig.23) |
| 4   | FAL8    | MSB of the first active line code; see Table 70.                                                                                                                                                                                                                                                                    |
| 3   | TTXEVE8 | MSB of the 9-bit code that selects the last line of occurrence of signal on pin TTXRQ in even field; see Table 69.                                                                                                                                                                                                  |
| 2   | TTXOVE8 | MSB of the 9-bit code that selects the last line of occurrence of signal on pin TTXRQ in odd field; see Table 67.                                                                                                                                                                                                   |
| 1   | TTXEVS8 | MSB of the 9-bit code that selects the first line of occurrence of signal on pin TTXRQ in even field; see Table 68.                                                                                                                                                                                                 |
| 0   | TTXOVS8 | MSB of the 9-bit code that selects the first line of occurrence of signal on pin TTXRQ in odd field; see Table 66.                                                                                                                                                                                                  |

**Table 73** Subaddress 7EH

| BIT    | SYMBOL     | DESCRIPTION                                                                                                                                                                                                                                                                 |
|--------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7 to 0 | LINE[12:5] | Individual lines in both fields (PAL counting) can be disabled for insertion of teletext by the respective LINE bits. Disabled line = LINE <sub>enn</sub> (50 Hz field rate). This bit mask is effective only, if the lines are enabled by TTXOVS/TTXOVE and TTXEVS/TTXEVE. |

**Table 74** Subaddress 7FH

| BIT    | SYMBOL      | DESCRIPTION                                                                                                                                                                                                                                                                 |
|--------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7 to 0 | LINE[20:13] | Individual lines in both fields (PAL counting) can be disabled for insertion of teletext by the respective LINE bits. Disabled line = LINE <sub>enn</sub> (50 Hz field rate). This bit mask is effective only, if the lines are enabled by TTXOVS/TTXOVE and TTXEVS/TTXEVE. |

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Digital video encoderSAF7129AH

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**7.14 Slave transmitter**

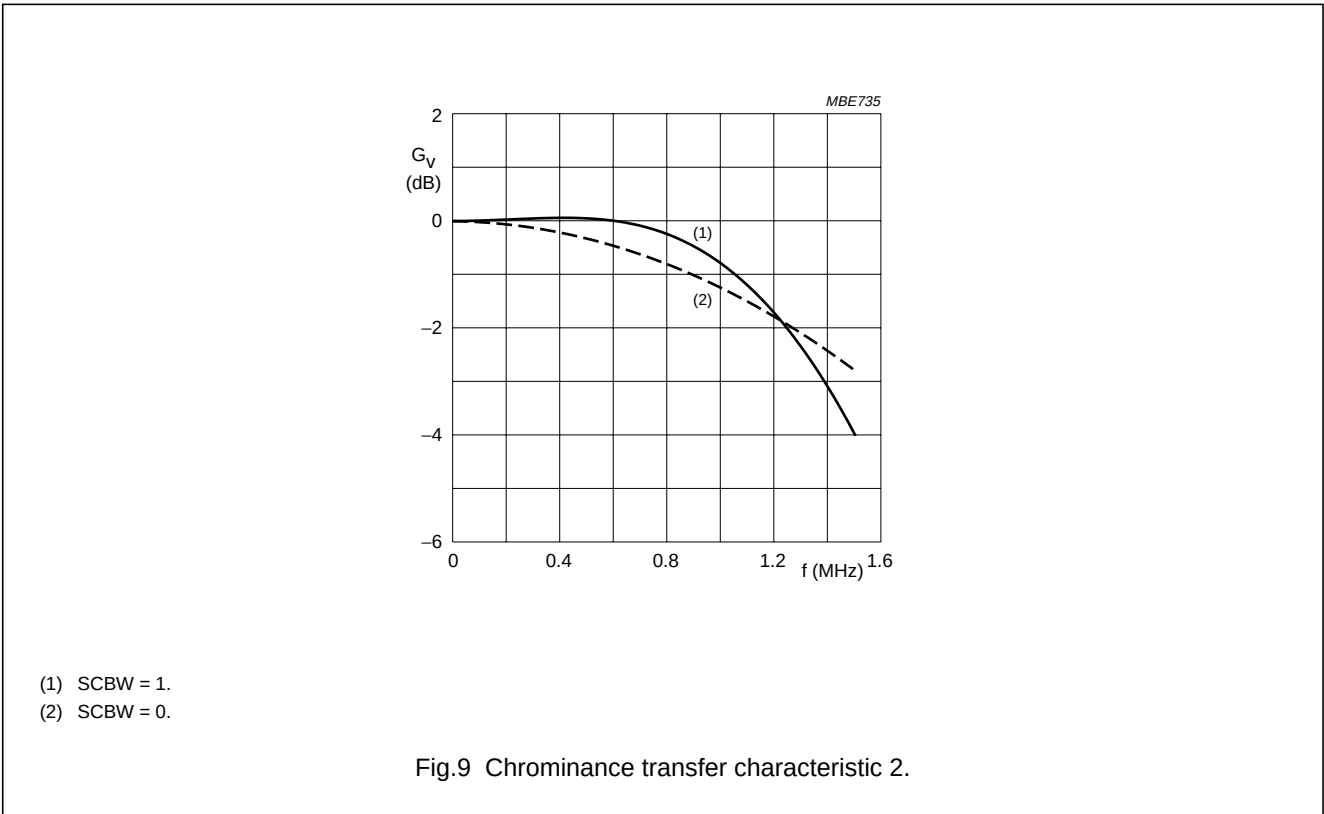
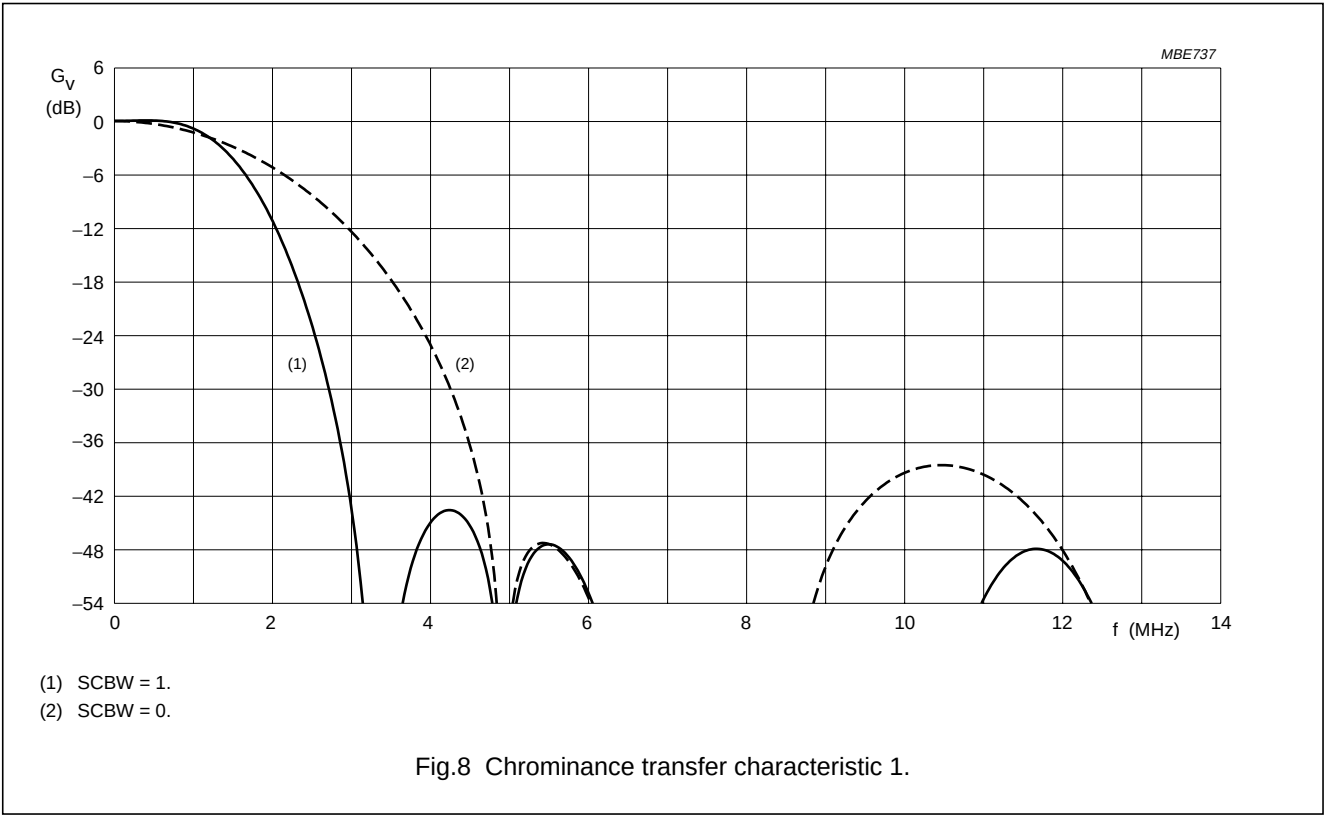
The slave transmitter slave address is 89H.

**Table 75** Subaddress 00H

| BIT | SYMBOL | DESCRIPTION                                                                                                                                                                                                    |
|-----|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | VER2   | These 3 bits form the version identification number of the device: it will be changed with all versions of the IC that have different programming models; current version is 000 binary.                       |
| 6   | VER1   |                                                                                                                                                                                                                |
| 5   | VER0   |                                                                                                                                                                                                                |
| 4   | CCRDO  | 1 = closed caption bytes of the odd field have been encoded<br>0 = the bit is reset after information has been written to the subaddresses 67H and 68H; it is set immediately after the data has been encoded  |
| 3   | CCRDE  | 1 = closed caption bytes of the even field have been encoded<br>0 = the bit is reset after information has been written to the subaddresses 69H and 6AH; it is set immediately after the data has been encoded |
| 2   | –      | not used; set to logic 0                                                                                                                                                                                       |
| 1   | FSEQ   | 1 = during first field of a sequence (repetition rate: NTSC = 4 fields, PAL = 8 fields, SECAM = 12 fields)<br>0 = not first field of a sequence                                                                |
| 0   | O_E    | 1 = during even field<br>0 = during odd field                                                                                                                                                                  |

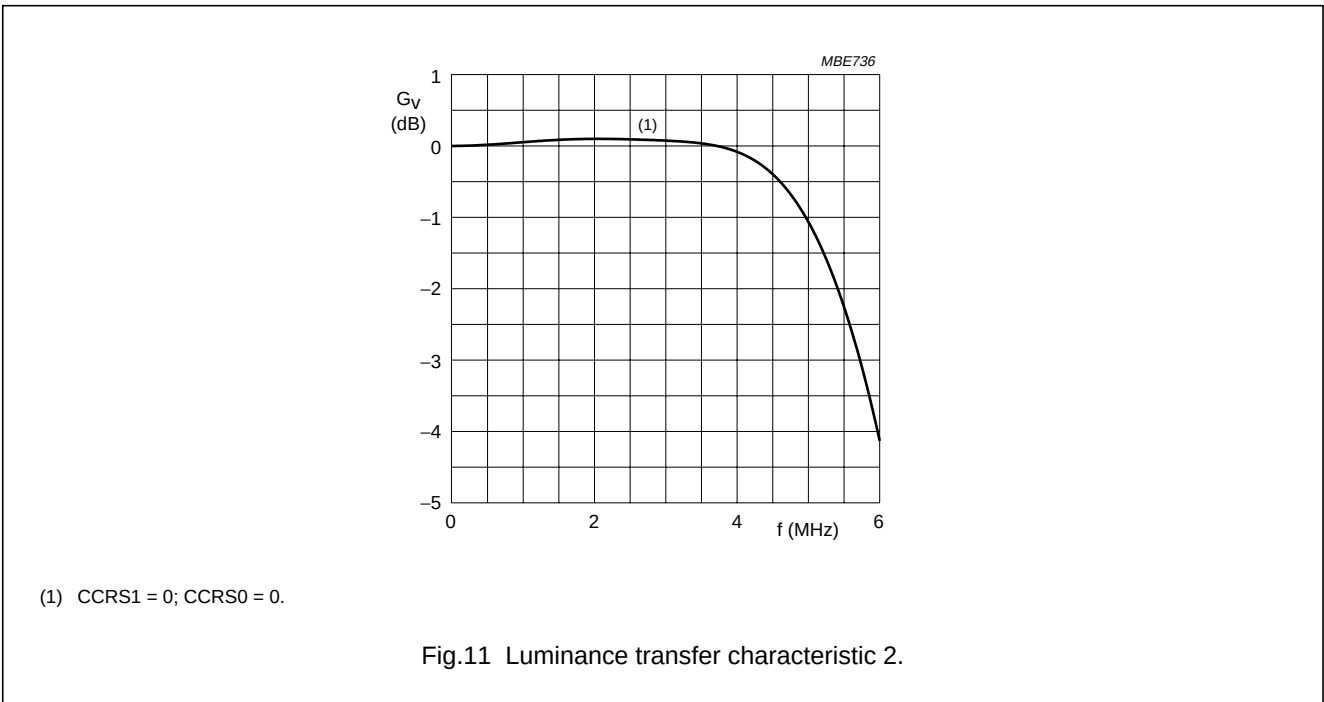
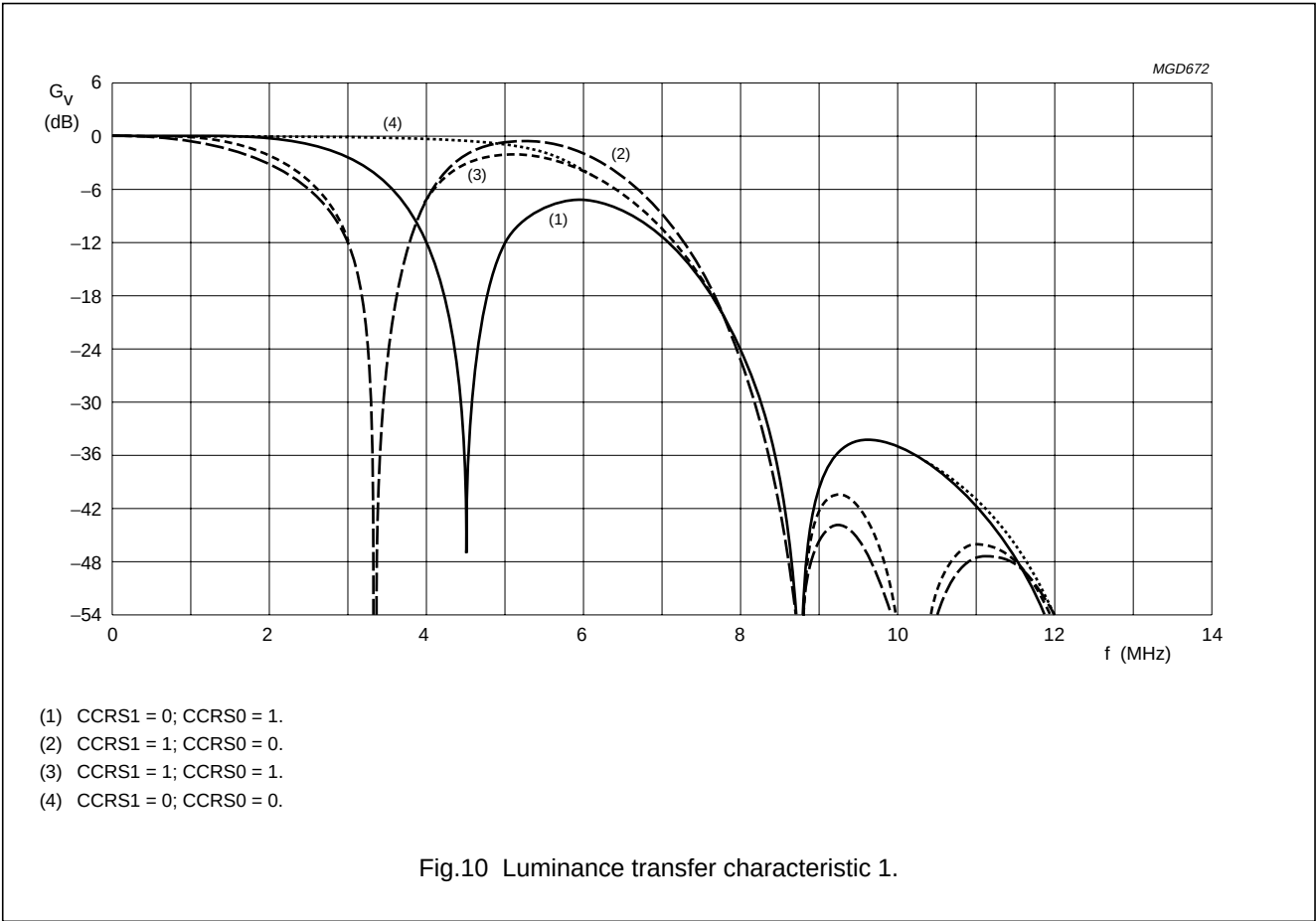
Digital video encoder

SAF7129AH



Digital video encoder

SAF7129AH



Digital video encoder

SAF7129AH

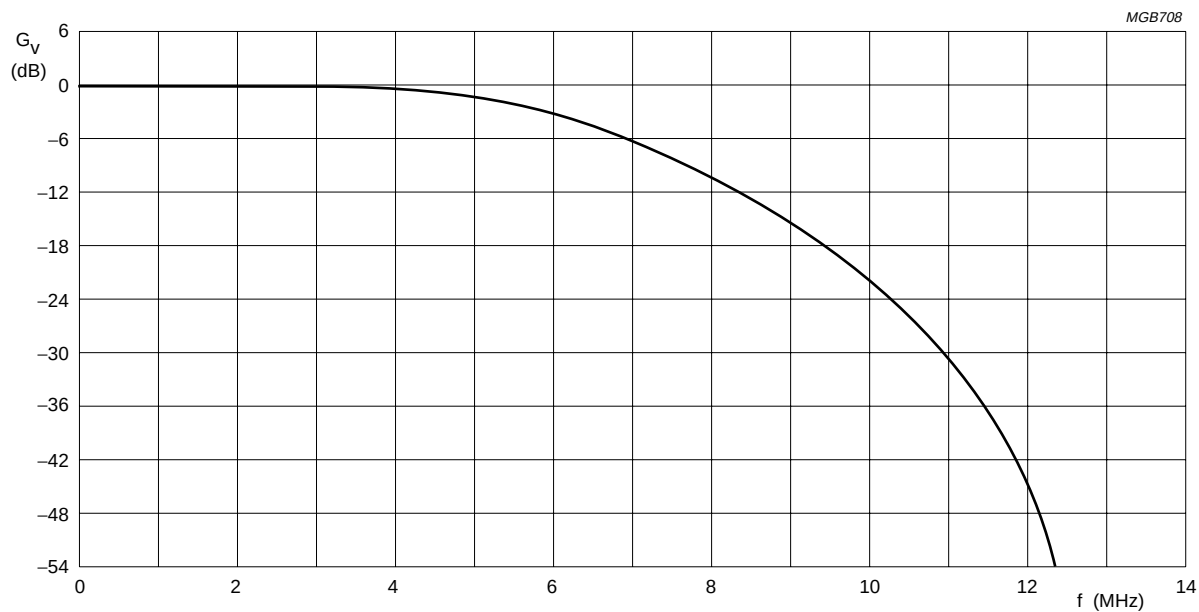


Fig.12 Luminance transfer characteristic in RGB.

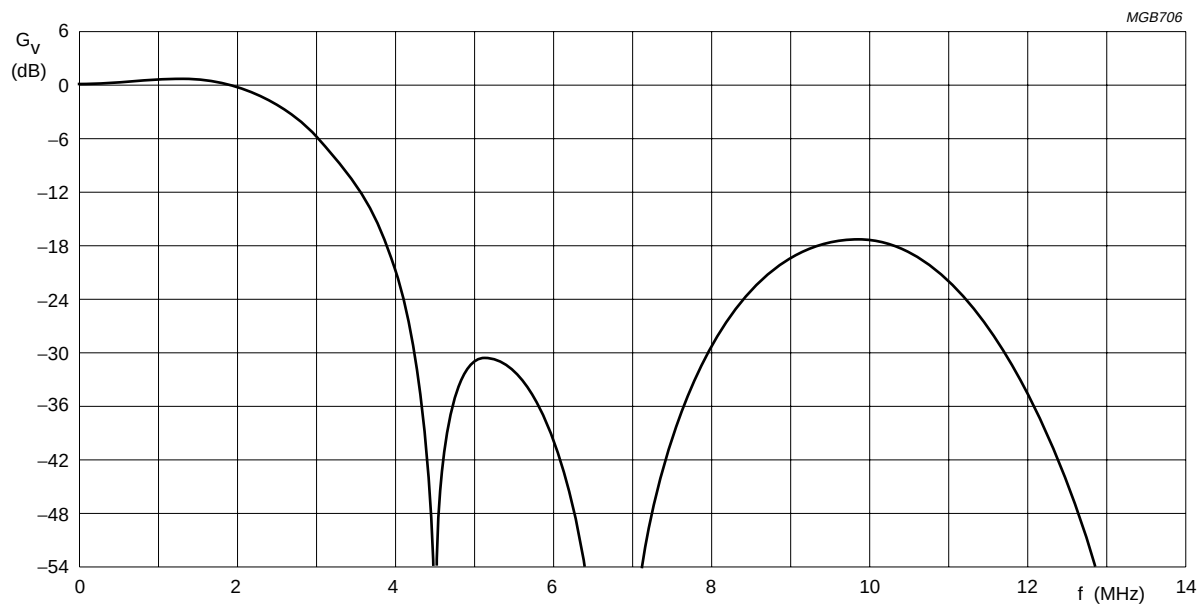


Fig.13 Colour difference transfer characteristic in RGB.

Digital video encoder

SAF7129AH

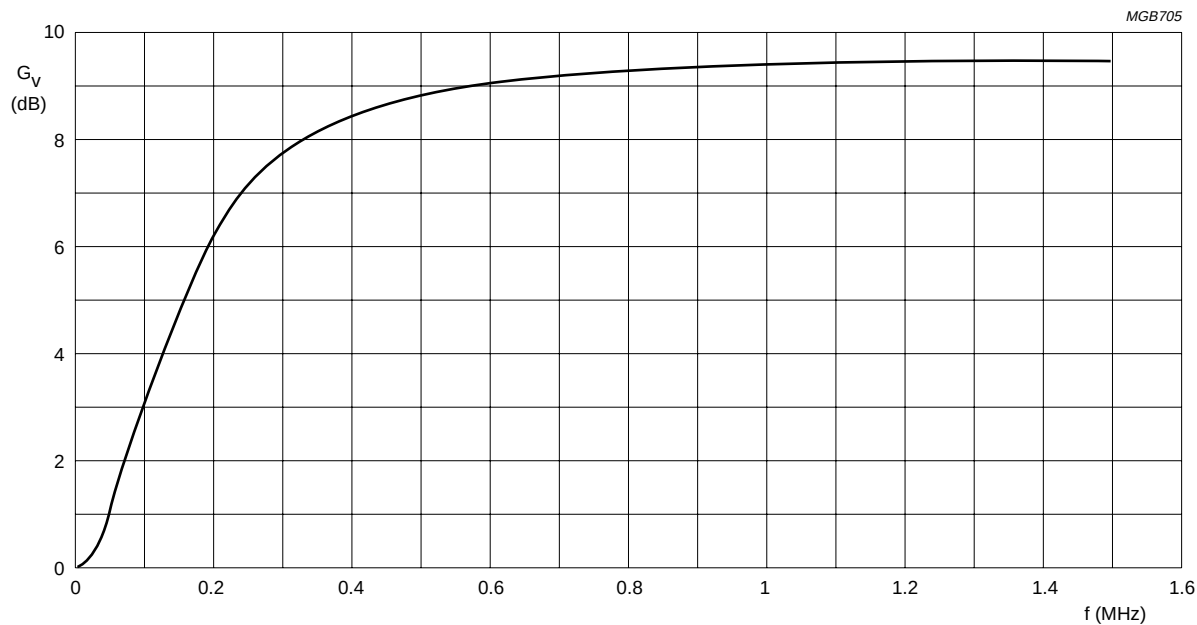


Fig.14 Gain of SECAM pre-emphasis.

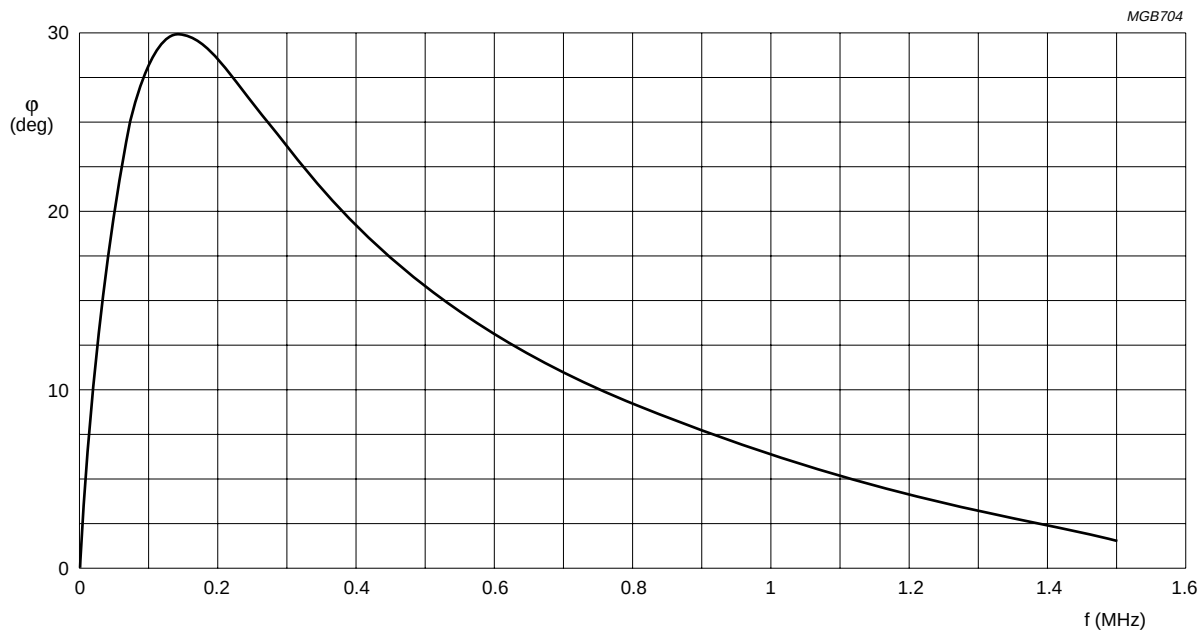


Fig.15 Phase of SECAM pre-emphasis.



Digital video encoder

SAF7129AH

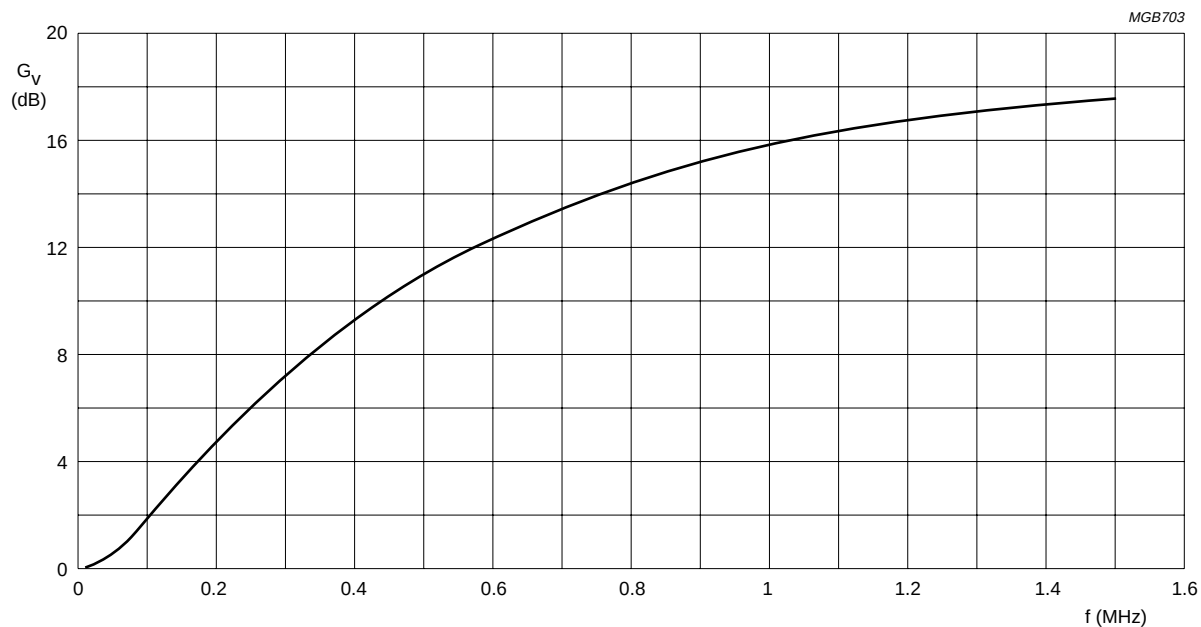


Fig.16 Gain of SECAM anti-Cloche.

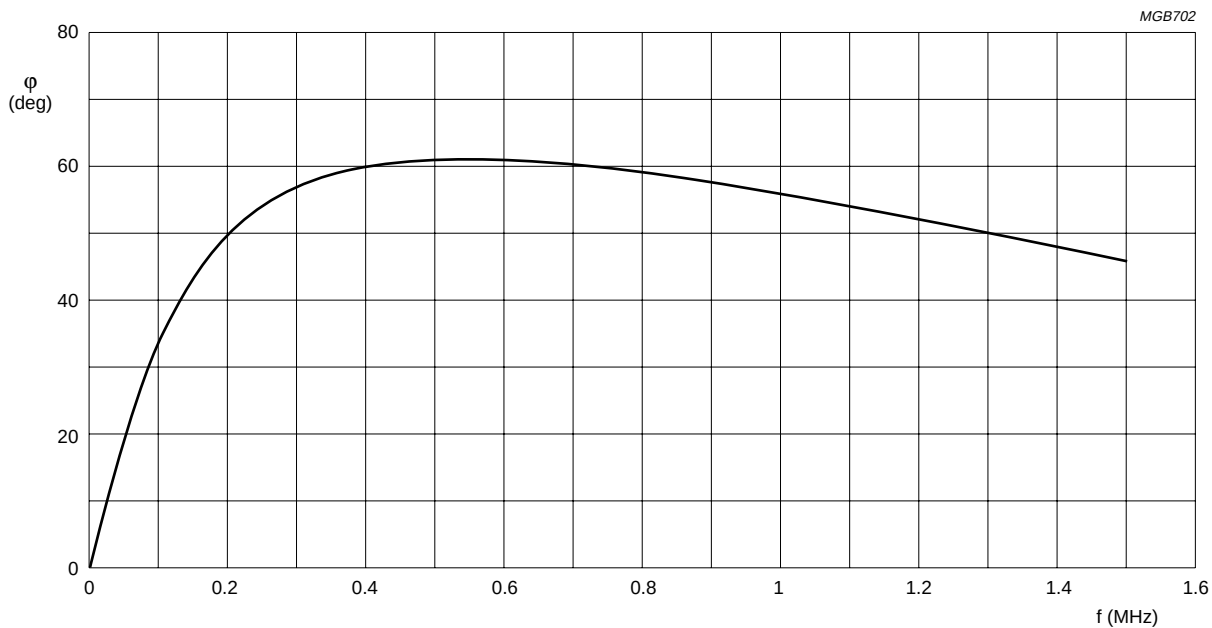
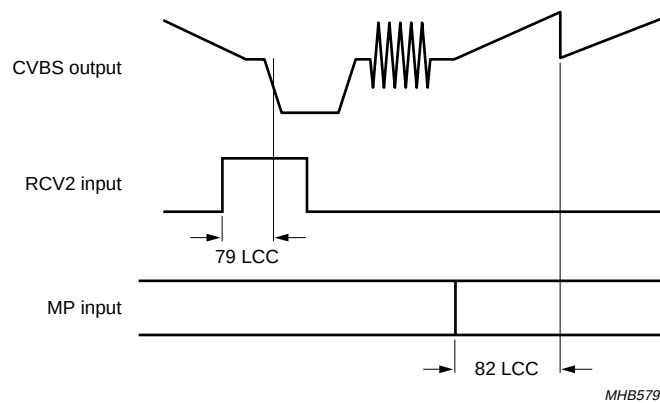


Fig.17 Phase of SECAM anti-Cloche.

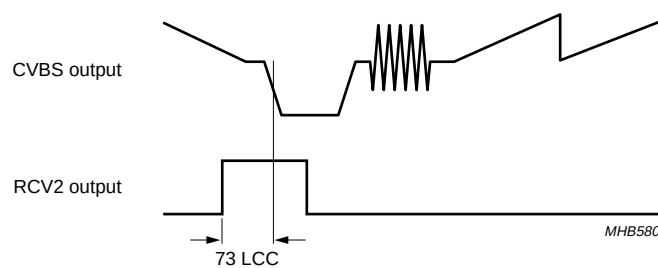
## Digital video encoder

## SAF7129AH



HTRIG = 0  
 PRCV2 = 0.  
 TRCV2 = 1.  
 ORCV2 = 0.

Fig.18 Sync and video input timing.



RCV2S = 0.  
 PRCV2 = 0.  
 ORCV2 = 1.

Fig.19 Sync and video output timing.

## Digital video encoder

## SAF7129AH

**8 LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134); all ground pins connected together and grounded (0 V); all supply pins connected together.

| SYMBOL          | PARAMETER                                                | CONDITIONS                    | MIN. | MAX.            | UNIT |
|-----------------|----------------------------------------------------------|-------------------------------|------|-----------------|------|
| $V_{DDD}$       | digital supply voltage                                   |                               | -0.5 | +4.6            | V    |
| $V_{DDA}$       | analog supply voltage                                    |                               | -0.5 | +4.6            | V    |
| $V_{i(A)}$      | input voltage at analog inputs                           |                               | -0.5 | +4.6            | V    |
| $V_{i(n)}$      | input voltage at pins XTALI, SDA and SCL                 |                               | -0.5 | $V_{DDD} + 0.5$ | V    |
| $V_{i(D)}$      | input voltage at digital inputs or I/O pins              | outputs in 3-state            | -0.5 | +4.6            | V    |
|                 |                                                          | outputs in 3-state;<br>note 1 | -0.5 | +5.5            | V    |
| $\Delta V_{SS}$ | voltage difference between $V_{SSA(n)}$ and $V_{SSD(n)}$ |                               | —    | 100             | mV   |
| $T_{stg}$       | storage temperature                                      |                               | -65  | +150            | °C   |
| $T_{amb}$       | ambient temperature                                      |                               | -40  | +85             | °C   |
| $V_{esd}$       | electrostatic discharge voltage                          | human body model;<br>note 2   | —    | ±2000           | V    |
|                 |                                                          | machine model;<br>note 3      | —    | ±200            | V    |

**Notes**

- Condition for maximum voltage at digital inputs or I/O pins:  $3.0\text{ V} < V_{DDD} < 3.6\text{ V}$ .
- Class 2 according to EIA/JESD22-114-B.
- Class B according to EIA/JESD22-115-A.

**9 THERMAL CHARACTERISTICS**

| SYMBOL        | PARAMETER                                   | CONDITIONS | VALUE             | UNIT |
|---------------|---------------------------------------------|------------|-------------------|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient |            | 47 <sup>(1)</sup> | K/W  |

**Note**

- The overall  $R_{th(j-a)}$  value can vary depending on the board layout. To minimize the effective  $R_{th(j-a)}$  all power and ground pins must be connected to the power and ground layers directly. An ample copper area direct under the SAF7129AH with a number of through-hole plating, which connect to the ground layer (four-layer board: second layer), can also reduce the effective  $R_{th(j-a)}$ . Please do not use any solder-stop varnish under the chip. In addition the usage of soldering glue with a high thermal conductance after curing is recommended.

## Digital video encoder

## SAF7129AH

**10 CHARACTERISTICS**

$V_{DD} = 3.0$  to  $3.6$  V;  $T_{amb} = -40$  to  $+85$  °C; unless otherwise specified.

| SYMBOL                                                        | PARAMETER                                        | CONDITIONS                       | MIN.                    | TYP. | MAX.                       | UNIT |
|---------------------------------------------------------------|--------------------------------------------------|----------------------------------|-------------------------|------|----------------------------|------|
| Supply                                                        |                                                  |                                  |                         |      |                            |      |
| V <sub>DDA</sub>                                              | analog supply voltage                            |                                  | 3.15                    | –    | 3.45                       | V    |
| V <sub>DDD</sub>                                              | digital supply voltage                           |                                  | 3.0                     | –    | 3.6                        | V    |
| I <sub>DDA</sub>                                              | analog supply current                            | note 1                           | –                       | 180  | 190                        | mA   |
| I <sub>DDD</sub>                                              | digital supply current                           | V <sub>DDD</sub> = 3.3 V; note 1 | –                       | 40   | 55                         | mA   |
| Inputs: LLC1, RCV1, RCV2, MP7 to MP0, RTCI, SA, RESET and TTX |                                                  |                                  |                         |      |                            |      |
| V <sub>IL</sub>                                               | LOW-level input voltage                          |                                  | –0.5                    | –    | +0.8                       | V    |
| V <sub>IH</sub>                                               | HIGH-level input voltage                         |                                  | 2.0                     | –    | V <sub>DDD</sub> + 0.3     | V    |
| I <sub>LI</sub>                                               | input leakage current                            |                                  | –                       | –    | 1                          | μA   |
| C <sub>i</sub>                                                | input capacitance                                | clocks                           | –                       | –    | 10                         | pF   |
|                                                               |                                                  | data                             | –                       | –    | 8                          | pF   |
|                                                               |                                                  | I/Os at high-impedance           | –                       | –    | 8                          | pF   |
| Outputs: RCV1, RCV2 and TTXRQ                                 |                                                  |                                  |                         |      |                            |      |
| V <sub>OL</sub>                                               | LOW-level output voltage                         | I <sub>OL</sub> = 2 mA           | –                       | –    | 0.4                        | V    |
| V <sub>OH</sub>                                               | HIGH-level output voltage                        | I <sub>OH</sub> = –2 mA          | 2.4                     | –    | –                          | V    |
| I <sup>2</sup> C-bus: SDA and SCL                             |                                                  |                                  |                         |      |                            |      |
| V <sub>IL</sub>                                               | LOW-level input voltage                          |                                  | –0.5                    | –    | +0.3V <sub>DD(I2C)</sub>   | V    |
| V <sub>IH</sub>                                               | HIGH-level input voltage                         |                                  | 0.7V <sub>DD(I2C)</sub> | –    | V <sub>DD(I2C)</sub> + 0.3 | V    |
| I <sub>i</sub>                                                | input current                                    | V <sub>i</sub> = LOW or HIGH     | –10                     | –    | +10                        | μA   |
| V <sub>OL</sub>                                               | LOW-level output voltage (pin SDA)               | I <sub>OL</sub> = 3 mA           | –                       | –    | 0.4                        | V    |
| I <sub>o</sub>                                                | output current                                   | during acknowledge               | 3                       | –    | –                          | mA   |
| Clock timing: LLC1 and XCLK                                   |                                                  |                                  |                         |      |                            |      |
| T <sub>LLC1</sub>                                             | cycle time                                       | note 2                           | 34                      | –    | 41                         | ns   |
| δ                                                             | duty factor t <sub>HIGH</sub> /T <sub>LLC1</sub> | LLC1 input                       | 40                      | –    | 60                         | %    |
| δ                                                             | duty factor t <sub>HIGH</sub> /T <sub>XCLK</sub> | XCLK output<br>typical 50%       | 40                      | –    | 60                         | %    |
| t <sub>r</sub>                                                | rise time                                        | note 2                           | –                       | –    | 5                          | ns   |
| t <sub>f</sub>                                                | fall time                                        | note 2                           | –                       | –    | 6                          | ns   |
| Input timing: RCV1, RCV2, MP7 to MP0, RTCI, SA and TTX        |                                                  |                                  |                         |      |                            |      |
| t <sub>SU;DAT</sub>                                           | input data set-up time                           |                                  | 6                       | –    | –                          | ns   |
| t <sub>HD;DAT</sub>                                           | input data hold time                             |                                  | 3                       | –    | –                          | ns   |

## Digital video encoder

## SAF7129AH

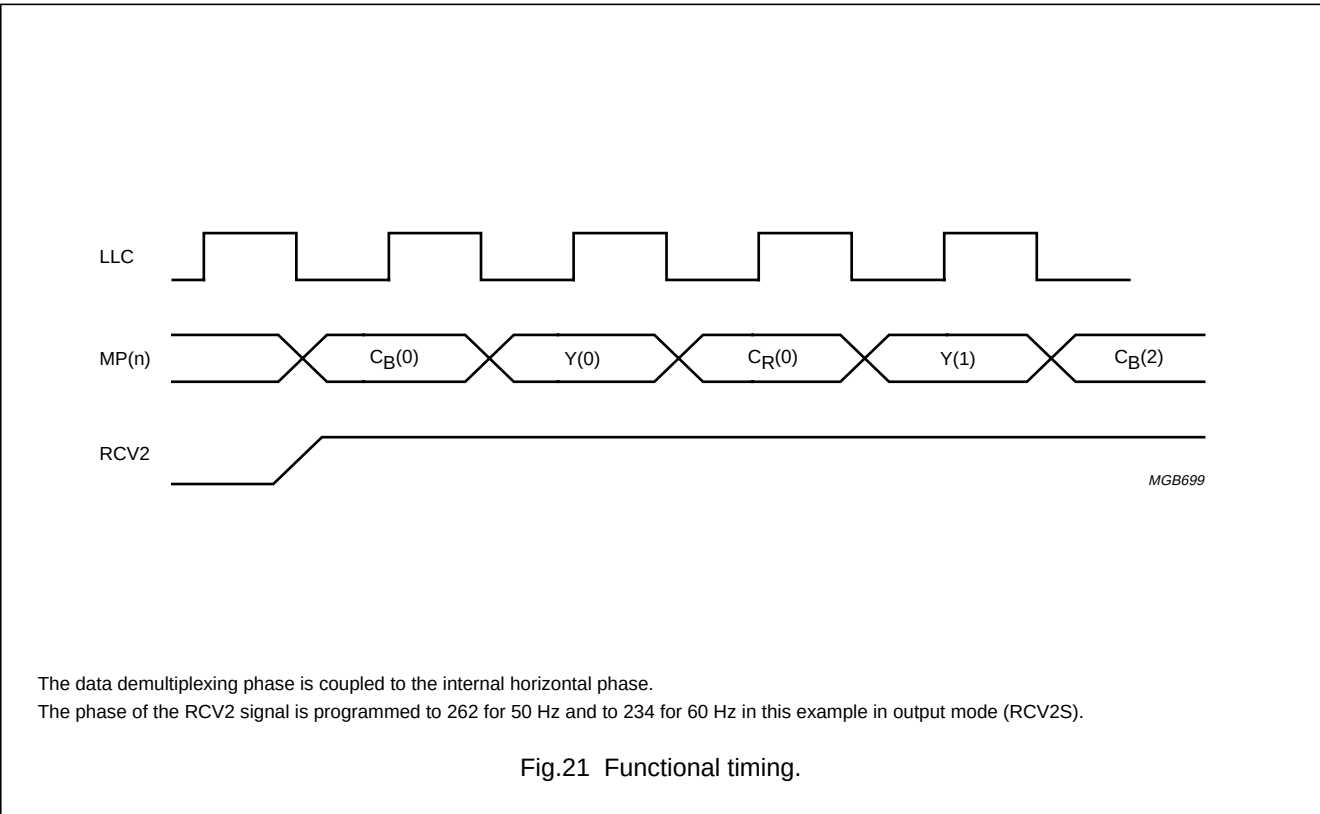
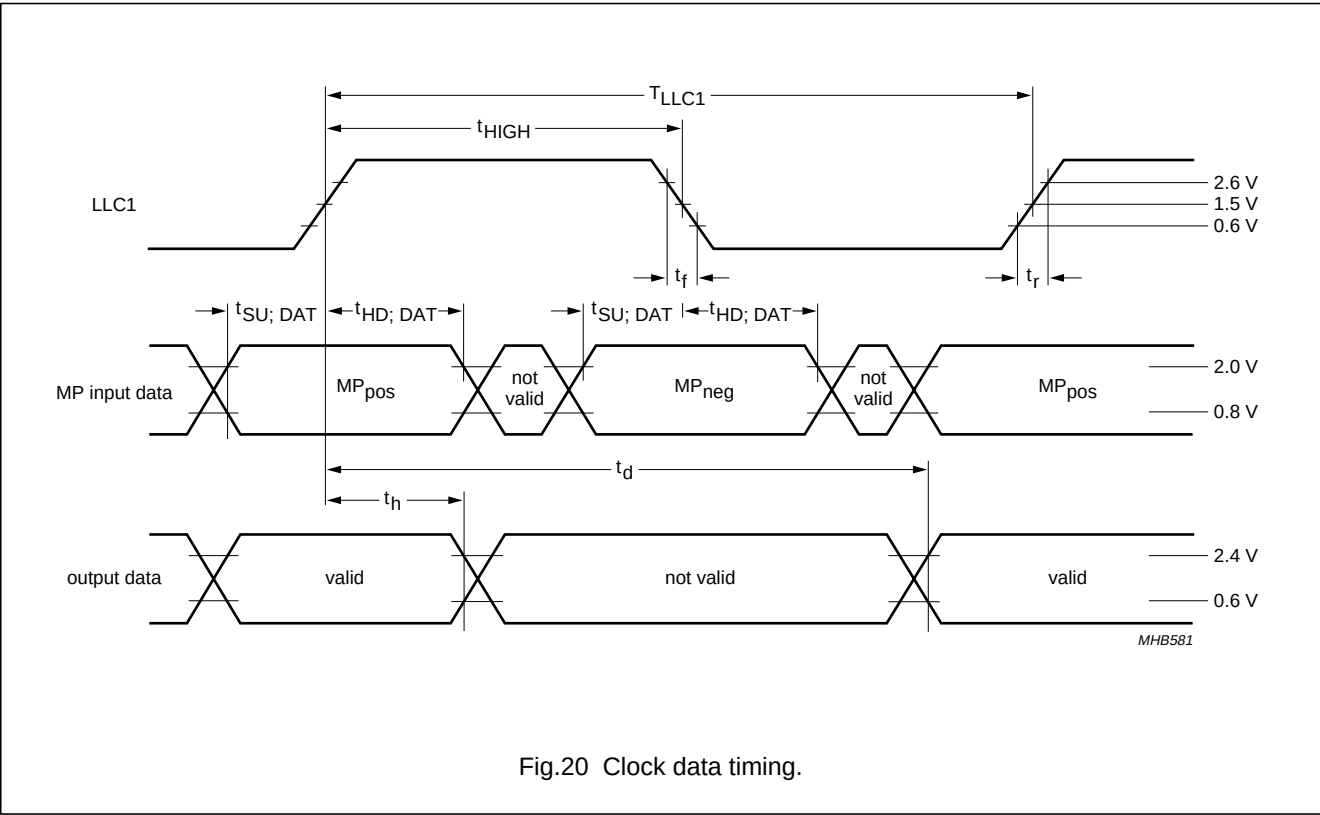
| SYMBOL                                         | PARAMETER                                          | CONDITIONS   | MIN.                 | TYP. | MAX.                 | UNIT     |
|------------------------------------------------|----------------------------------------------------|--------------|----------------------|------|----------------------|----------|
| <b>Crystal oscillator</b>                      |                                                    |              |                      |      |                      |          |
| $f_n$                                          | nominal frequency (usually 27 MHz)                 | 3rd harmonic | –                    | –    | 30                   | MHz      |
| $\Delta f/f_n$                                 | permissible deviation of nominal frequency         | note 3       | $-50 \times 10^{-6}$ | –    | $+50 \times 10^{-6}$ |          |
| CRYSTAL SPECIFICATION                          |                                                    |              |                      |      |                      |          |
| $T_{amb}$                                      | ambient temperature                                |              | 0                    | –    | 70                   | °C       |
| $C_L$                                          | load capacitance                                   |              | 8                    | –    | –                    | pF       |
| $R_S$                                          | series resistance                                  |              | –                    | –    | 80                   | $\Omega$ |
| $C_{mot}$                                      | motional capacitance (typical)                     |              | 1.2                  | 1.5  | 1.8                  | fF       |
| $C_{par}$                                      | parallel capacitance (typical)                     |              | 2.8                  | 3.5  | 4.2                  | pF       |
| <b>Data and reference signal output timing</b> |                                                    |              |                      |      |                      |          |
| $C_L$                                          | output load capacitance                            |              | 7.5                  | –    | 40                   | pF       |
| $t_h$                                          | output hold time                                   |              | 4                    | –    | –                    | ns       |
| $t_d$                                          | output delay time                                  |              | –                    | –    | 18                   | ns       |
| <b>Outputs: C, VBS, CVBS and RGB</b>           |                                                    |              |                      |      |                      |          |
| $V_{oCVBS(p-p)}$                               | output voltage CVBS (peak-to-peak value)           | see Table 76 | –                    | 1.23 | –                    | V        |
| $V_{oVBS(p-p)}$                                | output voltage VBS (S-video) (peak-to-peak value)  | see Table 76 | –                    | 1    | –                    | V        |
| $V_{oC(p-p)}$                                  | output voltage C (S-video) (peak-to-peak value)    | see Table 76 | –                    | 0.89 | –                    | V        |
| $V_{oR,G,B(p-p)}$                              | output voltage R, G, B (peak-to-peak value)        | see Table 76 | –                    | 0.7  | –                    | V        |
| $\Delta V$                                     | inequality of output signal voltages               | note 4       | –                    | –    | 2                    | %        |
| $R_L$                                          | output load resistance                             |              | –                    | 37.5 | –                    | $\Omega$ |
| B                                              | output signal bandwidth of DACs                    | –3 dB        | 10                   | –    | –                    | MHz      |
| $LE_{lf(i)}$                                   | low frequency integral linearity error of DACs     |              | –                    | –    | $\pm 3$              | LSB      |
| $LE_{lf(d)}$                                   | low frequency differential linearity error of DACs |              | –                    | –    | $\pm 1$              | LSB      |
| $t_{d(pipe)(MP)}$                              | total pipeline delay from MP port                  | 27 MHz       | –                    | –    | 82                   | LLC      |

**Notes**

1. At maximum supply voltage with highly active input signals.
2. The data is for both input and output direction.
3. If an internal oscillator is used, crystal deviation of nominal frequency is directly proportional to the deviation of subcarrier frequency and line/field frequency.
4. Referring to peak-to-peak analog voltages resulting from identical peak-to-peak digital codes.

Digital video encoder

SAF7129AH



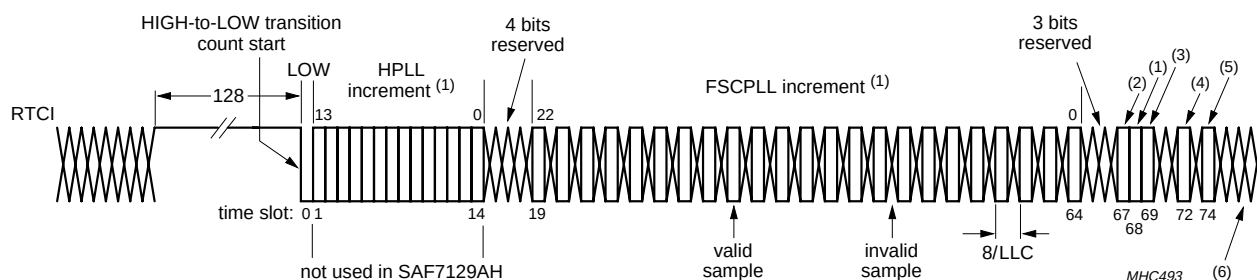
## Digital video encoder

## SAF7129AH

## 10.1 Explanation of RTCI data bits

1. The HPLL increment is not evaluated by the SAF7129AH.
2. The SAF7129AH generates the subcarrier frequency from the FSCPLL increment if enabled (see item 7).
3. The PAL bit indicates the line with inverted (R – Y) component of colour difference signal.
4. If the reset bit is enabled (RTCE = 1; DECPH = 1; PHRES = 00), the phase of the subcarrier is reset in each line whenever the reset bit of RTCI input is set to logic 1.
5. If the FISE bit is enabled (RTCE = 1; DECFIS = 1), the SAF7129AH takes this bit instead of the FISE bit in subaddress 61H.
6. If the odd/even bit is enabled (RTCE = 1; DECOE = 1), the SAF7129AH ignores its internally generated odd/even flag and takes the odd/even bit from RTCI input.
7. If the colour detection bit is enabled (RTCE = 1; DECCOL = 1) and no colour was detected (colour detection bit = 0), the subcarrier frequency is generated by the SAF7129AH. In the other case (colour detection bit = 1) the subcarrier frequency is evaluated out of FSCPLL increment.

If the colour detection bit is disabled (RTCE = 1; DECCOL = 0), the subcarrier frequency is evaluated out of FSCPLL increment, independent of the colour detection bit of RTCI input.



- (1) SAF7113 and SAF7118 support RTC level 3.1.
- (2) Sequence bit: PAL: 0 = (R – Y) line normal, 1 = (R – Y) line inverted; NTSC: 0 = no change.
- (3) FISE bit: 0 = 50 Hz, 1 = 60 Hz.
- (4) Odd/even bit: odd\_even from external.
- (5) Colour detection: 0 = no colour detected, 1 = colour detected.
- (6) Reserved bits: 229 with 50 Hz systems, 226 with 60 Hz systems.

Fig.22 RTCI timing.

## Digital video encoder

## SAF7129AH

## 10.2 Teletext timing

Time  $t_{FD}$  is the time needed to interpolate input data TTX and insert it into the CVBS and VBS output signal, such that it appears at  $t_{TTX} = 9.78 \mu\text{s}$  (PAL) or  $t_{TTX} = 10.5 \mu\text{s}$  (NTSC) after the leading edge of the horizontal synchronization pulse.

Time  $t_{PD}$  is the pipeline delay time introduced by the source that is gated by TTXRQ in order to deliver TTX data. This delay is programmable by register TTXHD. For every active HIGH state at output pin TTXRQ, a new teletext bit must be provided by the source (new protocol) or a window of TTXRQ going HIGH is provided and the number of teletext bits, depending on the chosen teletext standard, is requested at input pin TTX (old protocol).

Since the beginning of the pulses representing the TTXRQ signal and the delay between the rising edge of TTXRQ

and valid teletext input data are fully programmable (TTXHS and TTXHD), the TTX data is always inserted at the correct position after the leading edge of outgoing horizontal synchronization pulse.

Time  $t_{i(TTXW)}$  is the internally used insertion window for TTX data; it has a constant length that allows insertion of 360 teletext bits at a text data rate of 6.9375 Mbits/s (PAL), 296 teletext bits at a text data rate of 5.7272 Mbits/s (WST) or 288 teletext bits at a text data rate of 5.7272 Mbits/s (NABTS). The insertion window is not opened if the control bit TTXEN is logic 0.

Using appropriate programming, all suitable lines of the odd field (TTXOVS and TTXOVE) plus all suitable lines of the even field (TTXEVS and TTXEVE) can be used for teletext insertion.

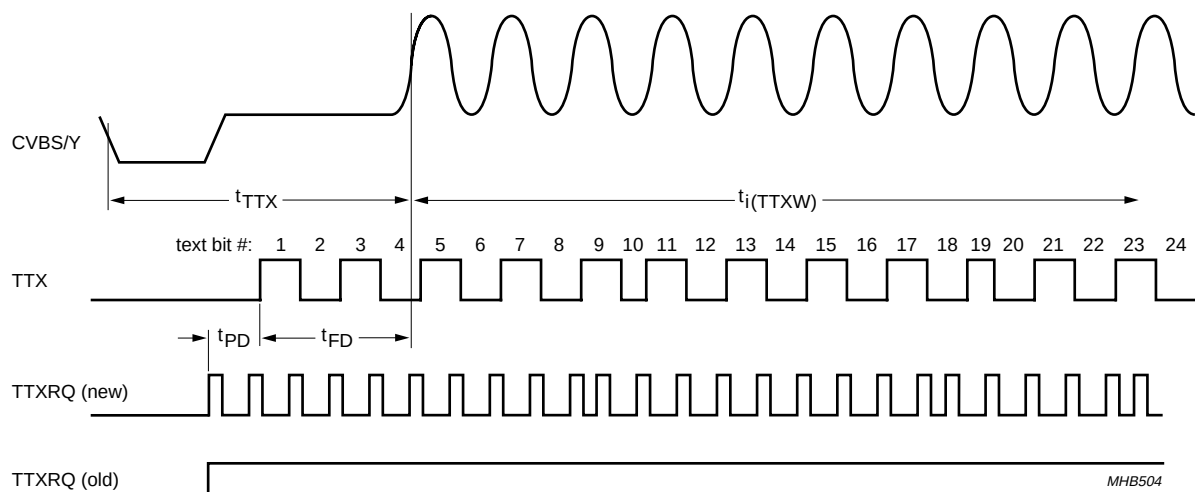


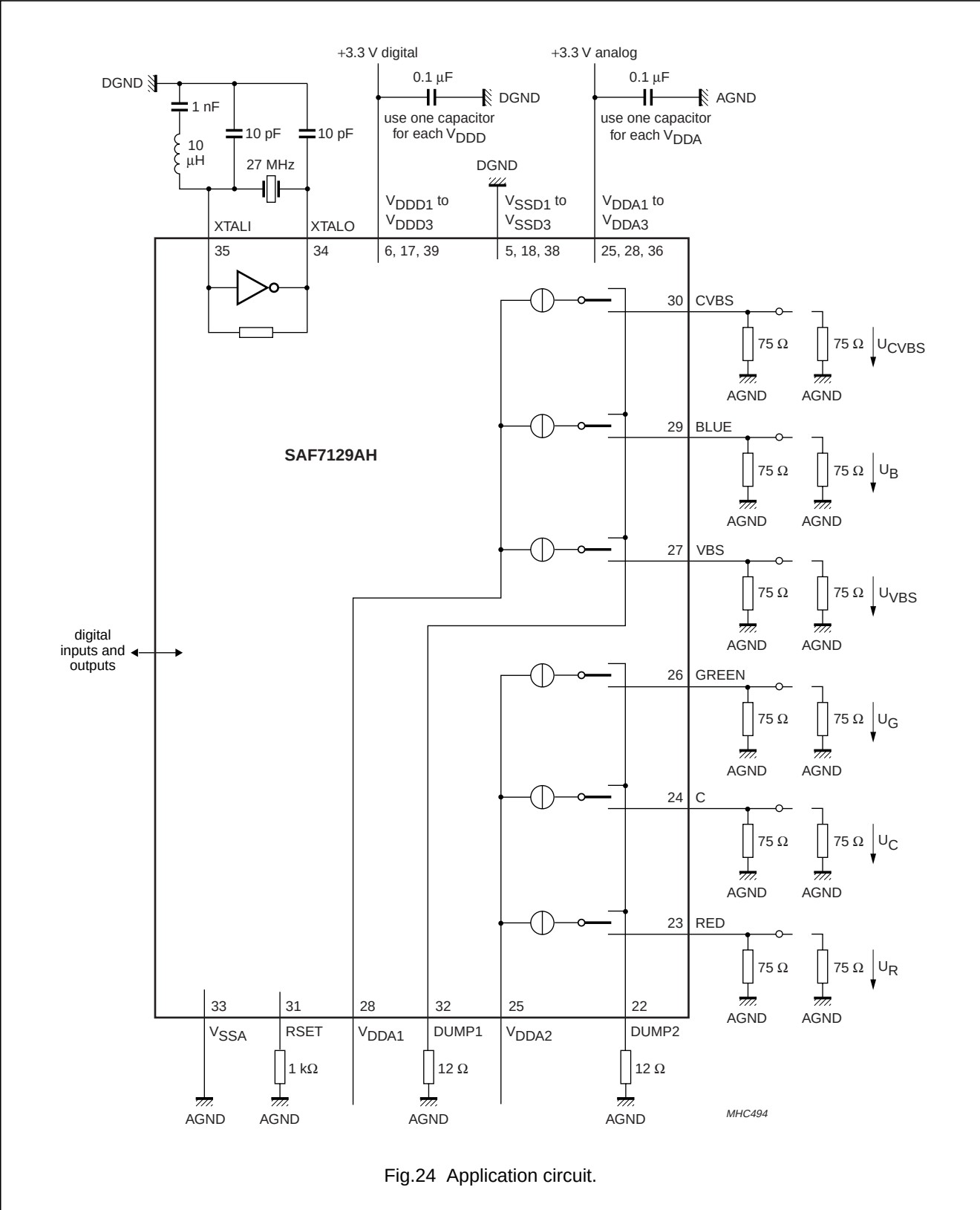
Fig.23 Teletext timing.



Digital video encoder

SAF7129AH

11 APPLICATION INFORMATION



Digital video encoder

SAF7129AH

11.1 Digital output signals

The digital output signals in front of the DACs under nominal conditions occupy different conversion ranges, as indicated in Table 76 for a <sup>100</sup>/<sub>100</sub> colour bar signal.

Values for the external series resistors result in a 75 Ω load.

Table 76 Digital output signals conversion range

| CONVERSION RANGE (peak-to-peak)           |                                       |                                                         |
|-------------------------------------------|---------------------------------------|---------------------------------------------------------|
| CVBS<br>SYNC-TIP TO PEAK-CARRIER (digits) | Y (VBS)<br>SYNC-TIP TO WHITE (digits) | RGB (Y)<br>BLACK TO WHITE AT<br>GDY = GDC = −6 (digits) |
| 1016                                      | 881                                   | 712                                                     |

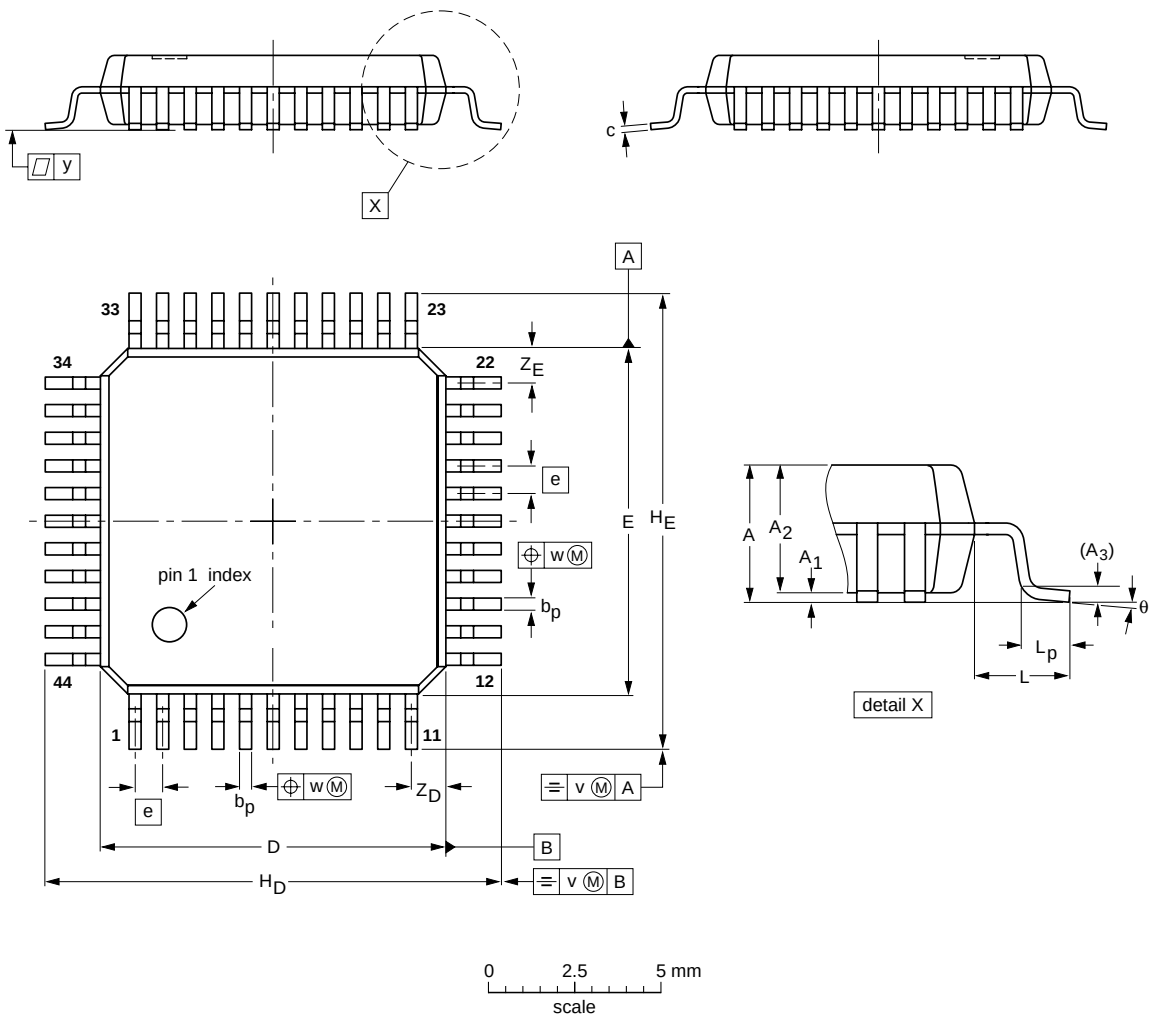
Digital video encoder

SAF7129AH

12 PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 1.6 mm); body 10 x 10 x 2 mm

SOT803-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A<br>max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c            | D <sup>(1)</sup> | E <sup>(1)</sup> | e   | H <sub>D</sub> | H <sub>E</sub> | L   | L <sub>p</sub> | v   | w   | y   | Z <sub>D</sub> <sup>(1)</sup> | Z <sub>E</sub> <sup>(1)</sup> | θ        |
|------|-----------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|-----|----------------|----------------|-----|----------------|-----|-----|-----|-------------------------------|-------------------------------|----------|
| mm   | 2.45      | 0.25<br>0.10   | 2.2<br>1.8     | 0.25           | 0.45<br>0.30   | 0.23<br>0.11 | 10.1<br>9.9      | 10.1<br>9.9      | 0.8 | 13.45<br>12.95 | 13.45<br>12.95 | 1.6 | 1.03<br>0.73   | 0.2 | 0.2 | 0.1 | 1.2<br>0.8                    | 1.2<br>0.8                    | 7°<br>0° |

**Note**  
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE<br>VERSION | REFERENCES |        |           |  | EUROPEAN<br>PROJECTION | ISSUE DATE |
|--------------------|------------|--------|-----------|--|------------------------|------------|
|                    | IEC        | JEDEC  | JEITA     |  |                        |            |
| SOT803-1           | 134E05     | MS-022 | ED-7311CB |  |                        | 03-01-29   |

## Digital video encoder

## SAF7129AH

**13 SOLDERING****13.1 Introduction to soldering surface mount packages**

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

**13.2 Reflow soldering**

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON-T and SSOP-T packages
  - for packages with a thickness  $\geq 2.5$  mm
  - for packages with a thickness  $< 2.5$  mm and a volume  $\geq 350$  mm<sup>3</sup> so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness  $< 2.5$  mm and a volume  $< 350$  mm<sup>3</sup> so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

**13.3 Wave soldering**

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

**13.4 Manual soldering**

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## Digital video encoder

## SAF7129AH

## 13.5 Suitability of surface mount IC packages for wave and reflow soldering methods

| PACKAGE <sup>(1)</sup>                                                                         | SOLDERING METHOD                  |                       |
|------------------------------------------------------------------------------------------------|-----------------------------------|-----------------------|
|                                                                                                | WAVE                              | REFLOW <sup>(2)</sup> |
| BGA, HTSSON..T <sup>(3)</sup> , LBGA, LFBGA, SQFP, SSOP..T <sup>(3)</sup> , TFBGA, USON, VFBGA | not suitable                      | suitable              |
| DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS           | not suitable <sup>(4)</sup>       | suitable              |
| PLCC <sup>(5)</sup> , SO, SOJ                                                                  | suitable                          | suitable              |
| LQFP, QFP, TQFP                                                                                | not recommended <sup>(5)(6)</sup> | suitable              |
| SSOP, TSSOP, VSO, VSSOP                                                                        | not recommended <sup>(7)</sup>    | suitable              |
| CWQCCN..L <sup>(8)</sup> , PMFP <sup>(9)</sup> , WQCCN..L <sup>(8)</sup>                       | not suitable                      | not suitable          |

## Notes

- For more detailed information on the BGA packages refer to the “(LF)BGA Application Note” (AN01026); order a copy from your Philips Semiconductors sales office.
- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”.
- These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding  $217\text{ °C} \pm 10\text{ °C}$  measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
- These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- If wave soldering is considered, then the package must be placed at a  $45^\circ$  angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
- Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
- Hot bar or manual soldering is suitable for PMFP packages.

## Digital video encoder

## SAF7129AH

## 14 DATA SHEET STATUS

| LEVEL | DATA SHEET STATUS <sup>(1)</sup> | PRODUCT STATUS <sup>(2)(3)</sup> | DEFINITION                                                                                                                                                                                                                                                                                     |
|-------|----------------------------------|----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| I     | Objective data                   | Development                      | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.                                                                                                    |
| II    | Preliminary data                 | Qualification                    | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.             |
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3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## 15 DEFINITIONS

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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## Digital video encoder

SAF7129AH

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SCA76

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