NEW ADVANCED INFORMATION

MX29F001T/B

1M-BIT [128K x 8] CMOS FLASH MEMORY

FEATURES

- 5.0V ± 10% for read, erase and write operation
- 131072x8 only organization
- Fast access time: 55/70/90/120ns
- Low power consumption
  - 30mA maximum active current(5MHz)
  - 1uA typical standby current
- Command register architecture
  - Byte Programming (7us typical)
  - Sector Erase (8K-Byte x1,4K-Byte x 2, 8K Bytex2, 32K-Bytex1, and 64K-Byte x1)
- Auto Erase (chip & sector) and Auto Program
  - Automatically erase any combination of sectors with Erase Suspend capability.
  - Automatically programs and verifies data at specified address
- Erase Suspend/Erase Resume
  - Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation.
- Status Reply
  - Data polling & Toggle bit for detection of program and erase cycle completion.
- Chip protect/unprotect for 5V only system or 5V/12V system
- 10,000 minimum erase/program cycles
- Latch-up protected to 100mA from -1 to VCC+1V
- Boot Code Sector Architecture
  - T = Top Boot Sector
  - B = Bottom Boot Sector
- Low VCC write inhibit is equal to or less than 3.2V
- Package type:
  - 32-pin PLCC
  - 32-pin TSOP
  - 32-pin PDIP
- Boot Code Sector Architecture
  - T=Top Boot Sector
  - B=Bottom Boot Sector

GENERAL DESCRIPTION

The MX29F001T/B is a 1-mega bit Flash memory organized as 128K bytes of 8 bits only MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX29F001T/B is packaged in 32-pin PLCC, TSOP, PDIP. It is designed to be reprogrammed and erased in-system or in-standard EPROM programmers.

The standard MX29F001T/B offers access time as fast as 55ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX29F001T/B has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

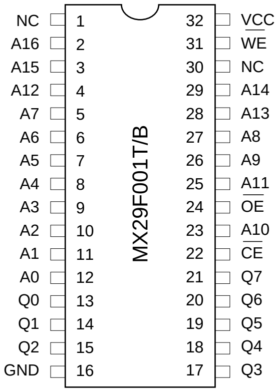
MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX29F001T/B uses a command register to manage this functionality. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

MXIC Flash technology reliably stores memory contents even after 10,000 erase and program cycles. The MXIC cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The MX29F001T/B uses a 5.0V ± 10% VCC supply to perform the High Reliability Erase and auto Program/Erase algorithms.

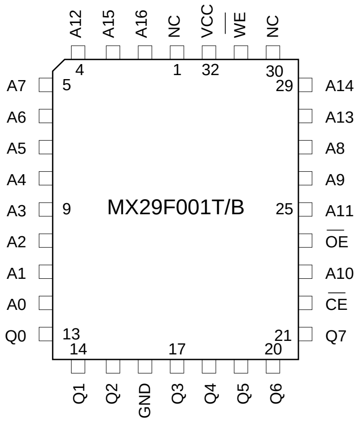
The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC + 1V.

PIN CONFIGURATIONS

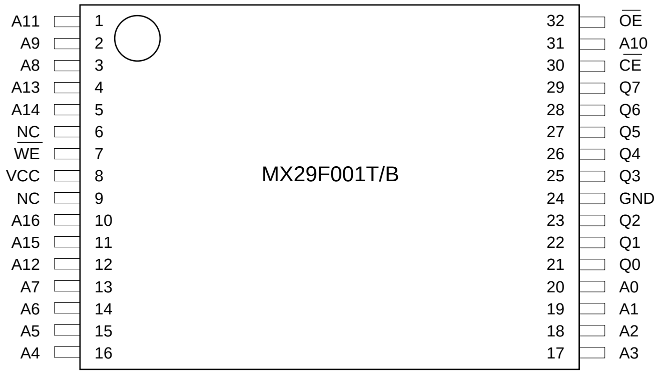
32 PDIP



32PLCC



TSOP (TYPE 1)

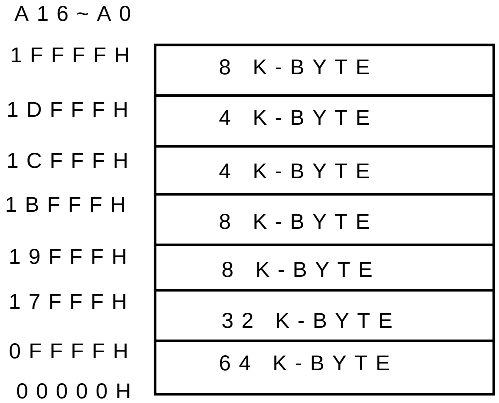


(NORMAL TYPE)

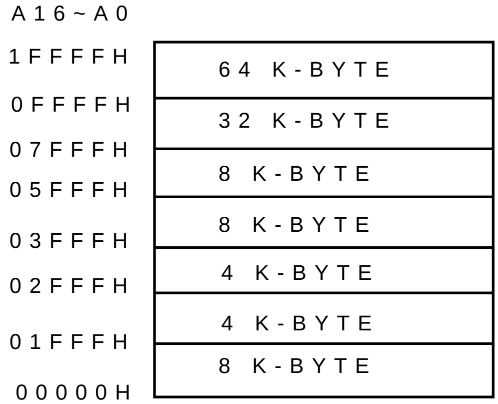
PIN DESCRIPTION:

SYMBOL	PIN NAME
A0~A16	Address Input
Q0~Q7	Data Input/Output
CE	Chip Enable Input
WE	Write Enable Input
OE	Output Enable Input
VCC	Power Supply Pin (+5V)
GND	Ground Pin

SECTOR STRUCTURE

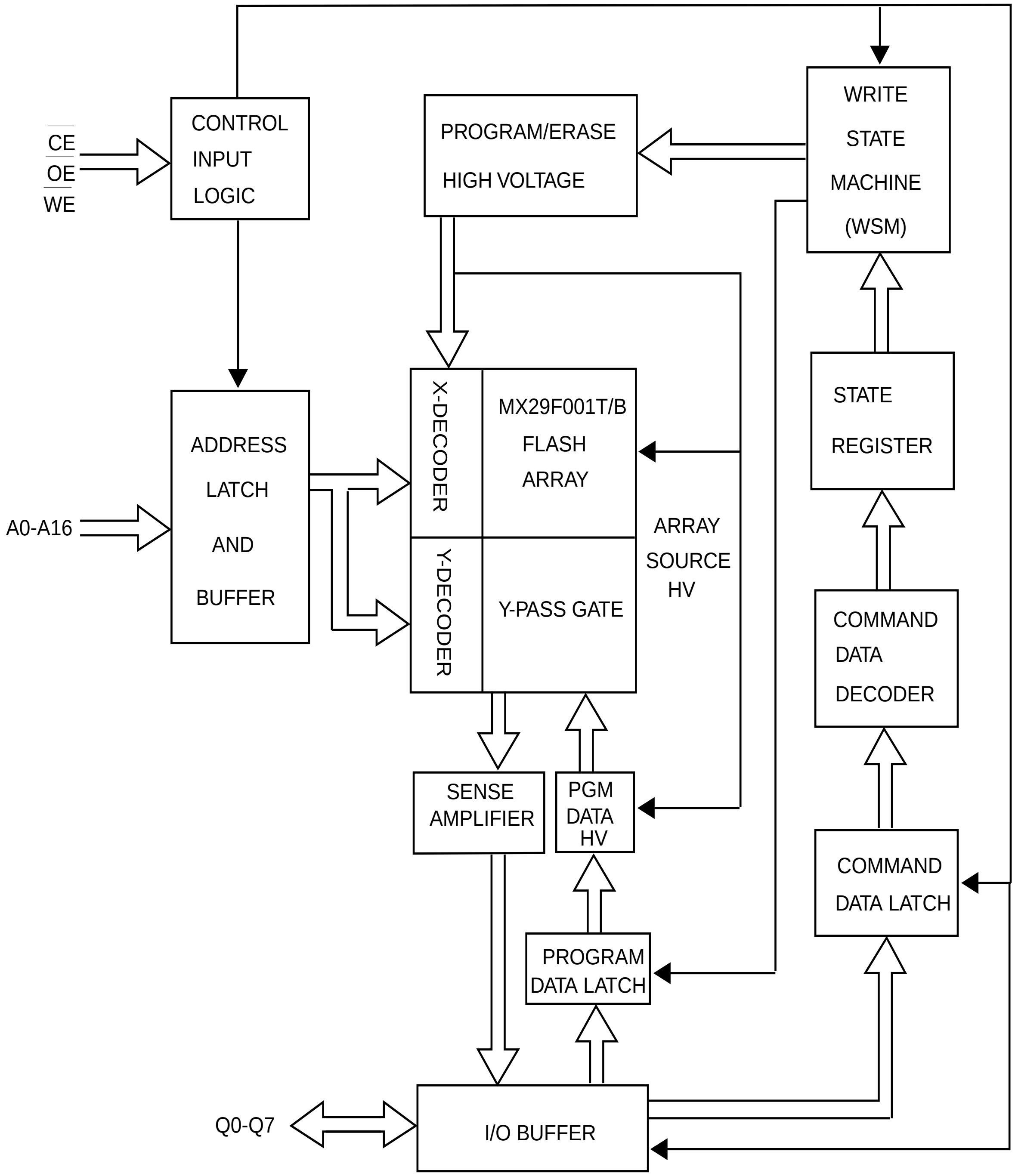


MX29F001T Sector Architecture



MX29F001B Sector Architecture

BLOCK DIAGRAM



AUTOMATIC PROGRAMMING

The MX29F001T/B is byte programmable using the Automatic Programming algorithm. The Automatic Programming algorithm does not require the system to time out or verify the data programmed. The typical chip programming time of the MX29F001T/B at room temperature is less than 3.5 seconds.

AUTOMATIC CHIP ERASE

The entire chip is bulk erased using 10 ms erase pulses according to MXIC's Automatic Chip Erase algorithm. Typical erasure at room temperature is accomplished in less than 3 second. The Automatic Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are internally controlled within the device.

AUTOMATIC SECTOR ERASE

The MX29F001T/B is sector(s) erasable using MXIC's Auto Sector Erase algorithm. Sector erase modes allow sectors of the array to be erased in one erase cycle. The Automatic Sector Erase algorithm automatically programs the specified sector(s) prior to electrical erase. The timing and verification of electrical erase are internally con trolled by the device.

AUTOMATIC PROGRAMMING ALGORITHM

MXIC's Automatic Programming algorithm requires the user to only write program set-up commands (include 2 unlock write cycle and A0H) and a program command (program data and address). The device automatically times the programming pulse width, provides the program verification, and counts the number of sequences. A status bit similar to $\overline{\text{DATA}}$ polling and a status bit toggling between consecutive read cycles, provides feedback to the user as to the status of the programming operation.

AUTOMATIC ERASE ALGORITHM

MXIC's Automatic Erase algorithm requires the user to write commands to the command register using standard microprocessor write timings. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, provides the erase verification, and counts the number of sequences. A status bit toggling between consecutive read cycles provides feedback to the user as to the status of the programming operation.

Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches addresses and data needed for the programming and erase operations. During a system write cycle, addresses are latched on the falling edge, and data are latched on the rising edge of $\overline{\text{WE}}$.

MXIC's Flash technology combines years of EPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MX29F001T/B electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed by using the EPROM programming mechanism of hot electron injection.

During a program cycle, the state-machine will control the program sequences and command register will not respond to any command set. During a Sector Erase cycle, the command register will only respond to Erase Suspend command. After Erase Suspend is completed, the device stays in read mode. After the state machine has completed its task, it will allow the command register to respond to its full command set.

TABLE1. SOFTWARE COMMAND DEFINITIONS

Command	Bus	First Bus Cycle		Second Bus Cycle		Third Bus Cycle		Fourth Bus Cycle		Fifth Bus Cycle		Sixth Bus Cycle	
	Cycle	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset	1	XXXH	F0H										
Read	1	RD	RD										
Read Silicon ID	4	555H	AAH	2AAH	55H	555H	90H	ADI	DDI				
Chip Protect Verify	4	555H	AAH	2AAH	55H	555H	90H	(SA) X02H	00H 01H				
Porgram	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD				
Chip Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
Sector Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	30H
Sector Erase Suspend	1	XXXH	B0H										
Sector Erase Resume	1	XXXH	30H										
Unlock for chip protect/unprotect	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	20H

Note:

1. ADI = Address of Device identifier;A1=0, A0 =0 for manufacture code, A1=0, A0 =1 for device code.(Refer to Table 3)
   DDI = Data of Device identifier : C2H for manufacture code, 18H/19H for device code.
   X = X can be VIL or VIH
   RA=Address of memory location to be read.
   RD=Data to be read at location RA.
2. PA = Address of memory location to be programmed.
   PD = Data to be programmed at location PA.
   SA = Address to the sector to be erased.
3. The system should generate the following address patterns: 555H or 2AAH to Address A0~A10.
   Address bit A11~A16=X=Don't care for all address commands except for Program Address (PA) and Sector Address (SA). Write Sequence may be initiated with A11~A16 in either state.
4. For chip protect verify operation : If read out data is 01H, it means the chip has been protected. If read out data is 00H, it means the chip is still not being protected.

COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. Table 1 defines the valid register command sequences. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress. Either of the two reset command sequences will reset the device(when applicable).

TABLE 2. MX29F001T/B BUS OPERATION

Pins Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A6	A9	Q0 ~ Q7
Read Silicon ID Manfacturer Code(1)	L	L	H	L	L	X	V_{ID}(2)	C2H
Read Silicon ID Device Code(1)	L	L	H	H	L	X	V_{ID}(2)	18H/19H
Read	L	L	H	A0	A1	A6	A9	D_{OUT}
Standby	H	X	X	X	X	X	X	HIGH Z
Output Disable	L	H	H	X	X	X	X	HIGH Z
Write	L	H	L	A0	A1	A6	A9	D_{IN}(3)
Chip Protect with 12V system(6)	L	V_{ID}(2)	L	X	X	L	V_{ID}(2)	X
Chip Unprotect with 12V system(6)	L	V_{ID}(2)	L	X	X	H	V_{ID}(2)	X
Verify Chip Protect with 12V system	L	L	H	X	H	X	V_{ID}(2)	Code(5)
Chip Protect without 12V system (6)	L	H	L	X	X	L	H	X
Chip Unprotect without 12V system (6)	L	H	L	X	X	H	H	X
Verify Chip Protect/Unprotect without 12V system (7)	L	L	H	X	H	X	H	Code(5)
Reset	X	X	X	X	X	X	X	HIGH Z

NOTES:

1. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 1.
2. VID is the Silicon-ID-Read high voltage, 11.5V to 12.5V.
3. Refer to Table 1 for valid Data-In during a write operation.
4. X can be VIL or VIH.
5. Code=00H means unprotected.
   Code=01H means protected.
6. Refer to chip protect/unprotect algorithm and waveform.
   Must issue "unlock for chip protect/unprotect" command before "chip protect/unprotect without 12V system" command.
7. The "verify chip protect/unprotect without 12V sysytem" is only following "Chip protect/unprotect without 12V system" command.

READ/RESET COMMAND

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

If program-fail or erase-fail happen, the write of F0H will reset the device to abort the operation. A valid command must then be written to place the device in the desired state.

SILICON-ID-READ COMMAND

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access siganature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not generally desired system design practice.

The MX29F001T/B contains a Silicon-ID-Read operation to supplement traditional PROM programming methodology. The operation is initiated by writing the read silicon ID command sequence into the command register. Following the command write, a read cycle with A1=VIL,A0=VIL retrieves the manufacturer code of C2H. A read cycle with A1=VIL, A0=VIH returns the device code of 18H for MX29F001T,19H for MX29F001B.

SET-UP AUTOMATIC CHIP ERASE COMMANDS

Chip erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command 80H. Two more "unlock" write cycles are then followed by the chip erase command 10H.

The Automatic Chip Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Chip Erase. Upon executing the Automatic Chip Erase, the device will automatically program and verify the entire memory for an all-zero data pattern. When the device is automatically verified to contain an all-zero pattern, a self-timed chip erase and verification begin. The erase and verification operations are completed when the data on Q7 is "1" at which time the device returns to the Read mode. The system does not require to provide any control or timing during these operations.

When using the Automatic Chip Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array(no erase verify command is required).

If the Erase operation was unsuccessful, the data on Q5 is "1"(see Table 4), indicating an erase operation exceed internal timing limit.

The automatic erase begins on the rising edge of the last WE pulse in the command sequence and terminates when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode.

TABLE 3. EXPANDED SILICON ID CODE

Pins	A0	A1	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Code(Hex)
Manufacture code	VIL	VIL	1	1	0	0	0	0	1	0	C2H
Device code for MX29F001T	VIH	VIL	0	0	0	1	1	0	0	0	18H
Device code for MX29F001B	VIH	VIL	0	0	0	1	1	0	0	1	19H
Chip Protection Verification	X	VIH	0	0	0	0	0	0	0	1	01H (Protected)
	X	VIH	0	0	0	0	0	0	0	0	00H (Unprotected)

SECTOR ERASE COMMANDS

The Automatic Sector Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Set-up Sector Erase command and Automatic Sector Erase command. Upon executing the Automatic Sector Erase command, the device will automatically program and verify the sector(s) memory for an all-zero data pattern. The system does not require to provide any control or timing during these operations.

When the sector(s) is automatically verified to contain an all-zero pattern, a self-timed sector erase and verification begin. The erase and verification operations are complete when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode. The system does not require to provide any control or timing during these operations.

When using the Automatic Sector Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verification command is required). Sector erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the set-up command 80H. Two more "unlock" write cycles are then followed by the sector erase command 30H. The sector address is latched on the falling edge of $\overline{WE}$, while the command(data) is latched on the rising edge of $\overline{WE}$. Sector addresses selected are loaded into internal register on the sixth falling edge of $\overline{WE}$. Each successive sector load cycle started by the falling edge of $\overline{WE}$ must begin within 80ms from the rising edge of the preceding $\overline{WE}$. Otherwise, the loading period ends and internal auto sector erase cycle starts. (Monitor Q3 to determine if the sector erase timer window is still open, see section Q3, Sector Erase Timer.) Any command other than Sector Erase (30H) or Erase Suspend (B0H) during the time-out period resets the derice to read mode.

ERASE SUSPEND

This command only has meaning while the state machine is executing Automatic Sector Erase operation, and therefore will only be responded during Automatic Sector Erase operation. Writing the Erase Suspend command during the Sector Erase time-out immediately terminates the time-out immediately terminates the time-out period and suspends the erase operation. After this command has been executed, the command register will initiate erase suspend mode. The state machine will return to read mode automatically after suspend is ready. At this time, state machine only allows the command register to respond to the Read Memory Array, Erase Resume and Program commands.

The system can determine the status of the program operation using the Q7 or Q6 status bits, just as in the standard program operation. After an erase-suspend program operation is complete, the system can once again read array data within non-suspended sectors.

Table 4. Write Operation Status

	Status		Q7	Q6	Q5	Q3
In Progress	Byte Program in Auto Program Algorithm		$\overline{Q7}$	Toggle	0	N/A
	Auto Erase Algorithm		0	Toggle	0	1
	Erase Suspended Mode	Erase Suspend Read	Data	Data	Data	Data
		Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{Q7}$	Toggle (Note1)	0	N/A
Exceeded Time Limits	Byte Program in Auto Program Algorithm		$\overline{Q7}$	Toggle	1	N/A
	Erase in Auto Erase Algorithm		0	Toggle	1	1
	Erase Suspended Mode	Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{Q7}$	Toggle	1	N/A

Note:

1. Performing successive read operations from any address will cause Q6 to toggle.

ERASE RESUME

This command will cause the command register to clear the suspend state and return back to Sector Erase mode but only if an Erase Suspend command was previously issued. Erase Resume will not have any effect in all other conditions.Another Erase Suspend command can be written after the chip has resumed erasing.

SET-UP AUTOMATIC PROGRAM COMMANDS

To initiate Automatic Program mode, A three-cycle command sequence is required. There are two "unlock" write cycles. These are followed by writing the Automatic Program command A0H.

Once the Automatic Program command is initiated, the next WE pulse causes a transition to an active programming operation. Addresses are latched on the falling edge, and data are internally latched on the rising edge of the WE pulse. The rising edge of WE also begins the programming operation. The system does not require to provide further controls or timings. The device will automatically provide an adequate internally generated program pulse and verify margin.

If the program opetation was unsuccessful, the data on Q5 is "1"(see Table 4), indicating the program operation exceed internal timing limit. The automatic programming operation is completed when the data read on Q6 stops toggling for two consecutive read cycles and the data on Q7 and Q6 are equivalent to data written to these two bits, at which time the device returns to the Read mode(no program verify command is required).

WRITE OPERATION STATUS

TOGGLE BIT-Q6

The MX29F001T/B features a "Toggle Bit" as a method to indicate to the host system that the Auto Program/ Erase algorithms are either in progress or complete.

While the Automatic Program or Erase algorithm is in progress, successive attempts to read data from the device will result in Q6 toggling between one and zero. Once the Automatic Program or Erase algorithm is completed, Q6 will stop toggling and valid data will be read. The toggle bit is valid after the rising edge of the sixth WE pulse of the six write pulse sequences for chip/ sector erase.

The Toggle Bit feature is active during Automatic Program/ Erase algorithms or sector erase time-out.(see section Q3 Sector Erase Timer)

DATA POLLING-Q7

The MX29F001T/B also features Data Polling as a method to indicate to the host system that the Automatic Program or Erase algorithms are either in progress or completed.

While the Automatic Programming algorithm is in operation, an attempt to read the device will produce the complement data of the data last written to Q7. Upon completion of the Automatic Program Algorithm an attempt to read the device will produce the true data last written to Q7. The Data Polling feature is valid after the rising edge of the fourth WE pulse of the four write pulse sequences for automatic program.

While the Automatic Erase algorithm is in operation, Q7 will read "0" until the erase operation is competed. Upon completion of the erase operation, the data on Q7 will read "1". The Data Polling feature is valid after the rising edge of the sixth WE pulse of six write pulse sequences for automatic chip/sector erase.

The Data Polling feature is active during Automatic Program/Erase algorithm or sector erase time-out.(see section Q3 Sector Erase Timer)

Q5
Exceeded Timing Limits

Q5 will indicate if the program or erase time has exceeded the specified limits(internal pulse count). Under these conditions Q5 will produce a "1". This time-out condition indicates that the program or erase cycle was not successfully completed. Data Polling and Toggle Bit are the only operating functions of the device under this condition.

If this time-out condition occurs during sector erase operation, it is specifies that a particular sector is bad and it may not be reused. However, other sectors are still functional and may be used for the program or erase operation. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this time-out condition occures during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this time-out condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector maynot be reused, (other sectors are still functional and can be reused).

The time-out condition may also appear if a user tries to program a non blank location without erasing. In this case the device locks out and never completes the Automatic Algorithm operation. Hence, the system never reads a valid data on Q7 bit and Q6 never stops toggling. Once the Device has exceeded timing limits, the Q5 bit will indicate a "1". Please note that this is not a device failure condition since the device was incorrectly used.

Q3
Sector Erase Timer

After the completion of the initial sector erase command sequence th sector erase time-out will begin. Q3 will remain low until the time-out is complete. Data Polling and Toggle Bit are valid after the initial sector erase command sequence.

If Data Polling or the Toggle Bit indicates the device has been written with a valid erase command, Q3 may be used to determine if the sector erase timer window is still open. If Q3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by Data Polling or Toggle Bit. If Q3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of Q3 prior to and following each subsequent sector erase command. If Q3 were high on the second status check, the command may not have been accepted.

DATA PROTECTION

The MX29F001T/B is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the Read mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

WRITE PULSE "GLITCH" PROTECTION

Noise pulses of less than 5ns(typical) on $\overline{\text{CE}}$ or $\overline{\text{WE}}$ will not initiate a write cycle.

LOGICAL INHIBIT

Writing is inhibited by holding any one of $\overline{\text{OE}}$ = VIL, $\overline{\text{CE}}$ = VIH or WE = VIH. To initiate a write cycle CE and WE must be a logical zero while OE is a logical one.

POWER SUPPLY DECOUPLING

In order to reduce power switching effect, each device should have a 0.1uF ceramic capacitor connected between its VCC and GND. (Using a 10uF bulk capacitor connected for high current condition is available if necessary.)

CHIP PROTECTION WITH 12V SYSTEM

The MX29F001T/B features hardware chip protection. which will disable both program and erase operations. To activate this mode, the programming equipment must force VID on address pin A9 and control pin $\overline{\text{OE}}$, (suggest VID=12V) A6=VIL and $\overline{\text{CE}}$=VIL.(see Table 2) Programming of the protection circuitry begins on the falling edge of the $\overline{\text{WE}}$ pulse and is terminated with the rising edge of the same. Please refer to chip protect algorithm and waveform.

To verify programming of the protection circuitry, the programming equipment must force VID on address pin A9 (with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ at VIL and $\overline{\text{WE}}$ at VIH. When A1=1, it will produce a logical "1" code at device output Q0 for the protected status. Otherwise the device will produce 00H for the unprotected status. In this mode, the address,except for A1, are don't care. Address locations with A1 = VIL are reserved to read manufacturer and device codes.(Read Silicon ID)

It is also possible to determine if the chip is protected in the system by writing a Read Silicon ID command. Performing a read operation with A1=VIH, it will produce a logical "1" at Q0 for the protected status.

CHIP UNPROTECT WITH 12V SYSTEM

The MX29F001T/B also features the chip unprotect mode, so that all sectors are unprotected after chip unprotect completion to incorporate any changes in the code.

To activate this mode, the programming equipment must force VID on control pin OE and address pin A9. The CE pins must be set at VIL. Pins A6 must be set to VIH.(see Table 2) Refer to chip unprotect algorithm and waveform for the chip unprotect algorithm. The unprotection mechanism begins on the falling edge of the WE pulse and is terminated with the rising edge of the same.

It is also possible to determine if the chip is unprotected in the system by writing the Read Silicon ID command. Performing a read operation with A1=VIH, it will produce 00H at data outputs (Q0-Q7) for an unprotected sector. It is noted that all sectors are unprotected after the chip unprotect algorithm is completed.

CHIP PROTECTION WITHOUT 12V SYSTEM

The MX29F001T/B also feature a hardware chip protection method in a system without 12V power suppply. The programming equipment do not need to supply 12 volts to protect all sectors. The details are shown in chip protect algorithm and waveform.

CHIP UNPROTECT WITHOUT 12V SYSTEM

The MX29F001T/B also feature a hardware chip unprotection method in a system without 12V power supply. The programming equipment do not need to supply 12 volts to unprotect all sectors. The details are shown in chip unprotect algorithm and waveform.

POWER-UP SEQUENCE

The MX29F001T/B powers up in the Read only mode. In addition, the memory contents may only be altered after successful completion of the predefined command sequences.

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to 7.0V
VCC to Ground Potential	-0.5V to 7.0V
A9&$\overline{OE}$	-0.5V to 13.5V

NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:
Specifications contained within the following tables are subject to change.

CAPACITANCE TA = 25°C, f = 1.0 MHz

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
CIN1	Input Capacitance			8	pF	VIN = 0V
CIN2	Control Pin Capacitance			12	pF	VIN = 0V
COUT	Output Capacitance			12	pF	VOUT = 0V

READ OPERATION
DC CHARACTERISTICS TA = 0°C TO 70°C, VCC = 5V ± 10%(VCC = 5V ± 5% for 29F001T/B-55)

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
ILI	Input Leakage Current			1	uA	VIN = GND to VCC
ILO	Output Leakage Current			10	uA	VOUT = GND to VCC
ISB1	Standby VCC current			1	mA	CE = VIH
ISB2			1	5	uA	CE = VCC + 0.3V
ICC1	Operating VCC current			30	mA	IOUT = 0mA, f=5MHz
ICC2				50	mA	IOUT = 0mA, f=10MHz
VIL	Input Low Voltage	-0.3(NOTE 1)		0.8	V	
VIH	Input High Voltage	2.0		VCC + 0.3	V	
VOL	Output Low Voltage			0.45	V	IOL = 2.1mA
VOH1	Output High Voltage(TTL)	2.4			V	IOH = -2mA
VOH2	Output High Voltage(CMOS)	VCC-0.4			V	IOH = -100uA VCC=VCC MIN

NOTES:

1. VIL min. = -1.0V for pulse width is equal to or less than 50 ns.
   VIL min. = -2.0V for pulse width is equal to or less than 20 ns.
2. VIH max. = VCC + 1.5V for pulse width is equal to or less than 20 ns
   If VIH is over the specified maximum value, read operation cannot be guaranteed.

AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%(TA=0°C to 70°C, 5V ± 5% for MX29F001T/B-55)

		29F001T/B-70		29F001T/B-90		29F001T/B-12			
SYMBOL	**PARAMETER**	**MIN.**	**MAX.**	**MIN.**	**MAX.**	**MIN.**	**MAX.**	**UNIT**	**CONDITIONS**
tACC	Address to Output Delay		70		90		120	ns	$\overline{CE}$=$\overline{OE}$=VIL
tCE	$\overline{CE}$ to Output Delay		70		90		120	ns	$\overline{OE}$=VIL
tOE	$\overline{OE}$ to Output Delay		40		40		50	ns	$\overline{CE}$=VIL
tDF	$\overline{OE}$ High to Output Float (Note1)	0	20	0	30	0	30	ns	$\overline{CE}$=VIL
tOH	Address to Output hold	0		0		0		ns	$\overline{CE}$=$\overline{OE}$=VIL

		29F001T/B-55			
SYMBOL	**PARAMETER**	**MIN.**	**MAX.**	**UNIT**	**CONDITIONS**
tACC	Address to Output Delay		55	ns	$\overline{CE}$=$\overline{OE}$=VIL
tCE	$\overline{CE}$ to Output Delay		55	ns	$\overline{OE}$=VIL
tOE	$\overline{OE}$ to Output Delay		30	ns	$\overline{CE}$=VIL
tDF	$\overline{OE}$ High to Output Float (Note1)	0	20	ns	$\overline{CE}$=VIL
tOH	Address to Output hold	0		ns	$\overline{CE}$=$\overline{OE}$=VIL

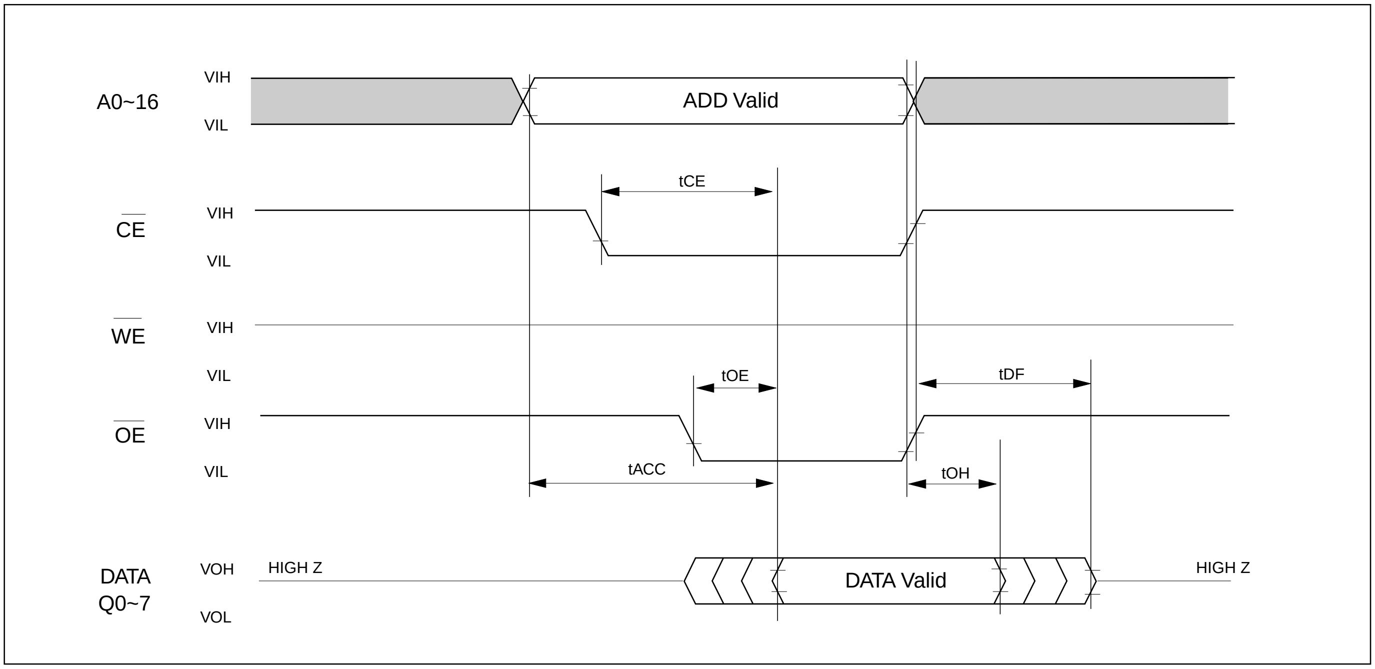
TEST CONDITIONS:

- Input pulse levels: 0.45V/2.4V for 70ns max. ; 0V/3.0V for 55ns
- Input rise and fall times: ≤ 10ns for 70ns max; ≤ 5ns for 55ns
- Output load: 1 TTL gate + 100pF (Including scope and jig) for 70ns max. ; 1 TTL gate + 30pF (Including scope and jig) for 55ns max.
- Reference levels for measuring timing : 0.8V & 2.0V for 70ns max.; 1.5V for 55ns

NOTE:

1. tDF is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

READ TIMING WAVEFORMS



COMMAND PROGRAMMING/DATA PROGRAMMING/ERASE OPERATION

DC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%(VCC = 5V ± 5% for 29F001T/B-55)

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
ICC1 (Read)	Operating VCC Current			30	mA	IOUT=0mA, f=5MHz
ICC2				50	mA	IOUT=0mA, F=10MHz
ICC3 (Program)				50	mA	In Programming
ICC4 (Erase)				50	mA	In Erase
ICCES	VCC Erase Suspend Current		2		mA	$\overline{\text{CE}}$=VIH, Erase Suspended

NOTES:

1. VIL min. = -0.6V for pulse width ≤ 20ns.
2. If VIH is over the specified maximum value, programming operation cannot be guranteed.
3. ICCES is specified with the device de-selected. If the device is read during erase suspend mode, current draw is the sum of ICCES and ICC1 or ICC2.
4. All current are in RMS unless otherwise noted.

AC CHARACTERISTICS TA = 0^{o}C to 70^{o}C, VCC = 5V ± 10%(VCC = 5V ± 5% for 29F001T/B-55)

		29F001T/B-70		29F001T/B-90		29F001T/B-12			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tOES	$\overline{\text{OE}}$ setup time	0		0		0		ns	
tCWC	Command programming cycle	70		90		120		ns	
tCEP	$\overline{\text{WE}}$ programming pulse width	45		45		50		ns	
tCEPH1	$\overline{\text{WE}}$ programming pluse width High	20		20		20		ns	
tCEPH2	$\overline{\text{WE}}$ programming pluse width High	20		20		20		ns	
tAS	Address setup time	0		0		0		ns	
tAH	Address hold time	45		45		50		ns	
tDS	Data setup time	30		45		50		ns	
tDH	Data hold time	0		0		0		ns	
tCESC	$\overline{\text{CE}}$ setup time before command write	0		0		0		ns	
tDF	Output disable time (Note 1)		30		40		40	ns	
tAETC	Total erase time in auto chip erase	3(TYP.)	24	3(TYP.)	24	3(TYP.)	24	s	
tAETB	Total erase time in auto sector erase	1(TYP.)	8	1(TYP.)	8	1(TYP.)	8	s	
tAVT	Total programming time in auto verify	7	210	7	210	7	210	us	
tBAL	Sector address load time	80		80		80		us	
tCH	$\overline{\text{CE}}$ Hold Time	0		0		0		ns	
tCS	$\overline{\text{CE}}$ setup to $\overline{\text{WE}}$ going low	0		0		0		ns	
tVLHT	Voltge Transition Time	4		4		4		us	
tOESP	$\overline{\text{OE}}$ Setup Time to $\overline{\text{WE}}$ Active	4		4		4		us	
tWPP	Write pulse width for chip protect	10		10		10		us	
tWPP2	Write pulse width for chip unprotect	12		12		12		ms	

NOTES:

1. tDF defined as the time at which the output achieves the open circuit condition and data is no longer driven.

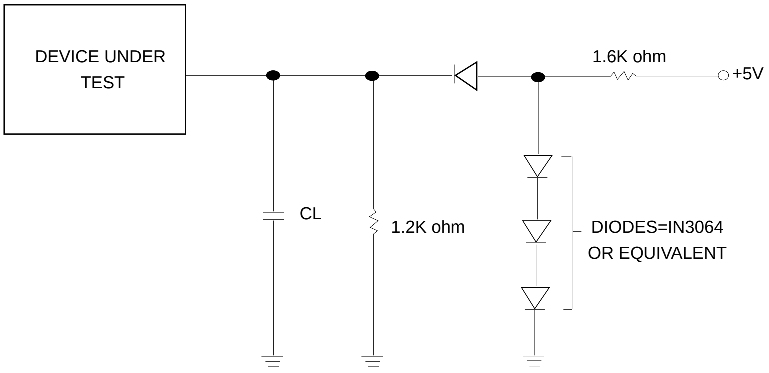
AC CHARACTERISTICS TA = 0ºC to 70ºC, VCC = 5V ± 5% for MX29F001T/B-55

		29F001T/B-55			
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
tOES	$\overline{\text{OE}}$ setup time	0		ns	
tCWC	Command programming cycle	70		ns	
tCEP	$\overline{\text{WE}}$ programming pulse width	45		ns	
tCEPH1	$\overline{\text{WE}}$ programming pluse width High	20		ns	
tCEPH2	$\overline{\text{WE}}$ programming pluse width High	20		ns	
tAS	Address setup time	0		ns	
tAH	Address hold time	45		ns	
tDS	Data setup time	20		ns	
tDH	Data hold time	0		ns	
tCESC	$\overline{\text{CE}}$ setup time before command write	0		ns	
tDF	Output disable time (Note 1)		20	ns	
tAETC	Total erase time in auto chip erase	3(TYP.)	24	s	
tAETB	Total erase time in auto sector erase	1(TYP.)	8	s	
tAVT	Total programming time in auto verify	7	210	us	
tBAL	Sector address load time	80		us	
tCH	$\overline{\text{CE}}$ Hold Time	0		ns	
tCS	$\overline{\text{CE}}$ setup to $\overline{\text{WE}}$ going low	0		ns	
tVLHT	Voltge Transition Time	4		us	
tOESP	$\overline{\text{OE}}$ Setup Time to $\overline{\text{WE}}$ Active	4		us	
tWPP	Write pulse width for chip protect	10		us	
tWPP2	Write pulse width for chip unprotect	12		ms	

NOTES:

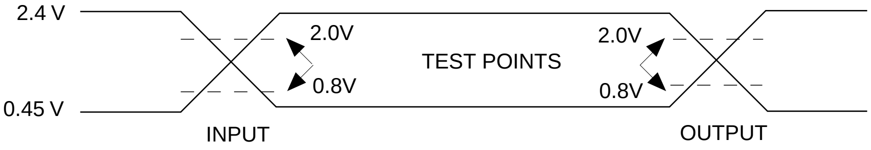
1. tDF defined as the time at which the output achieves the open circuit condition and data is no longer driven.

SWITCHING TEST CIRCUITS



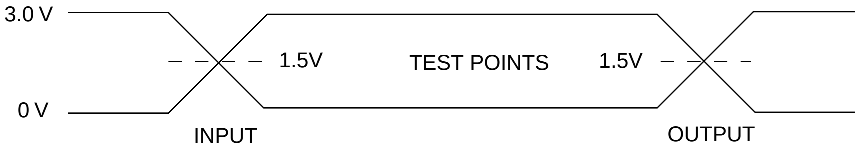
CL=100pF Including jig capacitance for 29F001T/B-70, 29F001T/B-90, 29F001T/B-12
30pF Including jig capacitance for 29F001T/B-55

SWITCHING TEST WAVEFORMS(I) for 29F001T/B-70, 29F001T/B-90, 29F001T/B-12



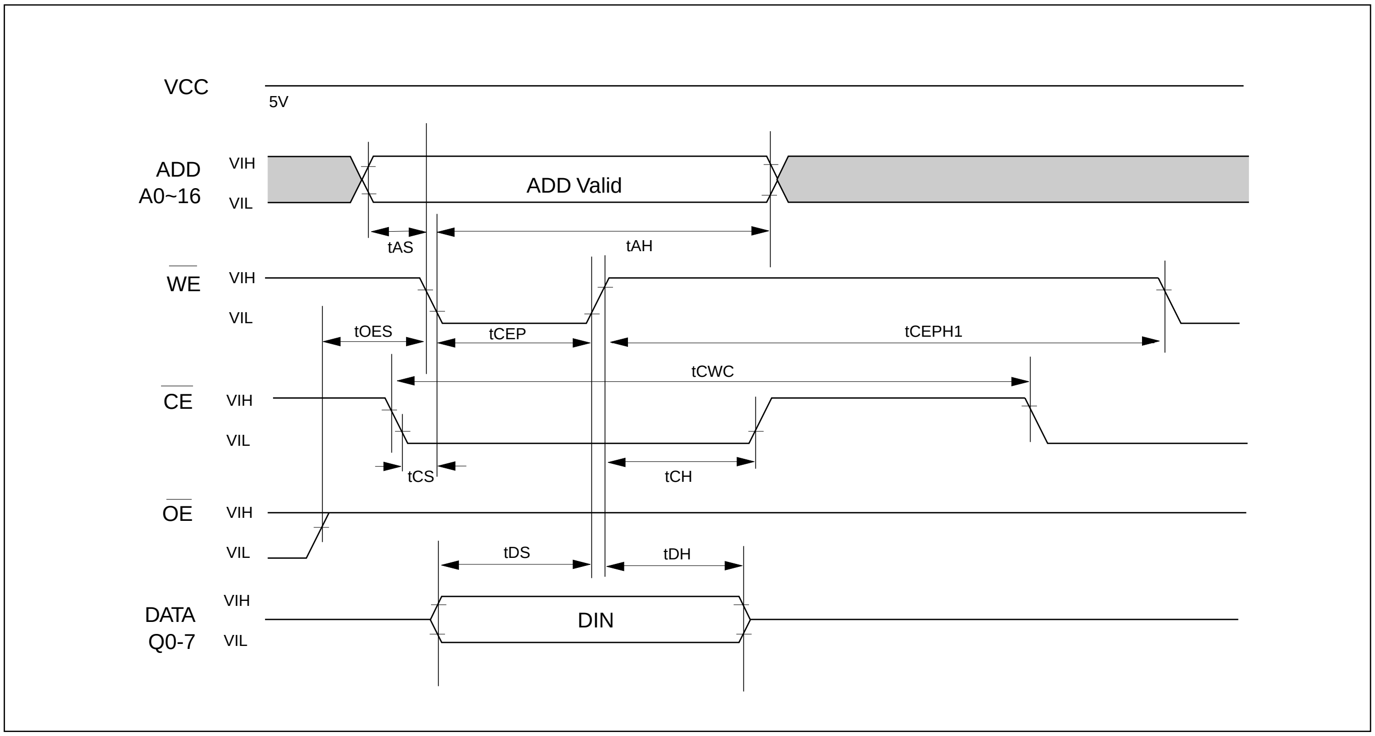
AC TESTING: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
Input pulse rise and fall times are < 10ns.

SWITCHING TEST WAVEFORMS(II) for 29F001T/B-55



AC TESTING: Inputs are driven at 3.0V for a logic "1" and 0V for a logic "0".
Input pulse rise and fall times are < 5ns.

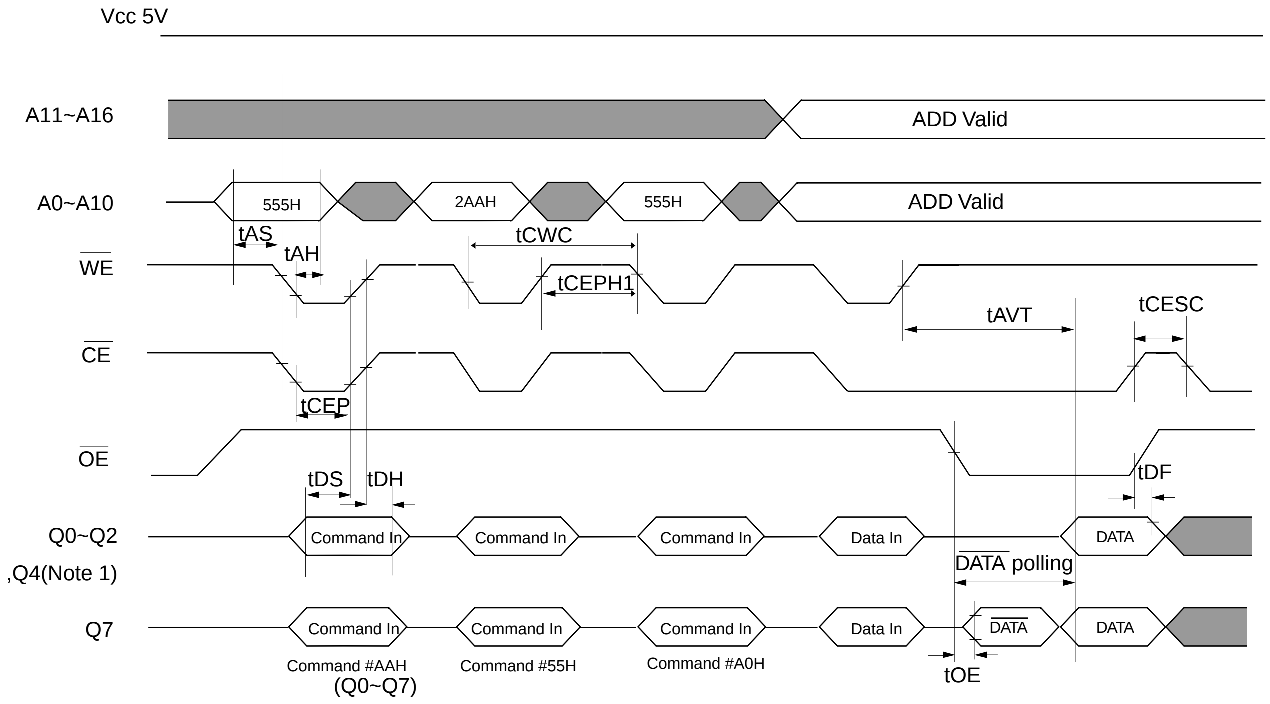
COMMAND WRITE TIMING WAVEFORM



AUTOMATIC PROGRAMMING TIMING WAVEFORM

One byte data is programmed. Verification in fast algorithm and additional programming by external control are not required because these operations are executed automatically by internal control circuit. Programming completion can be verified by DATA polling and toggle bit checking after automatic verify starts. Device outputs DATA during programming and DATA after programming on Q7.(Q6 is for toggle bit; see toggle bit, DATA polling, timing waveform)

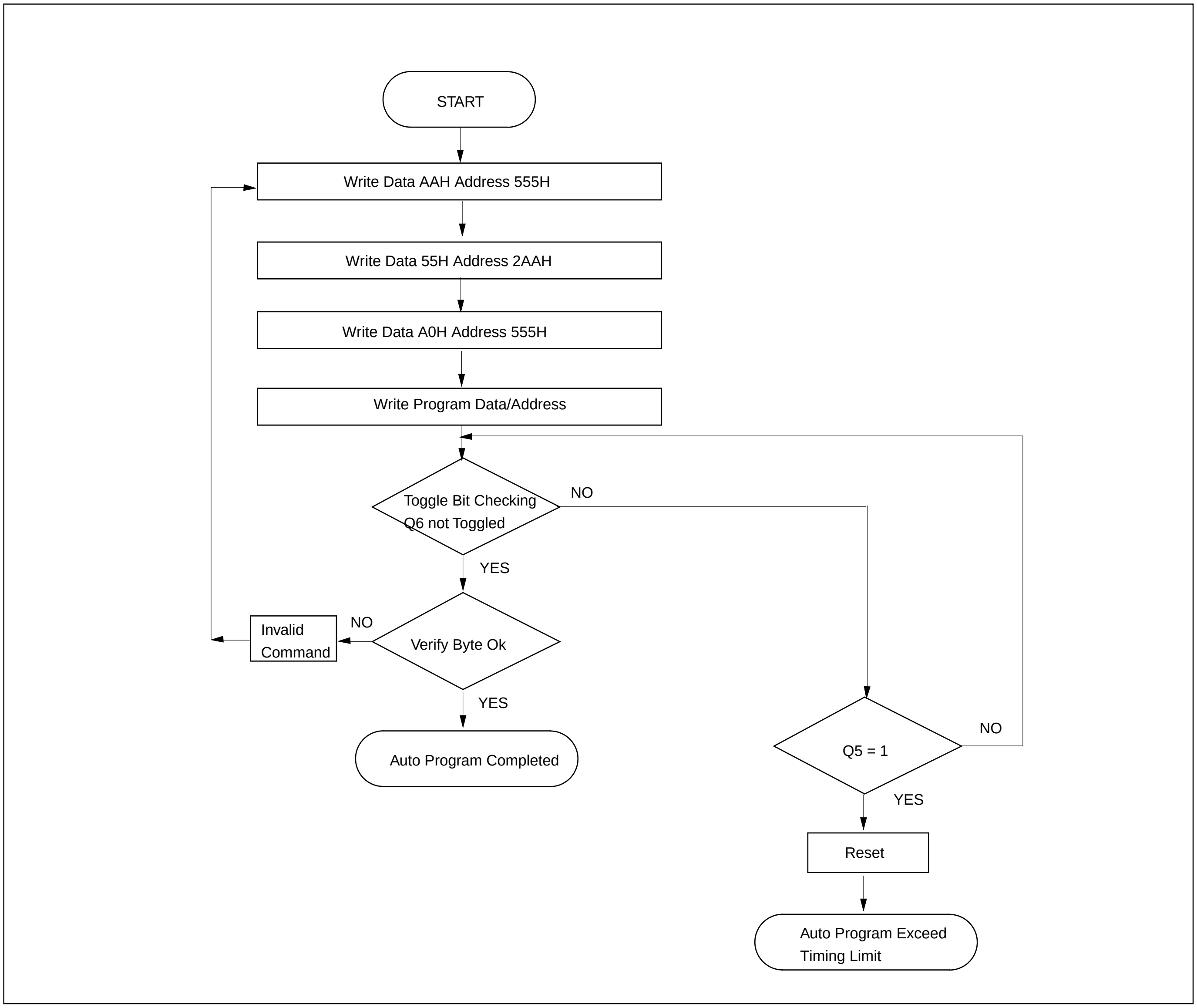
AUTOMATIC PROGRAMMING TIMING WAVEFORM



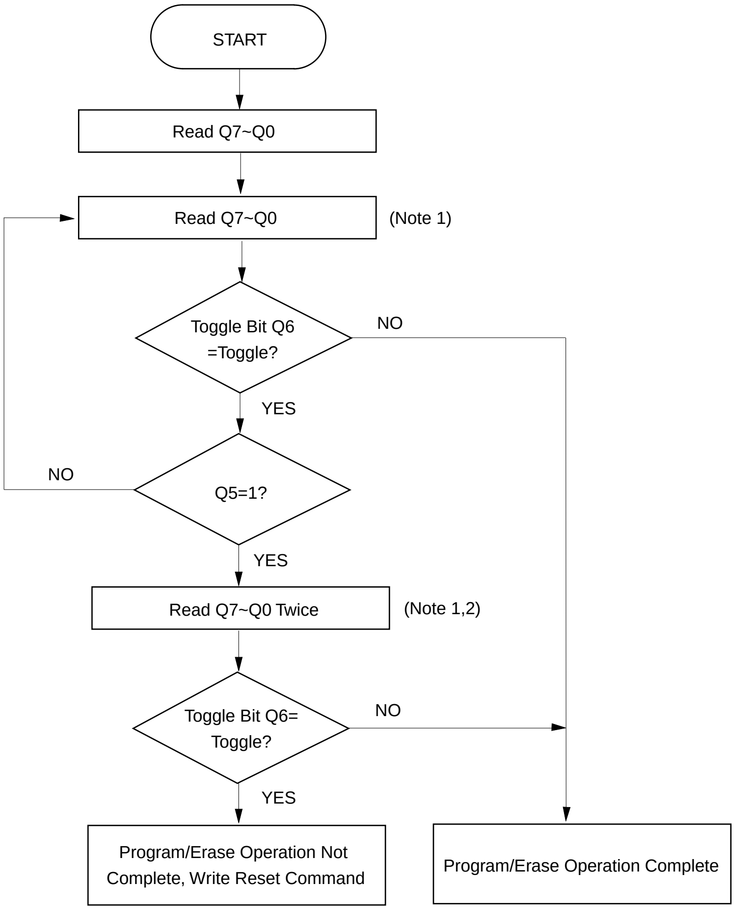
Notes:

(1). Q6:Toggle bit, Q5:Timing-limit bit, Q3: Time-out bit

AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART



TOGGLE BIT ALGORITHM



Notes:

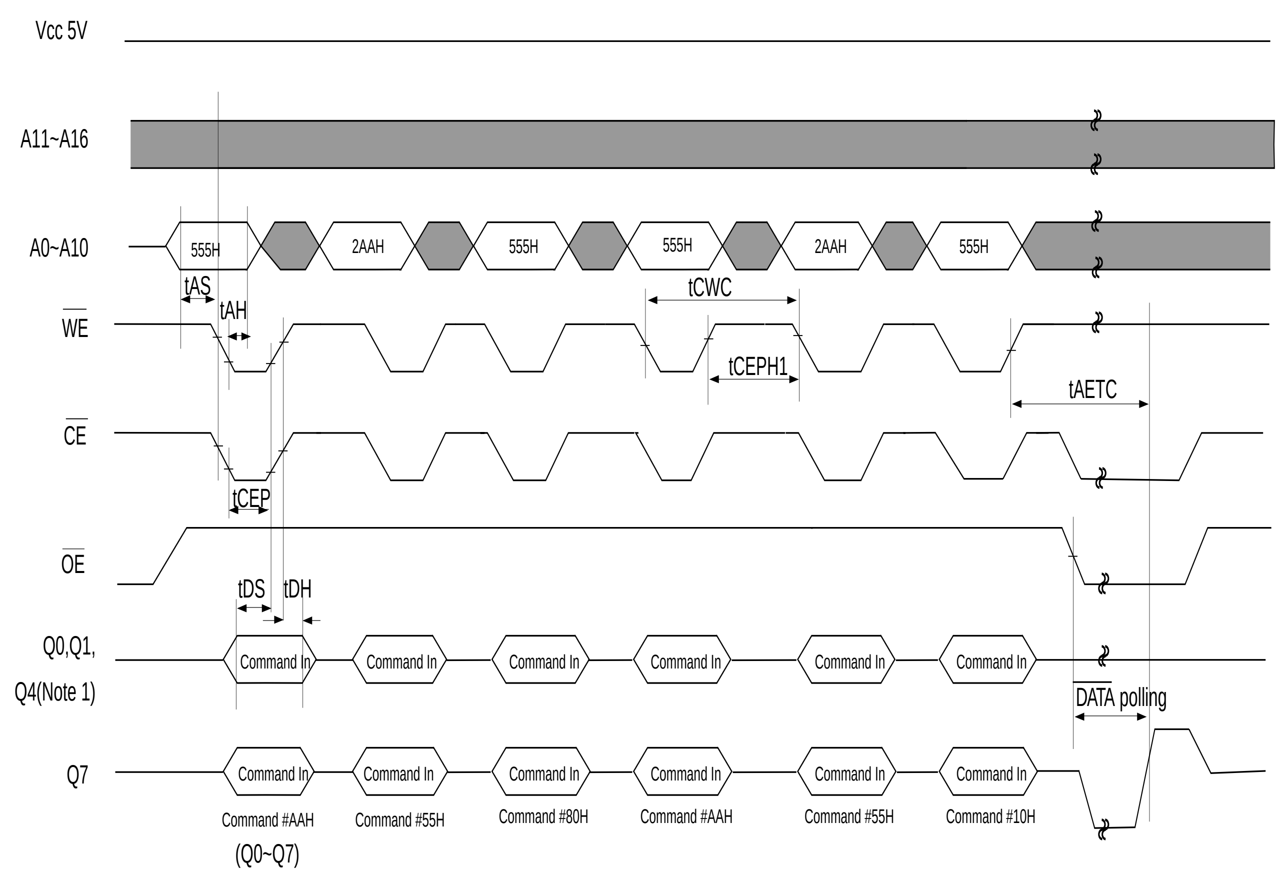
1.Read toggle bit Q6 twice to determine whether or not it is toggle. See text.

2.Recheck toggle bit Q6 because it may stop toggling as Q5 changes to "1". See text.

AUTOMATIC CHIP ERASE TIMING WAVEFORM

All data in chip are erased. External erase verification is not required because data is erased automatically by internal control circuit. Erasure completion can be verified by $\overline{\text{DATA}}$ polling and toggle bit checking after auto matic erase starts. Device outputs 0 during erasure and 1 after erasure 0n Q7.(Q6 is for toggle bit; see toggle bit, $\overline{\text{DATA}}$ polling, timing waveform)

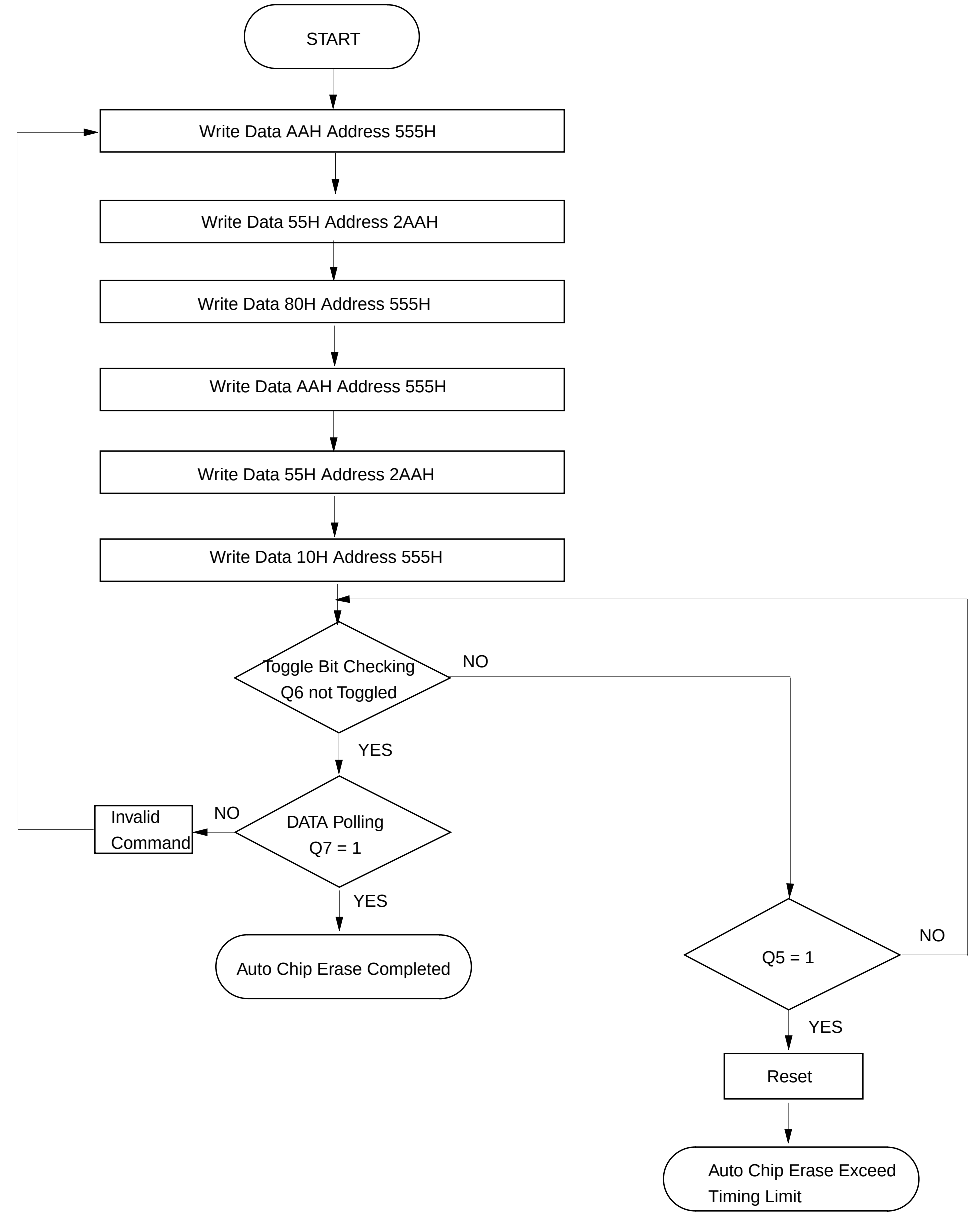
AUTOMATIC CHIP ERASE TIMING WAVEFORM



Notes:

(1). Q6:Toggle bit, Q5:Timing-limit bit, Q3: Time-out bit, Q2: Toggle bit

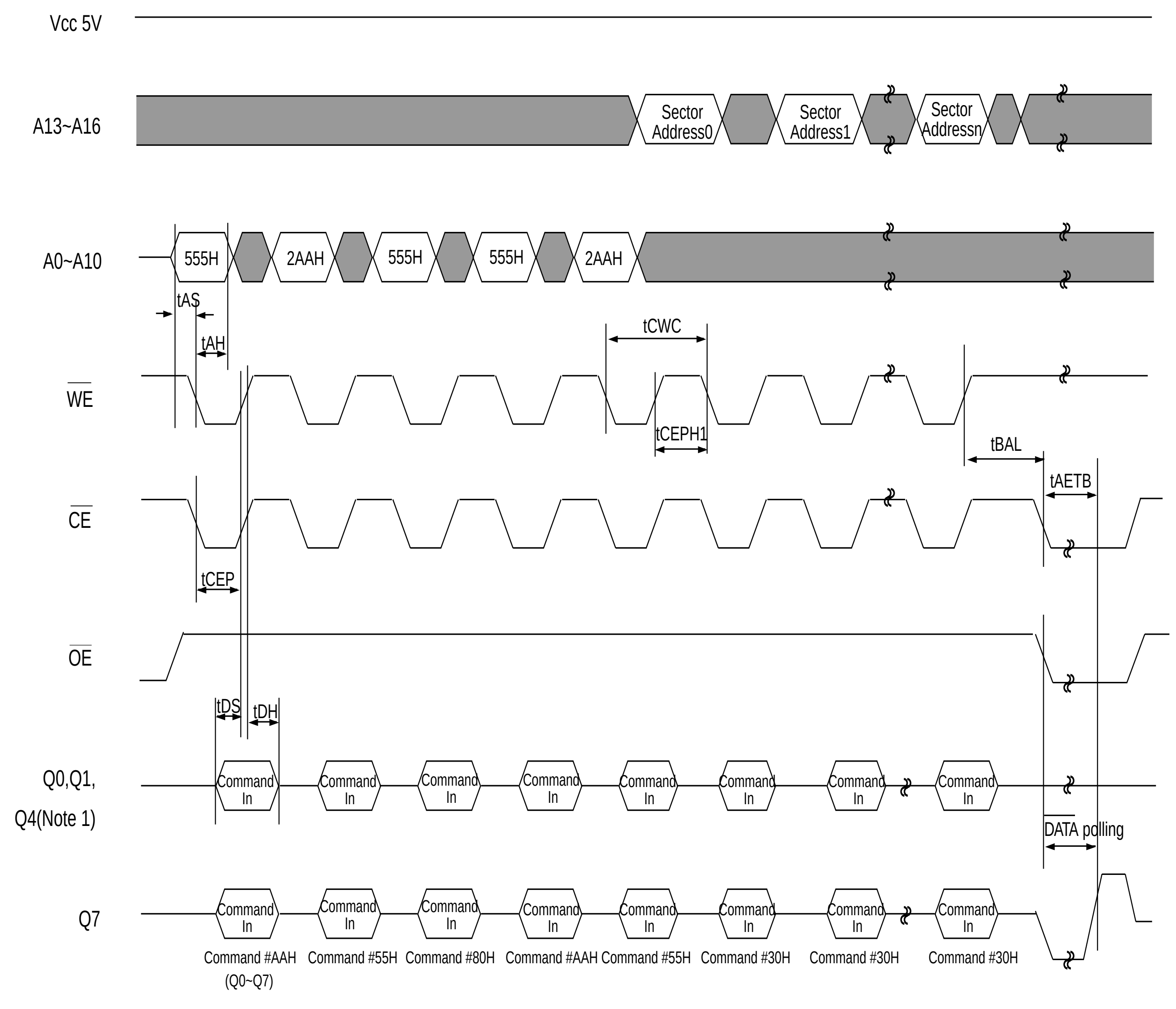
AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART



AUTOMATIC SECTOR ERASE TIMING WAVEFORM

Sector data indicated by A13 to A16 are erased. External erase verify is not required because data are erased automatically by internal control circuit. Erasure completion can be verified by $\overline{\text{DATA}}$ polling and toggle bit checking after automatic erase starts. Device outputs 0 during erasure and 1 after erasure on Q7.(Q6 is for toggle bit; see toggle bit, $\overline{\text{DATA}}$ polling, timing waveform)

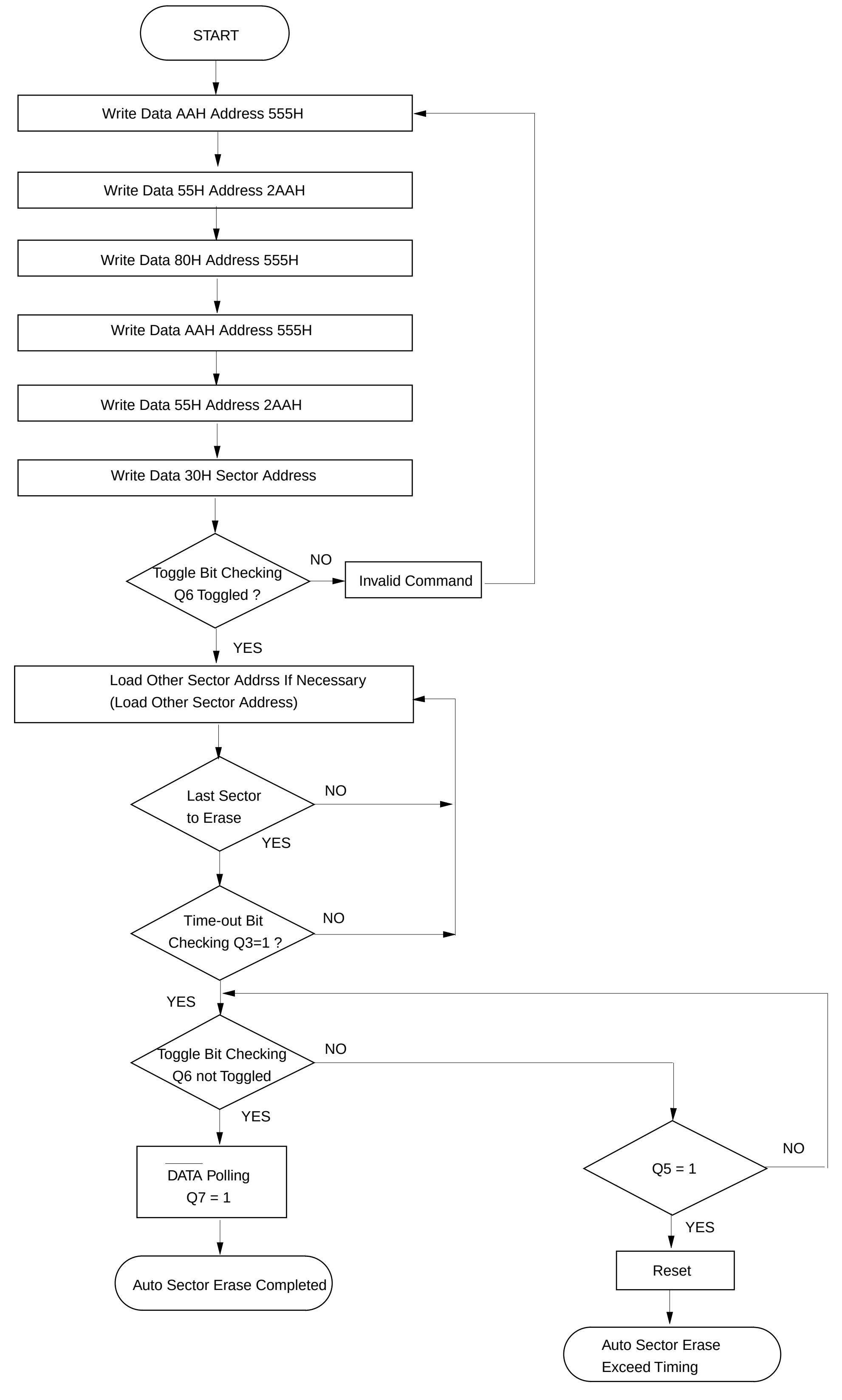
AUTOMATIC SECTOR ERASE TIMING WAVEFORM



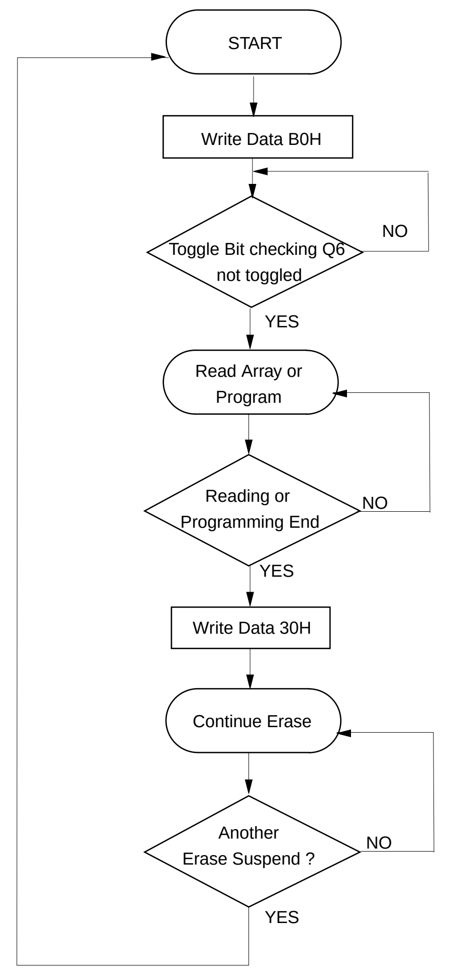
Notes:

(1). Q6:Toggle bit, Q5:Timing-limit bit, Q3: Time-out bit, Q2: Toggle bit

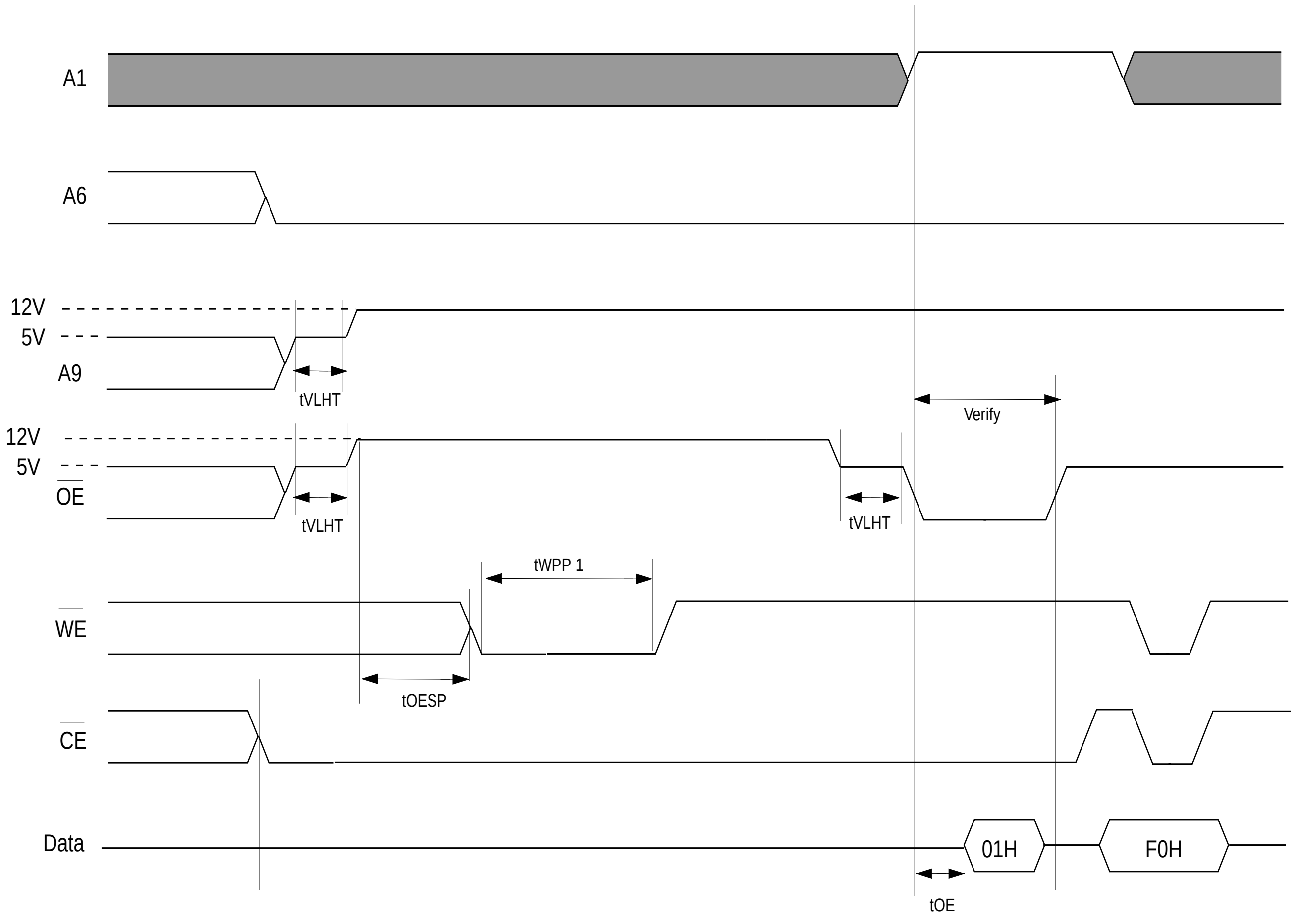
AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART



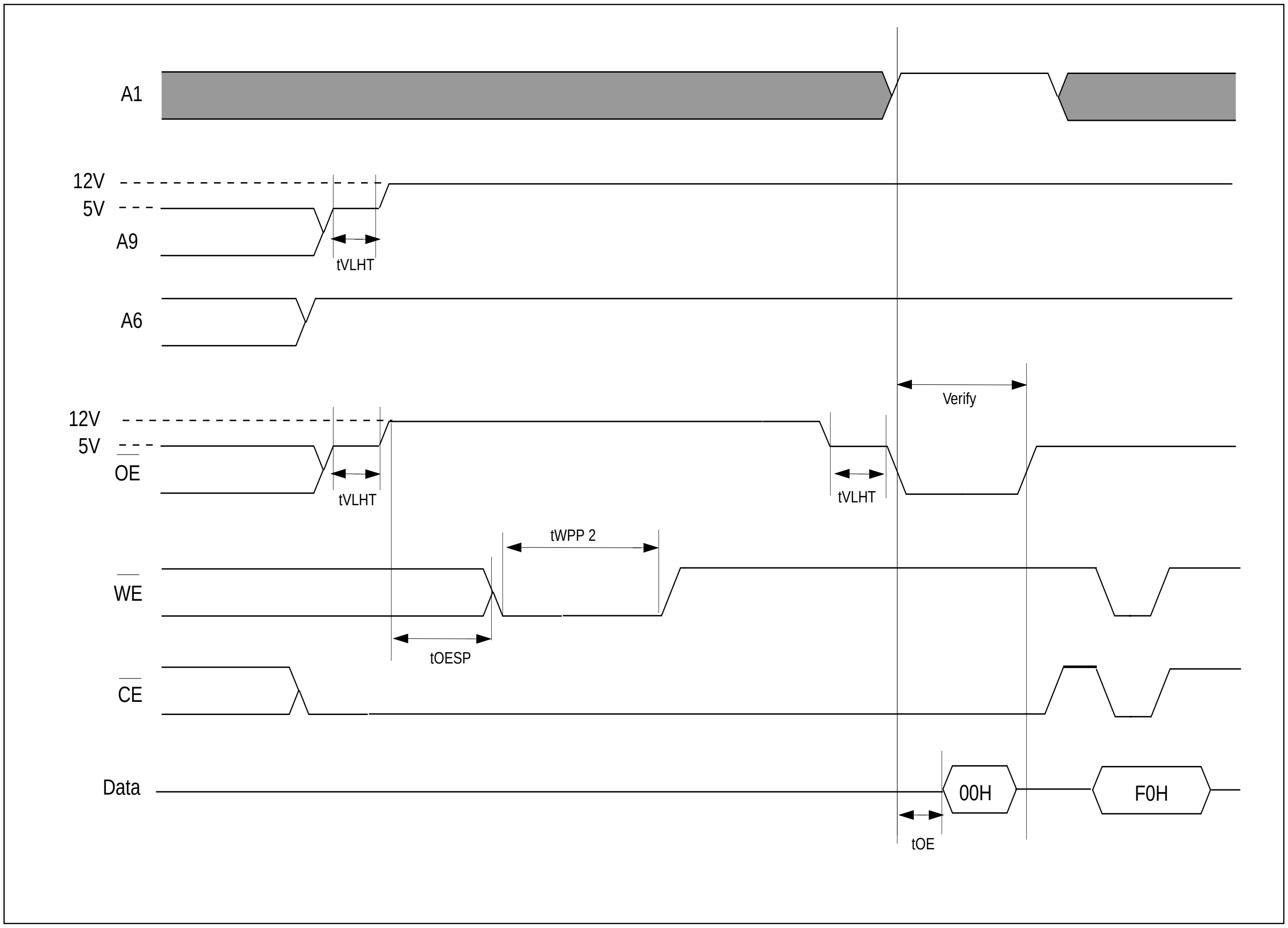
ERASE SUSPEND/ERASE RESUME FLOWCHART



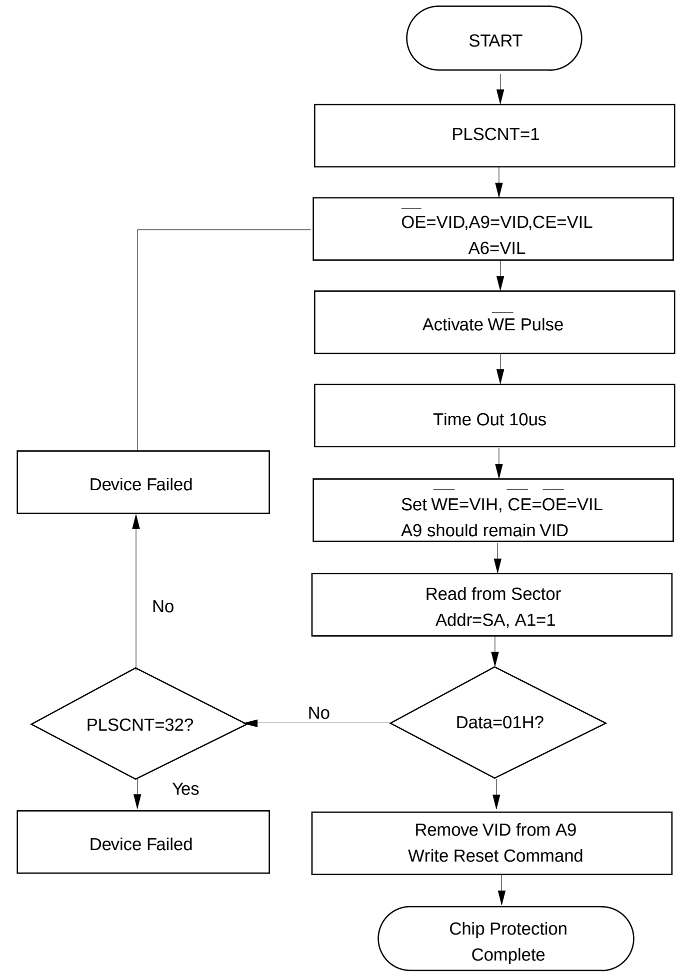
TIMING WAVEFORM FOR CHIP PROTECTION FOR SYSTEM WITH 12V



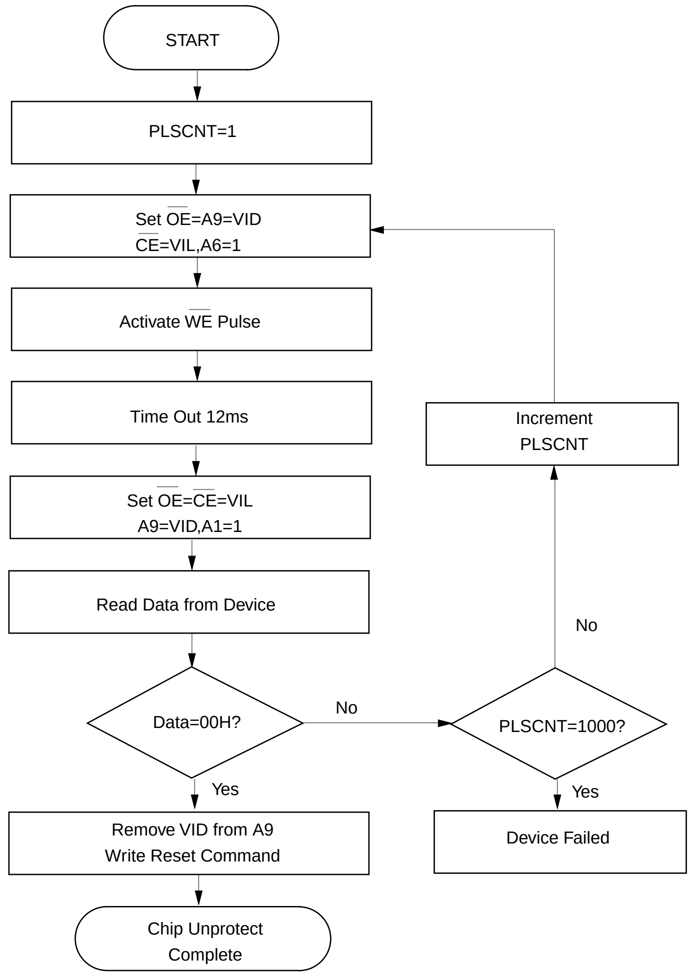
TIMING WAVEFORM FOR CHIP UNPROTECTION FOR SYSTEM WITH 12V



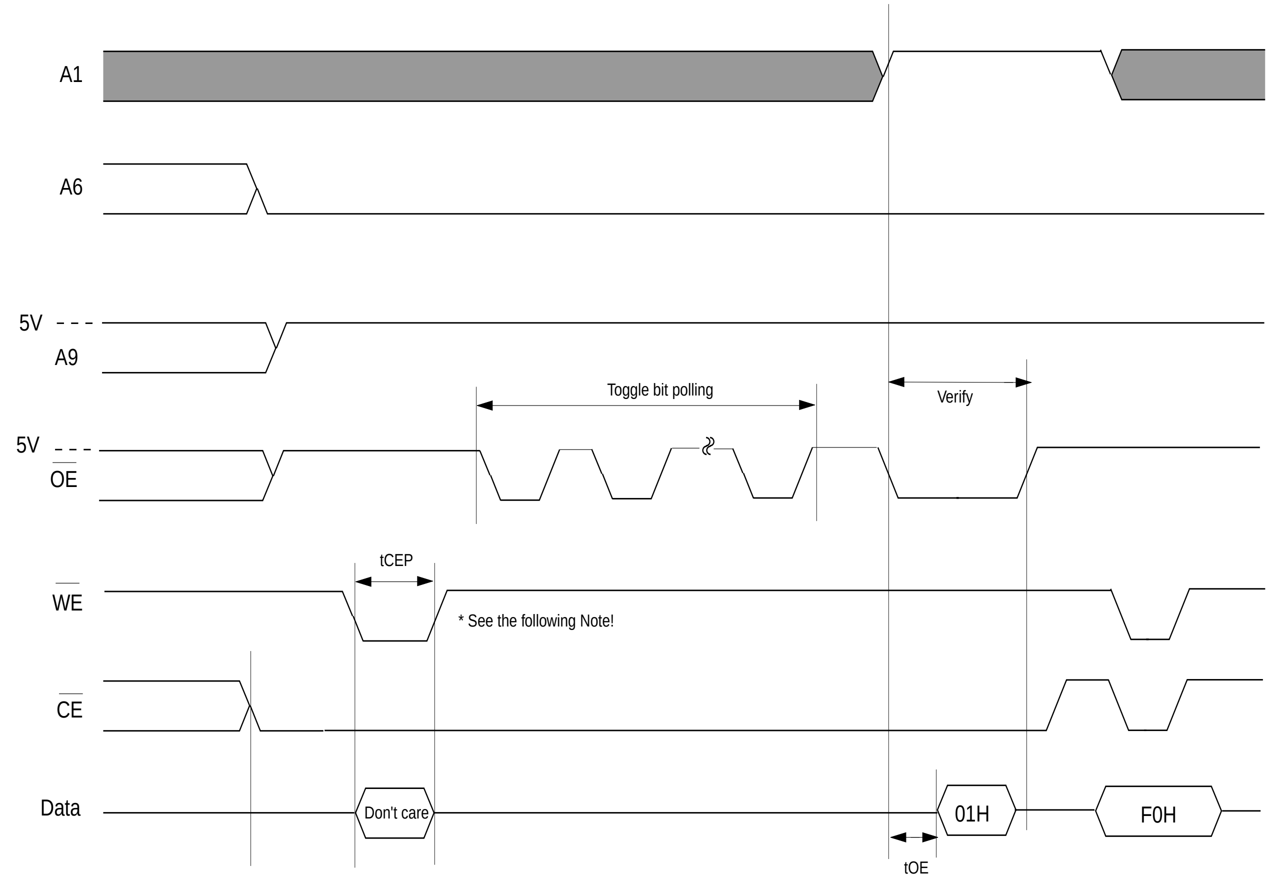
CHIP PROTECTION ALGORITHM FOR SYSTEM WITH 12V



CHIP UNPROTECTION ALGORITHM FOR SYSTEM WITH 12V

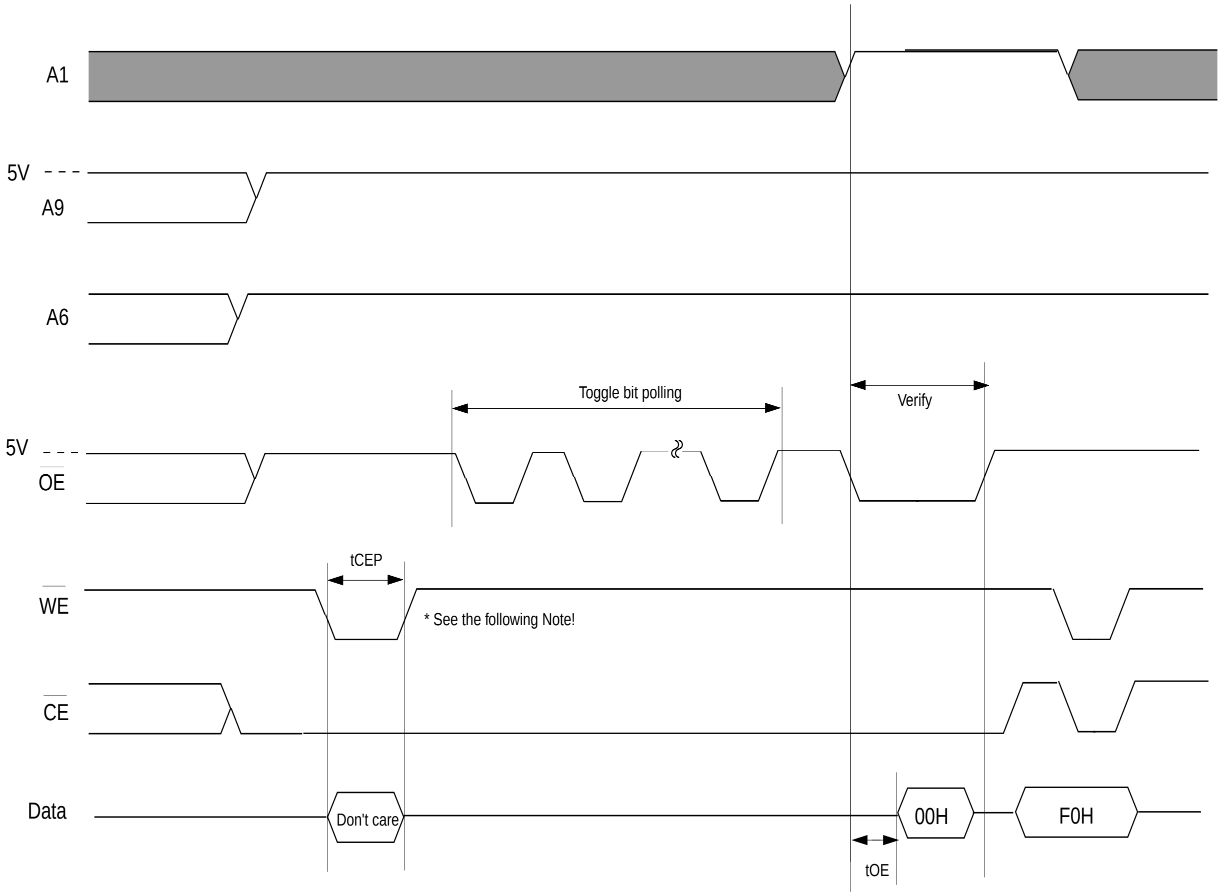


TIMING WAVEFORM FOR CHIP PROTECTION FOR SYSTEM WITHOUT 12V



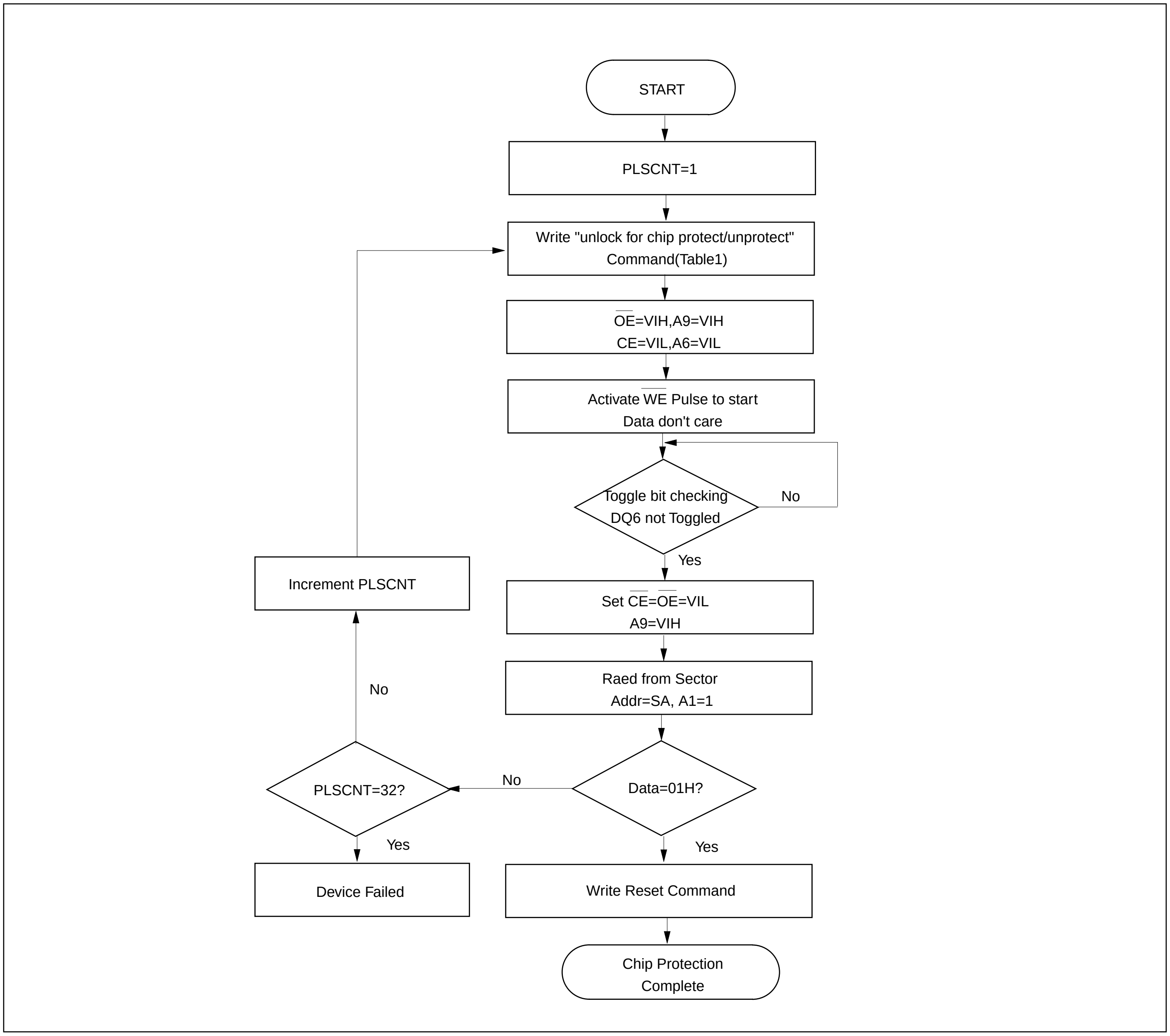
Note: Must issue "unlock for sector protect/unprotect" command
before chip protection for a system without 12V provided.

TIMING WAVEFORM FOR CHIP UNPROTECTION FOR SYSTEM WITHOUT 12V

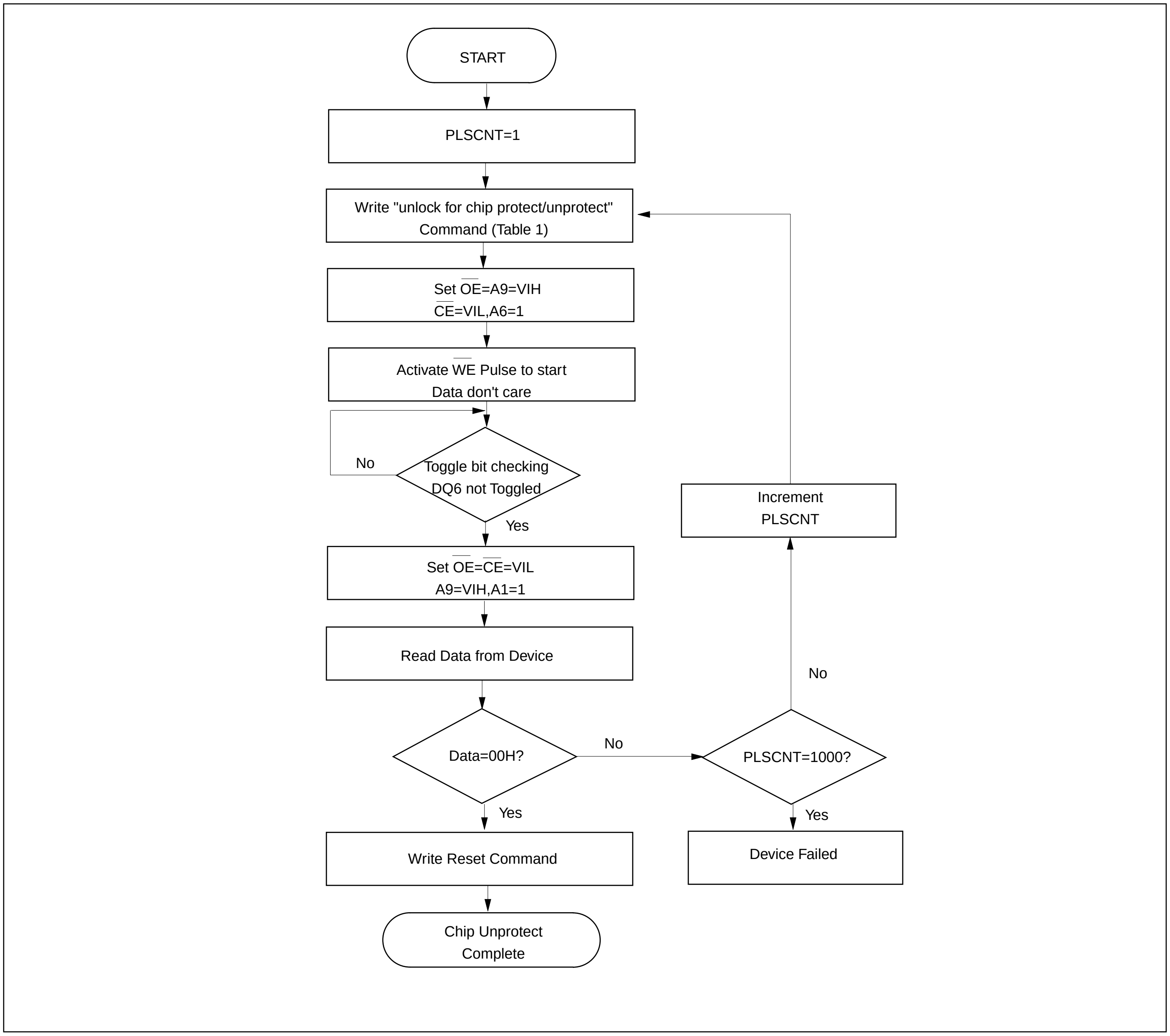


Note: Must issue "unlock for sector protect/unprotect" command before chip unprotection for a system without 12V provided.

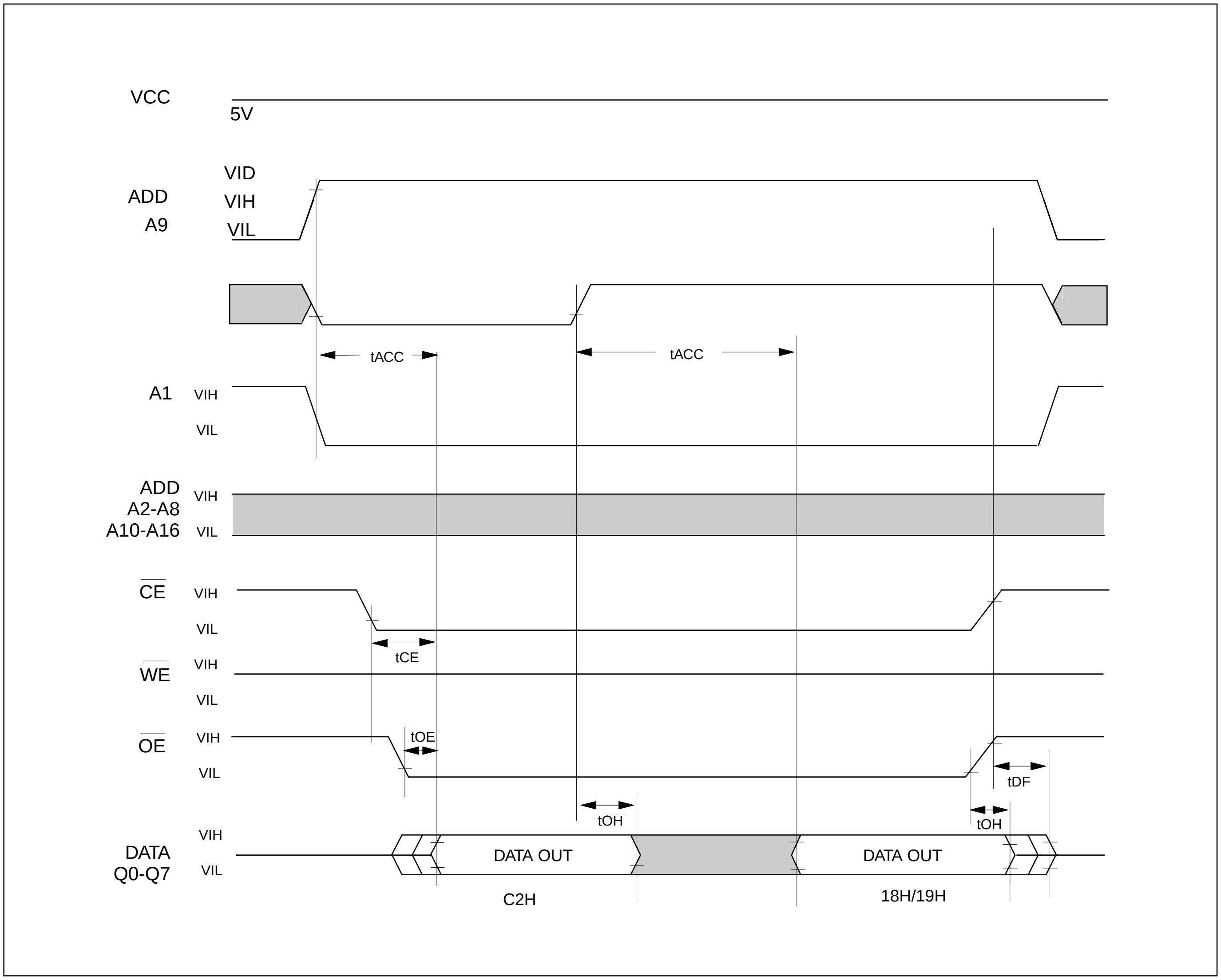
CHIP PROTECTION ALGORITHM FOR SYSTEM WITHOUT 12V



CHIP UNPROTECTION ALGORITHM FOR SYSTEM WITHOUT 12V



ID CODE READ TIMING WAVEFORM



ORDERING INFORMATION

PLASTIC PACKAGE (Top Boot Sector as an sample For Bottom Boot Sector ones,MX29F001Txx will change to MX29F001Bxx)

PART NO.	ACCESS TIME (ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(uA)	PACKAGE
MX29F001TQC-55	55	30	5	32 Pin PLCC
MX29F001TQC-70	70	30	5	32 Pin PLCC
MX29F001TQC-90	90	30	5	32 Pin PLCC
MX29F001TQC-12	120	30	5	32 Pin PLCC
MX29F001TTC-55	55	30	5	32 Pin TSOP (Normal Type)
MX29F001TTC-70	70	30	5	32 Pin TSOP (Normal Type)
MX29F001TTC-90	90	30	5	32 Pin TSOP (Normal Type)
MX29F001TTC-12	120	30	5	32 Pin TSOP (Normal Type)
MX29F001TPC-55	55	30	5	32 Pin PDIP
MX29F001TPC-70	70	30	5	32 Pin PDIP
MX29F001TPC-90	90	30	5	32 Pin PDIP
MX29F001TPC-12	120	30	5	32 Pin PDIP

ERASE AND PROGRAMMING PERFORMANCE(1)

PARAMETER	LIMITS			UNITS
	MIN.	TYP.(2)	MAX.(3)	
Sector Erase Time		1	8	s
Chip Erase Time		3	24	s
Byte Programming Time		7	210	us
Chip Programming Time		3.5	10.5	sec
Erase/Program Cycles	10,000			Cycles

Note: 1.Not 100% Tested, Excludes external system level over head.
2.Typical values measured at 25℃,5V.
3.Maxi,um values measured at 25℃,4.5V.

LATCHUP CHARACTERISTICS

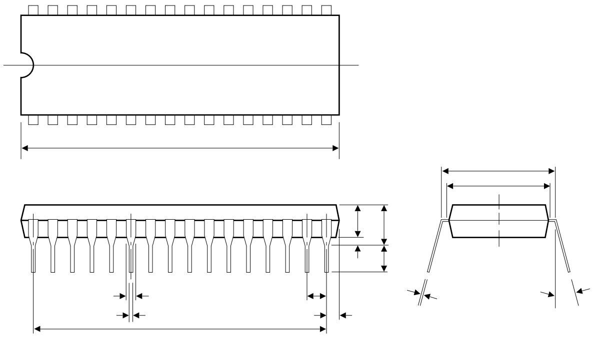
	MIN.	MAX.
Input Voltage with respect to GND on all pins except I/O pins	-1.0V	13.5V
Input Voltage with respect to GND on all I/O pins	-1.0V	Vcc + 1.0V
Current	-100mA	+100mA
Includes all pins except Vcc. Test conditions: Vcc = 5.0V, one pin at a time.		

PACKAGE INFORMATION

32-PIN PLASTIC DIP

ITEM	MILLIMETERS	INCHES
A	42.13 max.	1.660 max.
B	1.90 [REF]	.075 [REF]
C	2.54 [TP]	.100 [TP]
D	.46 [Typ.]	.050 [Typ.]
E	38.07	1.500
F	1.27 [Typ.]	.050 [Typ.]
G	3.30 ± .25	.130 ± .010
H	.51 [REF]	.020 [REF]
I	3.94 ± .25	1.55 ± .010
J	5.33 max.	.210 max.
K	15.22 ± .25	.600 ± .101
L	13.97 ± .25	.550 ± .010
M	.25 [Typ.]	.010 [Typ.]

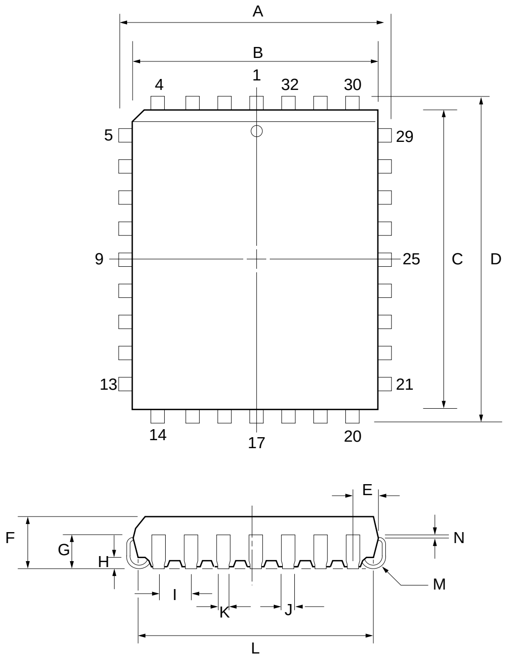
NOTE: Each lead certerline is located within .25mm[.01 inch] of its true position [TP] at a maximum at maximum material condition.



32-PIN PLASTIC LEADED CHIP CARRIER (PLCC)

ITEM	MILLIMETERS	INCHES
A	12.44 ± .13	.490 ± .005
B	11.50 ± .13	.453 ± .005
C	14.04 ± .13	.553 ± .005
D	14.98 ± .13	.590 ± .005
E	1.93	.076
F	3.30 ± .25	.130 ± .010
G	2.03 ± .13	.080 ± .005
H	.51 ± .13	.020 ± .005
I	1.27 [Typ.]	.050 [Typ.]
J	.71 [REF]	.028 [REF]
K	.46 [REF]	.018 [REF]
L	10.40/12.94 (W) (L)	.410/.510 (W) (L)
M	.89R	.035R
N	.25[Typ.]	.010[Typ.]

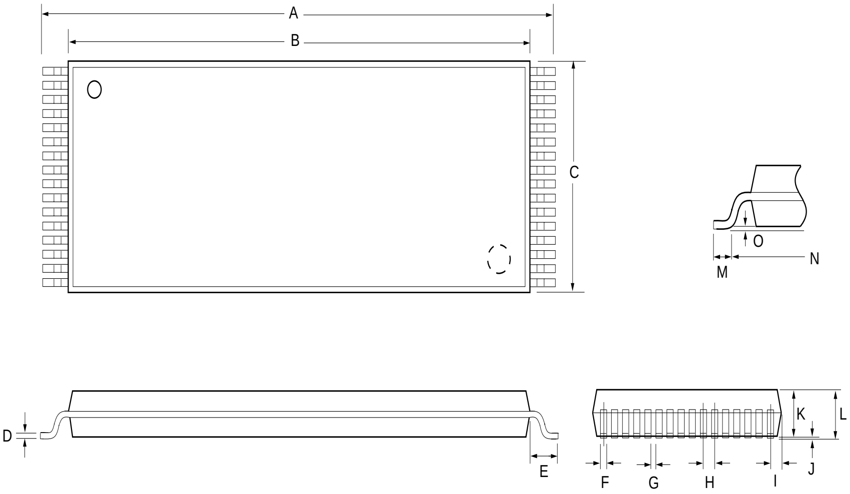
NOTE: Each lead certerline is located within .25mm[.01 inch] of its true position [TP] at a maximum at maximum material condition.



32-PIN PLASTIC TSOP

ITEM	MILLIMETERS	INCHES
A	20.0 ± .20	.078 ± .006
B	18.40 ± .10	.724 ± .004
C	8.20 max.	.323 max.
D	0.15 [Typ.]	.006 [Typ.]
E	.80 [Typ.]	.031 [Typ.]
F	.20 ± .10	.008 ± .004
G	.30 ± .10	.012 ± .004
H	.50 [Typ.]	.020 [Typ.]
I	.45 max.	.018 max.
J	0 ~ .20	0 ~ .008
K	1.00 ± .10	.039 ± .004
L	1.27 max.	.050 max.
M	.50	.020
N	0 ~5°	.500

NOTE: Each lead certerline is located within .25mm[.01 inch] of its true position [TP] at a maximum at maximum material condition.



REVISION HISTORY

Revision No.	Description	Page	Date
1.1	Update Block Erase Timing Waveform	P23	APR/16/1998
1.2	Update		AMY/08/1998
	1)Timing waveform for sector unprotection for system with 12V	P26	
	2)Sector protection algorithm for system with 12V	P27	
	3)Timing waveform for sector protection/unprotection for system without 12V	P29	
	4)Sector protection algorithm for system wothout 12V	P30	
	5)Sector unprotection algorithm for system wothout 12V	P31	
1.3	Update		JUN/11/1998
	1)Erase suspend and erase resume	P1	
	2)Sector protect/unprotect for 5V only system	P1, 8	
	3)Typing value of ICCES in DC Characteristic table	P15	
	4)Minimum value of tAVT(Total Progaming time in auto verify) in DC Characteristic table	P15	
	5)ID code read timing waveform	P32	
1.4	This product is featured with function of chip protect/unprotect.		JUL/28/1998
1.5	Chip Protect Verification is added on the software command table		AUG/18/1998
1.6	Modify the block diagram		AUG/28/1998
1.7	Modify the Q3 status into "0" for Exceeded Time Limits in Write Operation Status table	P9	SEP/10/1998
1.8	1)Modify Table 4. Write operation status table	P9	OCT/20/1998
1.9	2)Change IOH value at DC CHARACTERISTICS	P13	NOV/09/1998
	3)Change resistance value at SWITCHING TEST CIRCUITS	P17	
1.9.1	1)Modify Table 1 software command definitions	P5	DEC/09/1998
	2)Modify "Chip Protection with 12V system " section	P12	
	3)Correct typing error	P27,28,30,31	
1.9.2	1)Modify "Automatic Programming Timing Waveform"	P18	DEC/17/1998
	2)Modify "Toggle Bit Algorithm	P20	
1.9.3	1)Insert the 45/55ns section	P13,14,15,16, P17,33	JAN/25/1999
	2)Correct typing error	P29	
	3)Cancel Pin Configurations:Reverse type TSOP	P2	
	4)Modify Table1"Softwave command definitions"	P5	
	5)Modify Table 4" Write operation status"	P9	
	6)Modify AC CHARACTERISTICS Table "tOES" value	P16	
	7)Modify Timing waveform	P20,23,25	
1.9.4	1)Remove 45ns speed grade	P1,14,17,18,35	FEB/04/1999
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1.9.5	Modify "Chip protection for system without 12V" Timing waveform	P31	FEB/25/1999
1.9.6	Modify Ordering Information	P35	MAR/05/1999
1.9.7	Modify erase/program cycle from 100,000 to 10,000	P1	MAY/05/1999
	Modify naming "block" --> "sector"	P1,2,4,8,16,17 25,26	
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	Insert "CIN2" section to capacitance table & "VOH2" section to DC characteristics table	P13	
	Modify AC characteristics table VCC range for MX29F001T/B-55	P14,17	
	Modify Automatic chip/sector erase timing waveform	P23,25	
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1.9.8	ICC1 change to 40mA@5MHz	P1,13,15,37	MAY/17/1999
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	tCWC change to 70ns for 29F001T/B-55	P17	
	tCEP change to 45ns for 29F001T/B-55&29F001T/B-70	P16,17	
	Supplement "Note 3" for "Erase and Programming Performance"table	P38	
1.9.9	1)Active currect was improved from 40mA @5MHz to 30mA @5MHz	P1,13,15,37	JUL/12/1999
	2)Correct typing error	P5	
	3)To correct "Table 4" write Operation Status	P9	

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