National Semiconductor

PRELIMINARY
August 1983

MA2732 8k-Byte CMOS UVPROM/RAM Module

General Description

The MA2732 8k-byte CMOS UVPROM module is a member of the MA2000 series family. It provides a standard modular macrocomponent package and bus interconnect facility for industry-standard 27C16 or 27C32 UVPROMs. The module provides two standard sockets for the packaged parts. The UVPROMs are selected and programmed by the user and then simply inserted into the sockets provided in the MA2732 module. The MA2732 can be configured by the user in PROM capacities of 2k-bytes, 4k-bytes or 8k-bytes at the user's option. The MA2732 is designed such that if the user needs only one of the two sockets for program memory the remaining socket can be populated with a 2k x 8 CMOS RAM to obtain additional data memory. The internal macrobus provides for simple integration of the MA2732 with other members of the MA2000 family. Key features of this module include a complete UVPROM subsystem, self-contained memory map selection logic, opcode, decode and wait-state generator, and output buffered single 5V operation.

Features

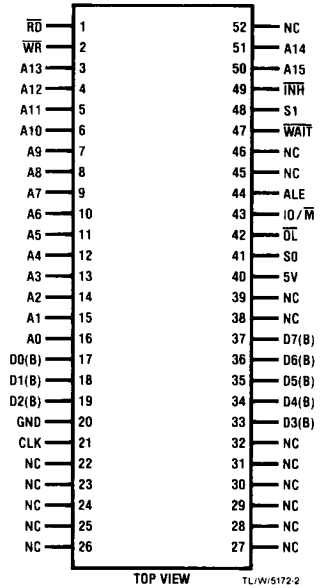
- Complete UVPROM subsystem
- Configurable as either 2k, 4k or 8k-bytes of ROM or 2/4k ROM and 2k RAM
- User selectable jumpers for memory mapping
- Internal user selectable wait-state generator
- Buffered data outputs
- Low power—when using two NMC27C32 EPROMs for a full 8k-bytes
- Sockets will accept any of the popular 24-pin ROMs/RAMs
- When the module is not selected it is automatically placed in standby mode (10 mW max using two NMC27C32s)
- Single 5V operation
- Unique stackable module

Applications

- Portable terminals
- Hand-held devices
- Pos terminals
- Remote instrumentation
- Process controllers
- Microcomputer memory

Connection Diagram

Dual-In-Line Package



TOP VIEW TL/W/5172-2

NC = no connection

Pin Names

$\overline{RD}$	Read strobe input
A0-A15	Address inputs
D0-D7	Data outputs (buffered)
CLK	Clock input
S0-S1	Status inputs
$\overline{OL}$	Overlay input
IO/$\overline{M}$	Input/output memory input
ALE	Address latch enable input
$\overline{INH}$	Inhibit input
5V	Power supply input
GND	Digital GND
$\overline{WR}$	Write strobe input

IM-B30M83/Printed in U.S.A.

Absolute Maximum Ratings

V_{CC} Supply Voltage	6.0V	Ambient Operating Temperature	−40°C to +85°C
Voltage at Any Pin Relative to GND	GND −0.3V to V_{CC} +0.3V	Storage Temperature	−55°C to +100°C
		Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics $T_A = +25°C$, $V_{CC} = 5V \pm 10\%$, GND = 0 unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		3.5			V
I_{IN}	Input Leakage A11-A15, $\overline{INH}$, CLK, $\overline{RD}$, $\overline{WR}$	$V_{IN} = 0$ to V_{CC} (Note 1)	−100	1	100	μA
I_{IN}	Input Current (Internal Pull-Up Resistors) $\overline{OL}$, E1-E6, IO/$\overline{M}$	$V_{IN} = 0.4V$	100		25	μA
I_{IN}	Input Current (Internal Pull-Down Resistors) ALE, S1, S0	$V_{IN} = 2.4V$	25		100	μA
V_{OL}	Output Low Voltage D0-D7	$I_O = 2.0$ mA			0.4	V
V_{OH}	Output High Voltage D0-D7	$I_O = -2.0$ mA	2.4			V
V_{OL}	Output Low Voltage $\overline{WAIT}$	$I_O = 3.0$ mA			0.4	V
V_{OH}	Output High Voltage $\overline{WAIT}$	$I_O = -1.0$ mA	2.4			V
I_{CC}	Supply Current	$V_{IN} = V_{CC}$ Outputs Open			600 (Note 2)	μA

Control Timing Diagram

Symbol	Parameter	Conditions	Typ	Units
t_{AVDV}	Valid Address to Valid Data		105	ns
t_{AXDZ}	Address to Data Hi-Z		120	ns
t_{AVEL}	Valid Address to Chip Enable		25	ns
t_{AXEH}	Address to Chip Disable		35	ns
t_{CVDV}	Valid Control Lines to Valid Data	$\overline{INH}$ = E5; IO/$\overline{M}$ = V_{IL}; $\overline{OL}$ = V_{IH}	100	ns
t_{CXDZ}	Control Line to Data Hi-Z	$\overline{INH}$ = E5; IO/$\overline{M}$ = V_{IH}; $\overline{OL}$ = V_{IL}	115	ns
t_{CVEL}	Valid Control Lines to Chip Enable	Same as for t_{CVDV}	25	ns
t_{CXEH}	Control Line to Chip Disable	Same as for t_{CXDZ}	35	ns
t_{WLDV}	$\overline{WR}$ Low to Data Valid Data		125	ns
t_{WHDZ}	$\overline{WR}$ High to Data Hi-Z		75	ns
t_{RLDV}	$\overline{RD}$ Low to Data Valid		125	ns
t_{RHDZ}	$\overline{RD}$ High to Data Hi-Z		75	ns
t_{PD}	Propagation Delay		50	ns
FOR MA2800 INTERFACE ONLY				
TAVQV	Valid Address to Valid Output (Note 3)		≤450	ns
TELQV	Chip Enable to Valid Output (Note 3)		≤450	ns
TOLQV	Output Enable ($\overline{RD}$) to Valid Output (Note 3)		≤120	ns
TQVWH	Output Valid to $\overline{WR}$ High		≤400	ns
TQVEH	Output Valid to $\overline{CE}$ High		≤500	ns
TELEH	Enable Strobe Width		≤1	μs

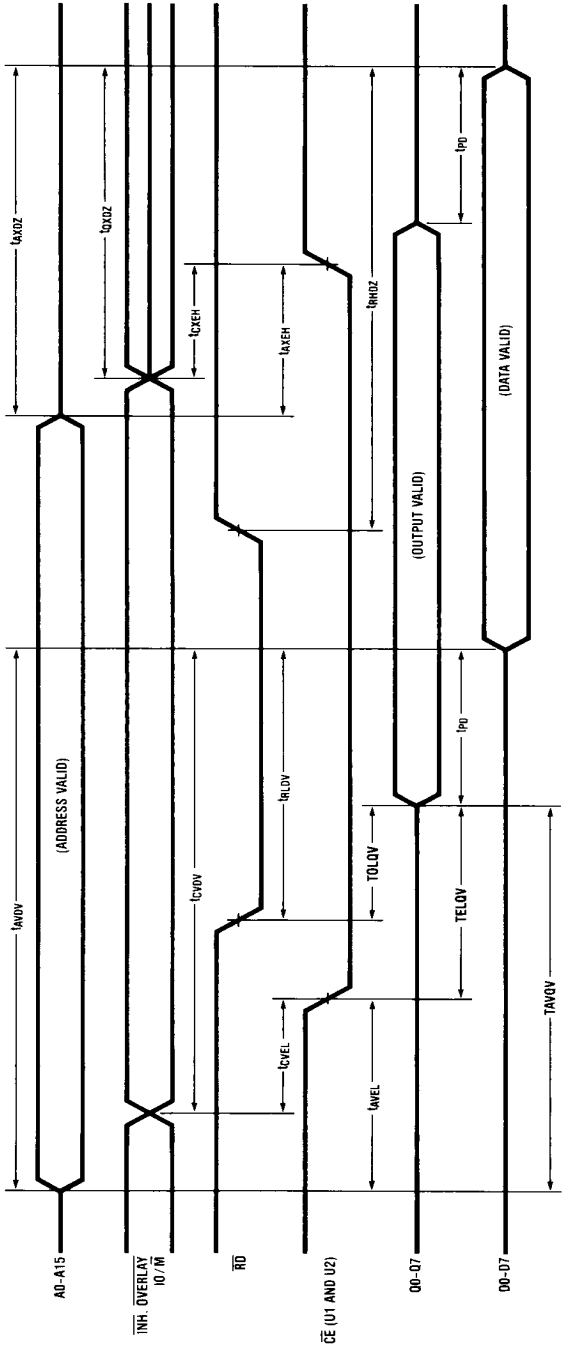
Note 1: I_{IN} on A0-A10 depends on user selected ROM or RAM.

Note 2: This does not include user supplied ROM or RAM.

Note 3: During an opcode fetch these timing values can be increased by 400 ns through jumpering E7.

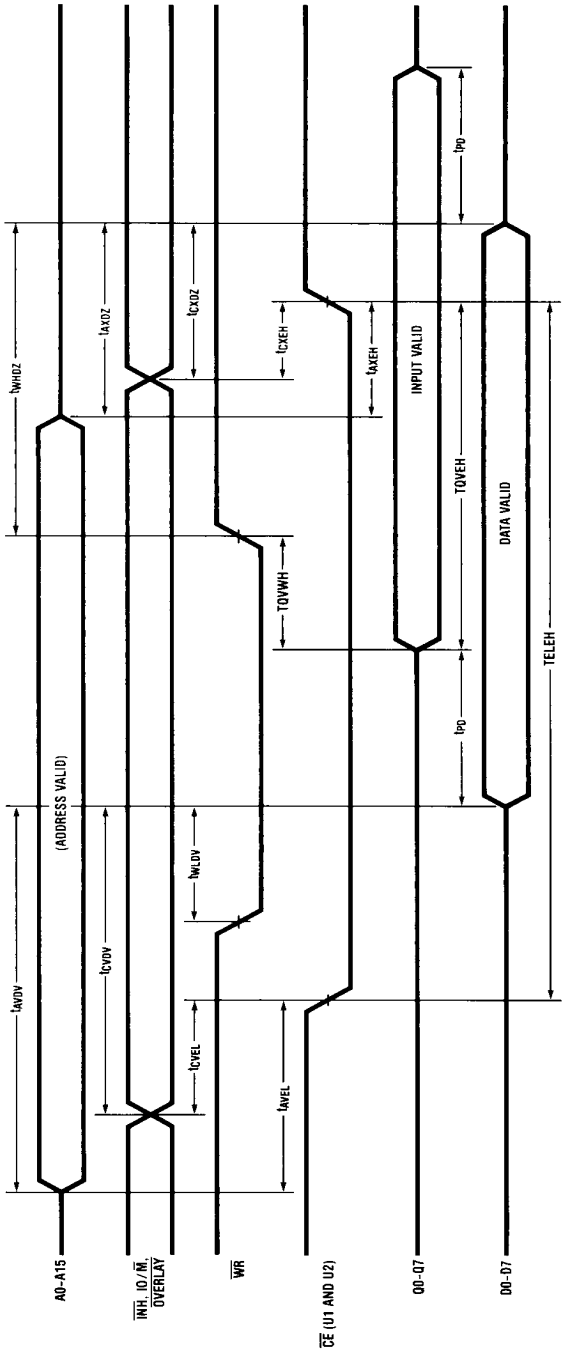
Timing Diagrams

Typical Read Cycle

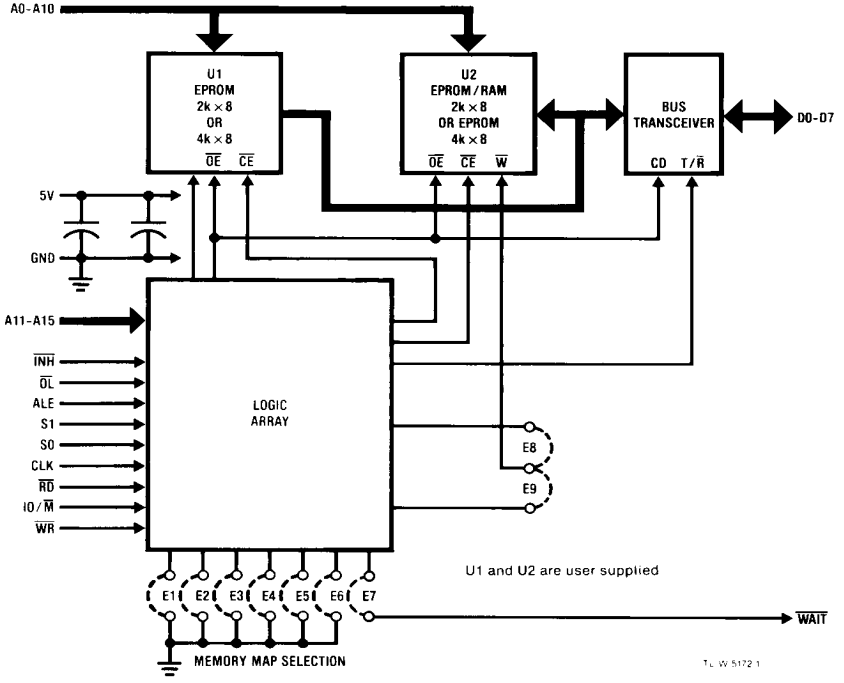


Timing Diagrams (Continued)

Typical Write Cycle



Block Diagram



MEMORY MAPPING

E1	E2	E3	E4	E6	Address	Boundary (HEX)	
•	•	•	•	•	0 0 0 0	F F F	4k Blocks U1 = Lower 2k U2 = Higher 2k
•	•	•		•	1 0 0 0	1 F F F	
•	•		•	•	2 0 0 0	2 F F F	
•	•			•	3 0 0 0	3 F F F	
•		•	•	•	4 0 0 0	4 F F F	
•		•		•	5 0 0 0	5 F F F	
•			•	•	6 0 0 0	6 F F F	
•				•	7 0 0 0	7 F F F	
	•	•	•	•	8 0 0 0	8 F F F	
	•	•		•	9 0 0 0	9 F F F	
	•		•	•	A 0 0 0	A F F F	
	•			•	B 0 0 0	B F F F	
		•	•	•	C 0 0 0	C F F F	
		•		•	D 0 0 0	D F F F	
			•	•	E 0 0 0	E F F F	
				•	F 0 0 0	F F F F	
•	•	•	X		0 0 0 0	1 F F F	8k Blocks U1 = Lower 4k U2 = Higher 4k or 2k RAM
•	•		X		2 0 0 0	3 F F F	
•		•	X		4 0 0 0	5 F F F	
•			X		6 0 0 0	7 F F F	
	•	•	X		8 0 0 0	9 F F F	
	•		X		A 0 0 0	B F F F	
		•	X		C 0 0 0	D F F F	
			X		E 0 0 0	F F F F	

X = don't care

E1 = A15 = logic "0" when jumper is installed (•)

E2 = A14 = logic "0" when jumper is installed (•)

E3 = A13 = logic "0" when jumper is installed (•)

E4 = A12 = logic "0" when jumper is installed (•)

E5 = $\overline{INH}$ = logic "0" when jumper is installed (•)

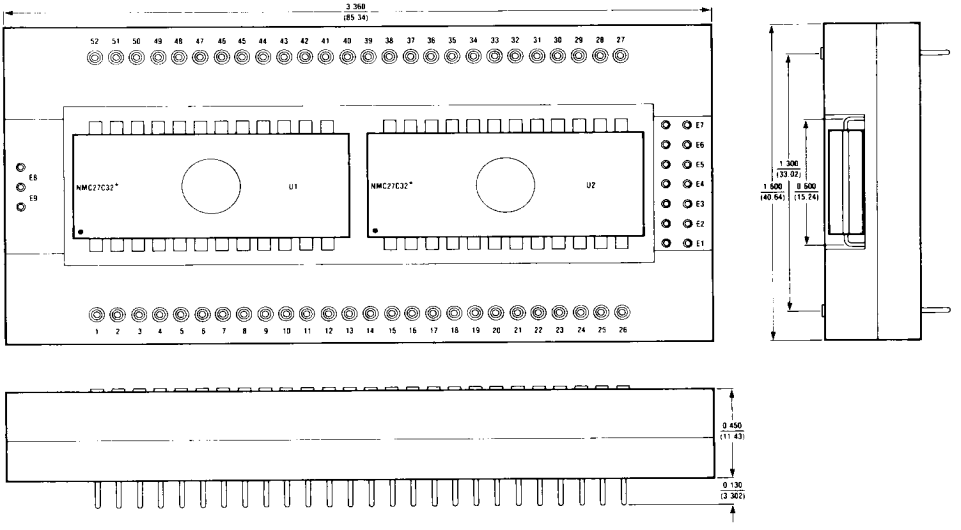
E6 = 4k block select = logic "0" when jumper is installed (•) otherwise 8k block

E7 = $\overline{WAIT}$ when jumper is installed (•) adds one wait state during opcode fetch only.

E8 = U2 is ROM when jumper is installed.

E9 = U2 is RAM when jumper is installed.

Physical Dimensions inches (millimeters)



*Note: U1 and U2 are user-supplied.

Order Number MA2732

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
2900 Semiconductor Drive
Santa Clara, California 95051
Tel: (408) 721-5000
TWX: (910) 339-9240

National Semiconductor GmbH
Furstenriederstrasse Nr 5
D8000 Munchen 21
West Germany
Tel: (089) 5 60 12 0
Telex: 522772

NS Japan K.K.
POB 4152 Shinjuku Center Building
1-25-1 Nishishinjuku, Shinjuku-ku
Tokyo 160, Japan
Tel: (03)349-0811
Telex: 232-2015 NSCJ-J

National Semiconductor (Hong Kong) Ltd.
1st Floor,
Cheung Kong Electronic Bldg
4 Hing Yip Street
Kwun Tong
Kowloon, Hong Kong
Tel: 3-899235
Telex: 43856 NSEHK HX
Cable: NATSEMI HX

National Semiconductores Do Brasil Ltda.
Avda Brigadeiro Faria Lima 830
8 ANDAR
01452 Sao Paulo, Brasil
Tel: 212-1181
Telex: 1131931 NS

NS Electronics Pty. Ltd.
Cnr. Stud Rd. & Mtn. Highway
Bayswater, Victoria 3153
Australia
Tel: 03-729-6333
Telex: 32096