RangeMAX™ LX1688

Multiple Lamp CCFL Controller

PRODUCTION DATA SHEET

DESCRIPTION

The LX1688 is a fixed frequency, dual current/voltage mode, switching regulator that provides the control function for Cold Cathode Fluorescent Lighting (CCFL). This controller can be used to drive a single lamp, but is specifically designed for multiple lamp LCD panels. The IC can be configured as a master or slave and synchronize up to 12 controllers.

The LX1688 includes highly integrated universal 'PWM or DC' dim input that allows either a PWM or DC input to adjust brightness without requiring external conditioning, since a single external capacitor CPWM can be used to integrate a PWM input. Burst mode dimming is possible if the user supplies a low frequency PWM signal on the BRITE input and no CPWM capacitor is used. The controller utilizes Microsemi's patented direct drive fixed frequency topology and patented resonant lamp strike generation technique.

Safety and reliability features include a dual feedback control loop that permits regulation of maximum lamp strike voltage as well as lamp current. Regulating maximum lamp voltage permits the designer to provide for ample worst-case lamp strike voltage while conservatively limiting maximum open circuit voltage. In addition the controller features include auto shutdown for an open or broken lamp, and a lamp fault detection with a status reporting output.

To improve design flexibility the IC includes the ability to select the polarity of both the chip enable and dim (BRITE) inputs. Also included is a switched VDD output of up to 10mA that will allow the user to power other circuitry that can be switched on and off with the inverters enable input. This preserves the micro power sleep mode with no additional components.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: **http://www.microsemi.com**

Protected by U.S. Patents 5,615,093; 5,923,129; 5,930,121; 6,198,234; Patents Pending

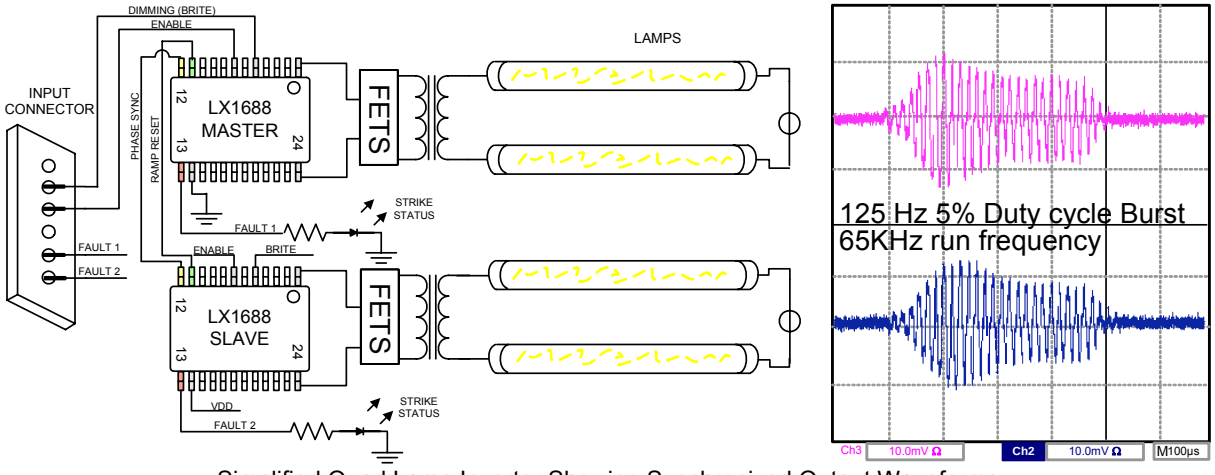
KEY FEATURES

- Provision to Synchronize Lamp Current & Frequency With Other Controllers
- Dimming With Analog or Digital (PWM) Methods (>20:1)
- Programmable Fixed Frequency
- Adjustable Power-up Reset
- ENABLE/BRITE Polarity Selection
- Voltage Limiting on Step-up Transformer Secondary Winding
- Open Lamp Timeout Circuitry
- Switched VDD Output (10mA)
- Micro-Amp Sleep Mode
- Operates With 3.3V to 5V Supply
- 100mA Output Drive Capability

APPLICATIONS / BENEFITS

- Desktop LCD Monitors
- Multiple Lamp Panels
- Low Ambient Light Displays
- High Efficiency
- Lower Cost than Conventional Buck/Royer Inverter Topologies
- Improved Lamp Strike Capability
- Improved Over-Voltage Control

PRODUCT HIGHLIGHT



Simplified Quad Lamp Inverter Showing Synchronized Output Waveforms

PACKAGE ORDER INFO

T_J (°C)	MIN V_{DD}	MAX V_{DD}	PW Plastic TSSOP 24-Pin RoHS compliant / Pb-free Transition DC: 0442
0 to 70	3.0V	5.5V	**LX1688CPW**
-40 to 85	3.0V	5.5V	**LX1688IPW**

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX1688CPW-TR)

Rev. 1.2, 2006-03-09

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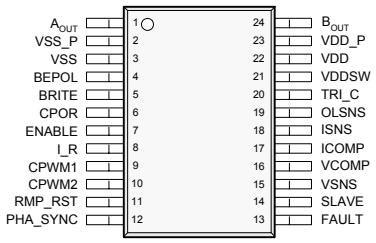
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VDD_P, VDD)..... 6.5V
Digital Inputs ..... -0.3V to VDD +0.5V
Analog Inputs..... –0.1V to VDD +0.5V
Digital Outputs..... -0.3V to VDD +0.5V
Analog Outputs ..... -0.1V to VDD +0.5V
Maximum Operating Junction Temperature ..... 150°C
Storage Temperature..... -65°C to 150°C
Peak Package Solder Reflow Temp. (40 seconds max. exposure) ..... 260°C(+0.-5)

Note 1: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.

PACKAGE PIN OUT



PW PACKAGE
(Top View)

RoHS / Pb-free 100% matte Tin Lead Finish

THERMAL DATA

PW **Plastic TSSOP 24-Pin**

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	100°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

FUNCTIONAL PIN DESCRIPTION

Pin Name	Description	Pin Name	Description
A_{OUT}	Output Driver A	**B_{OUT}**	Output Driver B
VSS_P	Connects to dedicated GND for Aout and Bout Drivers	**VDD_P**	Connects to dedicated VDD for Aout and Bout Drivers
VSS	Connects to analog GND	**VDD**	Connects to analog VDD
BEPOL	Tri-mode input pin to control the polarity of the ENABLE and BRITE signal	**VDDSW**	Switchable VDD output controlled by ENABLE
BRITE	Analog/PWM input for brightness control	**TRI_C**	Connects to external capacitor C_{TRI}
CPOR	Connects an external capacitor C_{POR} to VDD and is used for setting power-up reset pulse width.	**OLSNS**	Analog input to detect open-lamp condition
ENABLE	Used to enable or disable the chip	**ISNS**	Analog input from lamp current, has built-in 300mv offset
I_R	Connects to external resistor R_I; for bias current setting for internal oscillator	**ICOMP**	Current error Amp's output; connects to external capacitor C_{ICOMP}
CPWM1	Connects to external capacitor C_{PWM}, used for integrating an external digital PWM signal for analog dimming	**VCOMP**	Voltage error Amp's output; connects to external capacitor C_{VCOMP}, can be used for soft-start
CPWM2	Connects to external capacitor C_{PWM}, used for integrating an external digital PWM signal for analog dimming.	**VSNS**	Analog input from transformer output voltage
RMP_RST	If SLAVE = "0", RMP_RST is a CMOS output; if SLAVE = "1", it is a CMOS input that locks the ramp oscillation frequency to the master clock	**SLAVE**	Input control pin for setting the IC either in Master or Slave mode; "1" for slave mode and "0" for master mode.
PHA_SYNC	If SLAVE= "0", PHA_SYNC is a CMOS output; if SLAVE = "1", it is a CMOS input that make the A_{OUT}/B_{OUT} phase synchronous with the master	**FAULT**	Digital output to indicate maximum number of lamp striking attempts has occurred without lamp ignition.

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RECOMMENDED OPERATING CONDITIONS

Parameter	LX1688			Units
	Min	Typ	Max	
Supply Voltage (V_{DD} ,V_{DDP})	3		5.5	V
BRITE Linear DC Voltage Range	1		2.5	V
BRITE PWM Logic Signal Voltage Range	0		V_{DD}	V
Digital Inputs (SLAVE, PHA_SYNC, RMP_RST, BEPOL, ENABLE)	0		V_{DD}	V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, specifications apply over the range: T_A=-40 to 85^{O}C, V_{DD} (For LX1688IWP) & T_A= 0 to 70^{O}C, V_{DD} (For LX1688CWP), V_{DD_P} = 3.0 to 5.5V. R_I = 80Kohms, C_{TRI} = 0.083µF

Parameter	Symbol	Test Conditions	LX1688			Units
			Min	Typ.	Max	
DIMMER						
Conventional[1] Dimming BRITE Input Voltage	V_{BRITE_MAX}	V_{BEPOL} = V_{DD}	2.6	2.5		V
	V_{BRITE_MIN}	V_{BEPOL} = V_{DD}	0.4	0.5		
Reverse Dimming BRITE Input Voltage	V_{BRITE_MAX}	V_{BEPOL} = V_{SS} or float	0.4	0.5		V
	V_{BRITE_MIN}	V_{BEPOL} = V_{SS} or float	2.6	2.5		
Max Brightness V_{BRT} Voltage	V_{BRT_FULL}	V_{BEPOL} = V_{SS}, V_{BRITE} = 0.4V	1.90	2.0	2.05	V
Full-darkness V_{BRT} voltage	V_{BRT_DARK}	V_{BEPOL} = V_{SS}, V_{BRITE} = 2.6V		0	0.05	V
ISNS input threshold voltage	V_{TH_IAMP}	T_A= 0 to 70^{O}C	150	300	450	mV
ISNS input threshold voltage	V_{TH_IAMP}	T_A= -40 to 85^{O}C	150	300	550	mV
BRITE-to-ICOMP propagation delay	T_{D_BRITE}			2		µS
STRIKE AND RAMP GENERATOR						
Max. number of strike before fault	N_{FAULT}		63			
Triangular Wave Generator Analog Output Peak Voltage	V_{P_TRI}		2.3	2.5	2.6	V
Triangular Wave Generator Analog Output Valley Voltage	V_{V_TRI}		0.15	0.3	0.40	
Triangular Wave Generator Oscillation Frequency	$F_{\_TRI}$		7	10	13	Hz
Max. Lamp Strike Frequency	F_{MAX_STK}	F_{MAX_STK} = F_{LAMP} X ~2.5	150	195		KHz
Lamp Run Frequency	F_{LAMP}	V_{OLSNS} > 0.65V; VDD=5V T_A= 0 to 70^{O}C	60	65	70	KHz
Lamp Run Frequency	F_{LAMP}	V_{OLSNS} > 0.65V; VDD=5V T_A=-40 to 85^{O}C	57	65	70	KHz
Lamp Run Frequency regulation over V_{DD}	F_{LAMP_REG}	V_{OLSNS} > 0.65V		4	6	% /V
OLSNS threshold voltage	V_{TH_OLSNS}		740	790	840	mV
OLSNS hysteresis	V_{H_OLSNS}		540	590	640	mV
OLSNS-to-ICOMP propagation delay	T_{D_OLSNS}	GBNT [2]			1	us
Fault, PHA_SYNC, RMP_RST, logic high threshold	V_H		V_{DD} – 0.5			V
Fault, PHA_SYNC, RMP_RST, logic low threshold	V_L			0.7	1	V
Minimum Fault-pin output current	I_FAULT		10	15		mA

[1]Conventional polarity means that the lamp brightness increases with increasing voltage on the BRITE pin. Reverse polarity means that brightness decreases with increasing voltage

[2] Guaranteed but not production tested

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Parameter	Symbol	Test Conditions	LX1688 Min	LX1688 Typ.	LX1688 Max	Units
STRIKE AND RAMP GENERATOR (CONTINUED)						
Minimum PHA_SYNC-pin output current	$I_{\_PHA\_SYNC}$	V_{SLAVE} = 0V	10			mA
Minimum RMP_RST-pin output current	$I_{\_RMP\_RST}$	V_{SLAVE} = 0V	10			mA
Minimum A_SYNC output pulse duty-cycle	D_{O_ASYNC}	V_{SLAVE} = 0V	49	50		%
Minimum A_SYNC input pulse duty-cycle	D_{I_ASYNC}	V_{SLAVE} = V_{DD}	48	50		%
Minimum RMP_RST output pulse duty-cycle	D_{O_RST}	V_{SLAVE} = 0V	10	17		%
Minimum RMP_RST input pulse duty-cycle	D_{I_RST}	V_{SLAVE} = V_{DD}	5			%
OUTPUT BUFFER						
Output Sink Current	I_{SK_OUTBUF}	$V_{AOUT, BOUT}$ = 1V V_{DD} = 5.5V		100		mA
Output Source Current	I_{S_OUTBUF}	$V_{AOUT, BOUT}$ = 4.5V V_{DD} = 5.5V		100		mA
Output Sink Current	I_{SK_OUTBUF}	$V_{AOUT, BOUT}$ = 1V, V_{DD} = 3V		50		mA
Output Source Current	I_{S_OUTBUF}	$V_{AOUT, BOUT}$ = 2V, V_{DD} = 3V		50		mA
Output Sink Current	I_{SK_OUTBUF}	$V_{AOUT, BOUT}$ = 1V, V_{DD} = 5.5V		100		mA
PWM						
VSNS threshold voltage	V_{TH_VSNS}		1.2	1.25	1.3	V
VCOMP Discharge Current	I_{D_VCOMP}			4		mA
IAMP transconductance	G_{M_IAMP}	ΔI_{SNS} = 0.2V	100	200	500	µmho
VAMP, IAMP output source current	I_{S_IAMP}	V_{COMP}, I_{COMP} = 0		75		µA
VAMP, IAMP output sink current	I_{SK_IAMP}	V_{COMP}, I_{COMP} =V_{DD}		75		µA
ICOMP discharge current	I_{D_ICOMP}			10		mA
VAMP transconductance	G_{M_ICMP}	ΔV_{SNS} = 0.1V	200	500	800	µmho
ICOMP-to-output propagation delay	T_{D_ICOMP}			1100		nS
BIAS						
Voltage at Pin I_R	$V_{\_IR}$		0.95		1.05	V
Pin I_R max. source current	I_{MAX_IR}			50		µA
Power-on Reset Pulse Width	T_{POR}	C_{POR} =.1uF		31		mS
Minimum V_{DDSW} sourcing Current	I_{MIN_VDDSW}	(V_{DD} – V_{DDSW}) < 0.2V	10	25		mA
V_{DDSW} Off Current	I_{OFF_VDDSW}	V_{ENABLE} = 0.8V, V_{BEPOL} = V_{DD} V_{DDSW} = 0V		1	15	µA
GENERAL						
Operating Current	I_{DD}	V_{DD} = V_{DD_P} = 5V		5.5	8	mA
Output buffer operating current	I_{DD_P}	V_{OLSNS} = V_{DD} = V_{DD_P} = 5V, C_A = C_B = 1000pF		2	4	mA
ENABLE logic threshold	V_{TH_EN}		0.8	1.7	2.4	V
ENABLE threshold hysteresis	V_{TH_EN}			0.2		V
Sleep-mode current (see table-1 for Pin ENABLE polarity)	I_{DD_SLEEP}	V_{ENABLE} = 0.8V (V_{BEPOL} = V_{DD} or float)		20	50	µA
	I_{DD_SLEEP}	V_{ENABLE} = 2.5V (V_{BEPOL} = V_{DD} or float)		20	50	
VDD_P Leakage in Sleep Mode	I_{DD_SLEEP}	V_{ENABLE} = 0.8V (V_{BEPOL} = V_{SS})		20	300	
	I_{DD_SLEEP}	V_{ENABLE} = 2.5V (V_{BEPOL} = V_{SS})		20	300	
UVLO threshold	V_{TH_UVLO}	Rising turn-on threshold	2.6	2.8	2.9	V
UVLO hysteresis	V_{H_UVLO}	Falling turn-off hysteresis		190		mV

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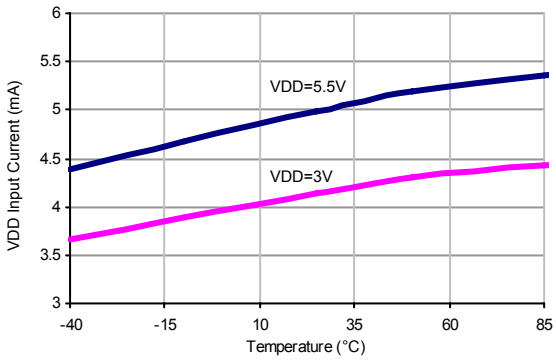
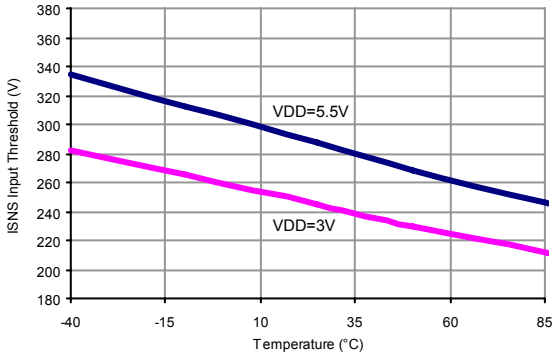
RESPONSE VS WAVELENGTH

Typical Operating Current (VDD)

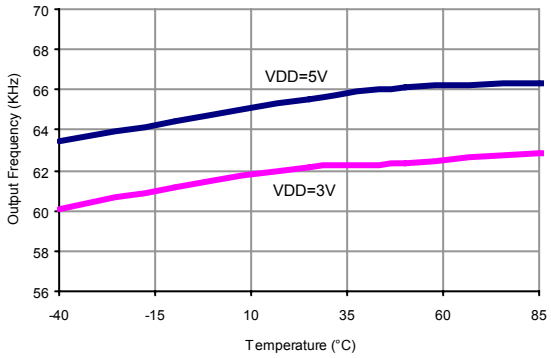


ISNK STEP RESPONSE

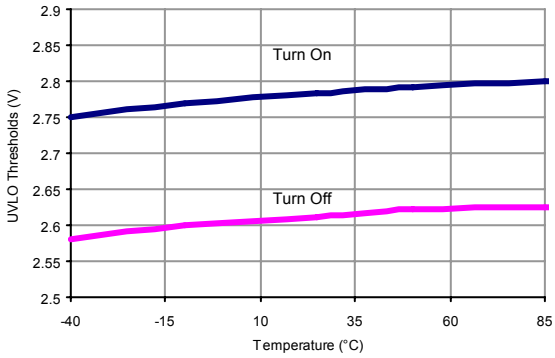
ISNS Input Threshold Voltage Vs Temperature



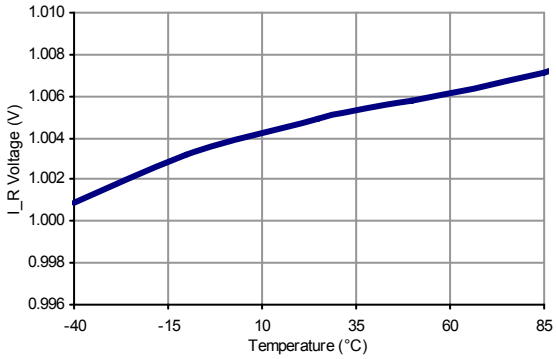
Output Frequency Vs Temperature



Under Voltage Lockout Vs Temperature



I_R Voltage Vs Temperature VDD=V



Power-on-Reset Pulse Width Vs Temperature VDD=5V

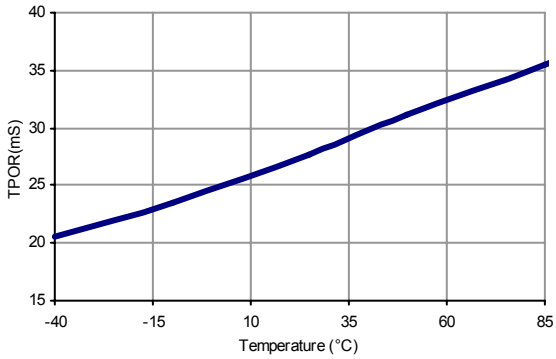


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TABLE 1

Pin BEPOL	ENABLE POLARITY	DIMMING POLARITY*
V_{DD}	+ (HI = CHIP_ON, LOW = CHIP_OFF	CONVENTIONAL
FLOAT	+ (HI = CHIP_ON, LOW = CHIP_OFF)	REVERSE
V_{SS}	- (LOW = CHIP_ON, HI = CHIP_OFF)	REVERSE

* Conventional polarity means that the lamp brightness increases with increasing voltage on the BRITE pin. Reverse polarity means that brightness decreases with increasing voltage

OPERATIONAL MODES

Controller Mode	Controller Operation	Input Pin: OLSNS	Input Pin: SLAVE	Output Pin: FAULT	Pin: RMP_RST	Pin: A_SYNC	Lamp Frequency
Master	Run	> 0.6V	VSS	L	Output: F_{INT}	Output: F_{INT} / 2	F_{INT} / 2
	Striking	< 0.2V	VSS	L	Output: F_{INT}	Output: F_{INT} / 2	Ramping up / down
	Fault	X	VSS	H	Output: F_{INT}	Output: F_{INT} / 2	Off
Slave	Run	> 0.6V	VDD	L	Input: F_{EXT}	Input: F_{EXT} / 2	F_{EXT} / 2
	Striking	< 0.2V	VDD	L	Input: F_{EXT}	Input: F_{EXT} / 2	Ramping up / down
	Fault	X	VDD	H	Input: F_{EXT}	Input: F_{EXT} / 2	Off

SIMPLIFIED BLOCK DIAGRAM

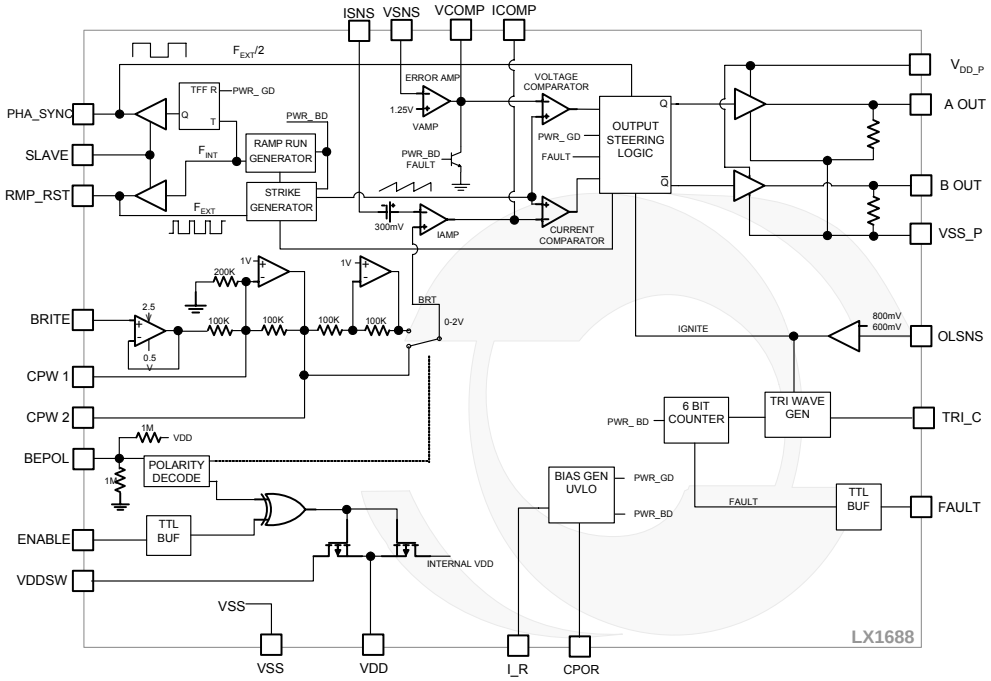

Figure – Simplified Block Diagram

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DETAILED DESCRIPTION

The LX1688 is a backlight controller specifically designed with a special feature set needed in multiple lamp desktop monitors, and other multiple lamp displays. While utilizing the same architecture as Microsemi's LX1686 controller it eliminates the synchronized digital dimming and adds, lamp 'strike' count out timer, lamp fault status output, and external clock input/output that permits multiple controllers to synchronize their output current both in frequency and phase.

OPERATION FROM 3.3V AND/OR 5.0V INPUT SUPPLY

The LX1688 is designed to operate and meet all specifications at 3.3V ±10% to 5.0V ±10%. The under voltage lockout is set at nominally 2.8V with a 190mV hysteresis.

MASTER/SLAVE CLOCK SYNCHRONIZATION

One or more controllers (up to 11) may be designated as slave controllers and receive ramp reset and phase synchronization from the designated master controller. This will allow up to 12 lamps (24 with two lamps in series/controller design) to all operate in phase and frequency synchronization. This is important to prevent random interference between lamps through unpredictably changing electric and magnetic fields that will inevitably link them.

The LX1688 has two independent oscillators, one for lamp strike and one for the lamp run frequency. The strike oscillator ramps the operating frequency slowly up and down when the open lamp sense input (OLSNS) indicates the lamp is not ignited. During this lamp strike condition the operating frequency of each IC will vary up and down as needed to strike its lamp. The controller is so designed that the master controller clock remains at the pre-selected frequency for fully ignited lamps even while striking. Likewise the designated slave controller will not alter the frequency or phase of the master clock during its strike phase. Thus each controller will vary its frequency as needed to strike its lamp then it will synchronize to the master clock frequency and phase.

The TRI_C wave generator (see Block Diagram) sets the rate of operating frequency variation during lamp strike. The TRI_C generator is connected to a 6-bit counter that times out after 63 cycles and then latches the FAULT output high if the OLSNS input indicates no lamp current is flowing. Even in the case of timeout fault the master controller clock will continue to provide synchronization to the slave controllers.

When synchronizing more than one controller the Ramp Reset (RMP_RST), Phase Sync (PHA_SYNC), and Slave Input/Output are used. RMP_RST and PHA_SYNC should be connected between all the controllers. The master controller should have its SLAVE pin connected to VSS (GND) and the slave controllers SLAVE input to VDD (High).

BEPOL INPUT

The BEPOL pin is a tri-mode input that controls the polarity of the ENABLE and BRITE input signals. Depending on the state of this pin (VDD, floating, or VSS) the controller can be set to allow active high enable with active high full brightness or active high or low enable with active low full brightness (see Table 1).

BRITE INPUT (DIMMING INPUT)

The BRITE input is capable of accepting either a DC voltage ($\geq$ .5V to $\leq$ 2.5V) or a PWM digital signal that is clamped on chip ($\leq$ .5V or $\geq$ 2.5V). A digital signal can either be passed unfiltered to effect pulse 'digital' dimming or filtered with a capacitor to effect analog dimming with a digital PWM signal.

Analog Dimming Methods:

- Mechanical or digital potentiometer set to provide 1V to 2.5V on the wiper output. A filter cap from BRITE to signal ground is recommended.
- D/A converter output directly connected to BRITE input. A R/C filter using a capacitor from the CPW1 input to ground for applications where the ADC output may contain noise sufficient to modulate the BRITE input.
- A high frequency PWM digital logic pulse connected directly to the BRITE input. The Brightness (BRT, internal node) output will be sensitive only to the PWM duty cycle, and not to the PWM signal amplitude, so long as the amplitude exceeds 2.6V for a logic high (1) and is less than .4V for a logic (0). This pulse frequency will typically be between 1KHz and 100KHz and will not be synchronized with the LCD video frame rate. A capacitor (CPWM) between CPW1 and CPW2 will integrate the PWM signal for use by the controller.

Digital Dimming Methods:

- Low frequency PWM digital logic pulses connected directly to the BRITE input. As above the Brightness (BRT internal) will be sensitive only to the PWM duty cycle, and not to the PWM signal amplitude, so long as the amplitude exceeds 2.6V for a logic high (1) and is less than .4V for a logic (0). This pulse frequency will typically be in the range of 90-320Hz.

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DETAILED DESCRIPTION

and may or may not be externally synchronized to the LCD video frame rate. It will directly gate the signal BRT. CPWM should not be used in this case.

FAULT PIN

The fault pin is a digital output that indicates that the maximum numbers of strike attempts has occurred without lamp ignition. In this condition the FAULT pin will go active high with typically 20mA drive capability. Holding the OLSNS pin low (<200mV) will also force timeout and activate the FAULT pin. When used as a master, fault condition true does not inhibit master clock outputs PHA_SYNC and RMP_RST.

I_R PIN

The run mode frequency of the output is one half the internal ramp frequency, which is proportional to a bias current set by resistor RI of 80.6K. The output frequency can thus be adjusted by varying the value of RI-R, the typical range from about 50K to 100K. Since there is some variation in the frequency due to change in the input supply (VDD) it is recommended that the value of RI-R be selected at the nominal input voltage.

SLEEP MODE (ENABLE SIGNAL) AND SWITCHED VDD (VDDSW)

Since the LX1688 can be used in portable battery operated systems, a very low power sleep mode is included. The IC will consume less than 10µA quiescent current from both the VDD and VDD_P pins combined, when the ENABLE pin is deactivated. The polarity of the ENABLE pin is programmable by the BEPOL input (see table 1). In addition the controller provides a switched supply pin VDDSW this output supplies at least 10mA at VDD – .2V for external circuitry. This output can be used to power additional circuitry that can be enabled with the controller.

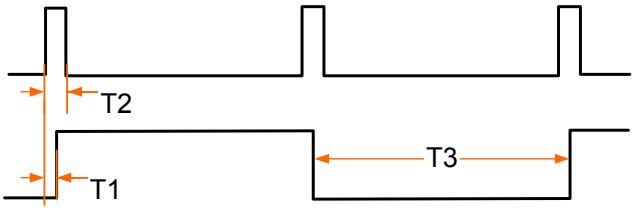
RMP_RST AND PHA_SYNC PIN TIMING REQUIREMENT WITH SLAVE MODE OPERATION

When the LX1688 is configured for slave mode operation, and RMP_RST and PHA_SYNC is supplied from an external source, the signal timing should be met as outlined below.

RMP_RST should be 2 times frequency of lamp frequency and duty should be 10 to 13%, and PHA_SYNC should be generated by divide by 2 of RMP_RST signal. Phase of these signals should be met the as shown, note the delay between the RMP_RST and PHA_SYNC signals:

	Min	Typ	Max	Unit
T1	150	250		nsec
T2	10		13	%
T3	49	50	51	%
Tr, Tf			100	nsec

T3 duty is 50% of operating frequency.



BIAS & TIMING EQUATIONS

Formula 1:
Triangular Wave Generator Frequency, F_{TRI}

$$F_{TRI} = \frac{1}{(25 \times R_I \times C_{TRI})} \text{ [Hz]}$$

Formula 2:
Lamp Frequency (A_{OUT}'s switching frequency), F_{LAMP}

$$F_{LAMP} = \frac{1}{200e\text{-}12 \times R_I} \text{ [Hz]}$$

Formula 3:
Minimum Current Error Amp Bandwidth, BW_{IEA_MIN}

$$B_{WIEA\_MIN} = \frac{0.000048}{C_{ICOMP}} \text{ [Hz]}$$

Formula 4:
Minimum Voltage Error Amp Bandwidth, B_{WVEA_MIN}

$$B_{WVEA\_MIN} = \frac{0.000048}{C_{VCOMP}} \text{ [Hz]}$$

Formula 5:
Softstart time, T_{SS}

$$T_{SS} = 4{,}500{,}000 \times C_{VCOMP} \text{ [sec]}$$

Formula 6:
Minimum Power-on Reset Pulse Width, T_{MIN_POR}

$$T_{MIN\_POR} = 2.3e6 \times C_{POR} \text{ [sec]}$$

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APPLICATION CIRCUITS

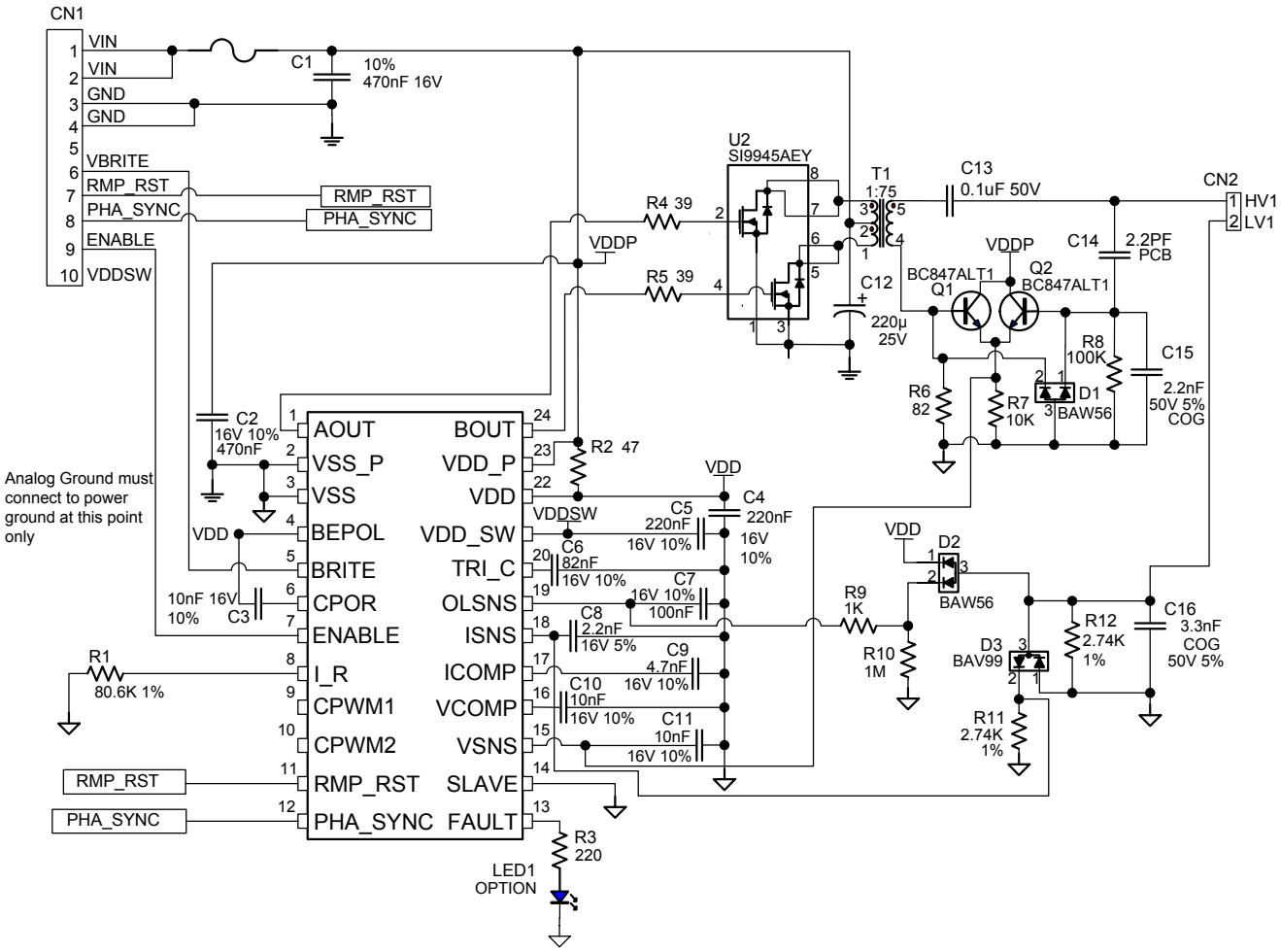

Figure 1 – Schematic for LX1688 Inverter Module Configured as Master

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APPLICATION INFORMATION

APPLICATION EXAMPLE WITH LX1688

This section will highlight the features of LX1688 controller by showing a practical example. Three identical inverter modules are connected to each other and each module drives a single lamp. One module configured as a master and two others configured as slaves.

A complete schematic hooked up a a master is given in Figure 1, the schematic provides all necessary functions such as high voltage feedback for regulation the peak lamp voltage, short-circuit protection, open lamp sensing and lamp current regulation needed for a typical application. The section follows with measurement waveforms and list of material of the actual modules. For more detail design procedure and circuit description please refer to application note (AN-13), which is available in Microsemi's web site.

INPUT VOLTAGE

The LX1688 controller can operate at 3.3 to 5.0V ±10%, in this application all modules were driven by the same power voltage (a constant 5.0V), which provides VDD for controllers, and input voltage for the power section. Notice that VDD feeds all analog signals and VDD_P feeds only the output driver stage, these two signals should be filtered separately (Figure 1).

SETTING LAMP FREQUENCY

The value of R1 determines magnitude of internal current sources that set timing parameters. Equation (2) gives the relationship between Lamp frequency (FLAMP) and (RI_R), R1 in schematic. For this application we choose R6=80.6 KΩ, which results to a lamp frequency at 62.0 KHz.

DIMMING

The LX1688 includes highly integrated universal 'PWM or DC' dim input that allows either a PWM or DC input without requiring external conditioning.

In this application we choose Digital Dimming by applying a PWM signal to BRITE pin.

All modules were driven by the same PWM signals, but notice that it is possible to dim each module quite separately.

BEPOL pin has three different modes (see table 1), in this application it is connected to VDD which means active high enable with active high full brightness.

The PWM signal can be varied in frequency between 48-320 HZ. No capacitor between CPWM1 and CPWM2 is necessary.

SETTING MASTER/SLAVE CONFIGURATION

Simply connecting pin 14 to the ground for a master and to the VDD for a slave will do master and slave configuration. As shown in figure 2, module (A) configured as master and modules (B) and (C) configured as slaves.

SYNCHRONIZATION OF FREQUENCY AND PHASE

To synchronize the Lamp frequency and phase of all modules, it is required to connect the RMP_RST pin of all the modules together and connect PHA_SYNC pin of all the modules together.

LAYOUT CONSIDERATION

By designing the layout in a proper way we can reduce the overall noise and EMI for the module.

The gate drivers for MOSFETs should have an independent loop that doesn't interface with the more sensitive analog control function, therefore LX1688 provides two power inputs with separate ground pins (analog/signal), VDD feeds all analog signals and VDD_P feeds only the output drivers, as shown in figure1 these two pins (pin 23, 24) are separated and filtered by R14, C2 and C7. The connection of two ground pins should be at only one point as shown in figure1.

The power traces should be short and wide as possible and all periphery components such capacitors should be located as closed as possible to the controller.

OSCILLOSCOPE WAVEFORMS PICTURES

The following oscilloscope waveform pictures are taken from the actual circuits and will show the operation of the modules in different modes when three identical modules are synchronized, one as a master, and two others as slaves.

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TYPICAL SLAVE APPLICATIONS

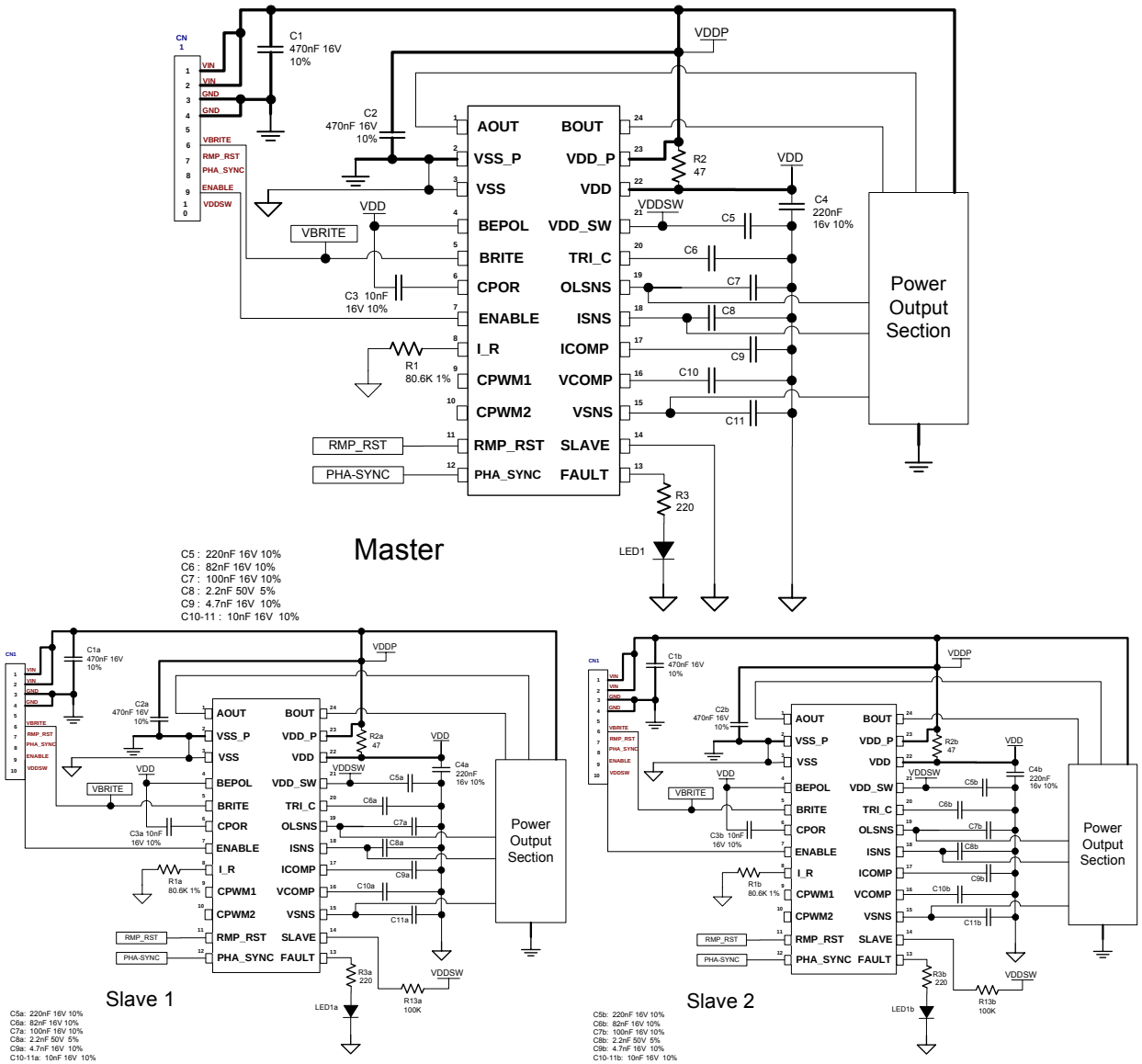

Figure 2 – Schematic Modules Connected as a Master and Slave

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THEORY OF OPERATION

Multiple Lamp Sync

The figure 3 shows the sync signals (PHA_SYNC and RMP_RST) timing relationship to Gate signal AOUT, for the master module. AOUT and PHA_SYNC running at the same frequency and RMP_RST signal has the twice frequency.

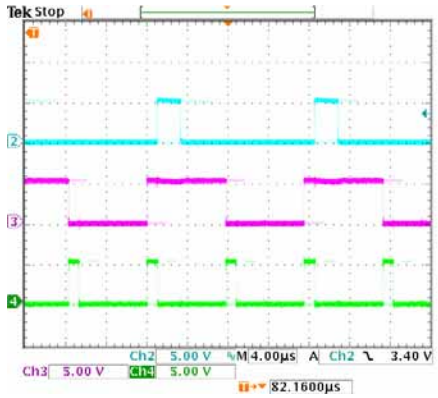

Figure 3- Sync signals-Timing relationship to A_{OUT} CH2= A_{OUT}(Master), CH3=PHA_SYNC, CH4=RMP_RST

Strike Mode

Every IC includes a separate strike controller that operates from the primary oscillator; therefore the strike controller is independent of the sync signals. The following oscilloscope waveform picture is taken when the master module is on striking mode and the salves are on running mode.

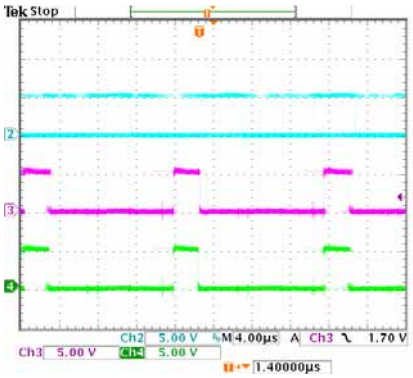

Figure 5- Master is in striking mode while slaves are in running mode CH2= A_{OUT}(Master), CH3=A_{OUT}(Slave1), CH4=A_{OUT}(Slave2)

Output Drivers

The figure 4 shows the gate signals of the modules, which are operating, in running mode during digital dimming with 95% duty cycle. As shown all signals are synchronized. The difference between each signal's duty cycles is because each lamp has an independent control loop.

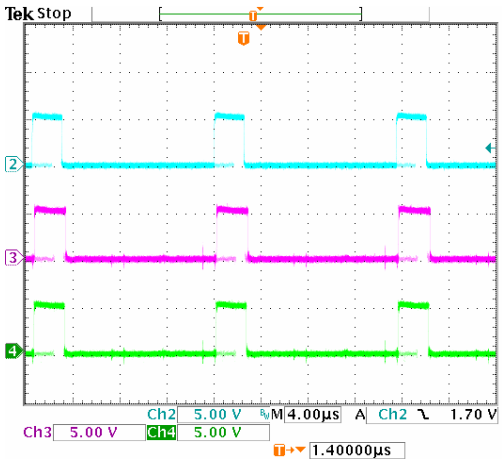

Figure 4- Output drivers of both Master and Slaves.
CH2=A_{OUT}(Master),
CH3=A_{OUT}(Slave1),
CH4=A_{OUT}(Slave2)

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THEORY OF OPERATION

Digital Dimming

The following oscilloscope waveforms are showing gate signals of Master and slaves during digital dimming at 50% and 5% duty cycle.

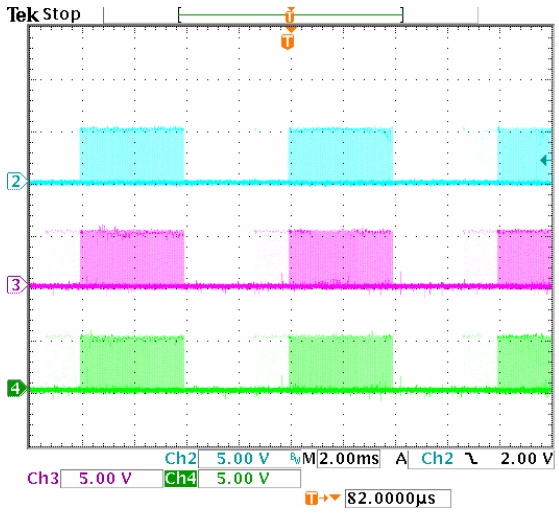

Figure 6- Gate signals during digital dimming with 50% duty cycle CH2= A_{OUT}(Master), CH3=A_{OUT}(Slave1), CH4=A_{OUT}(Slave2)

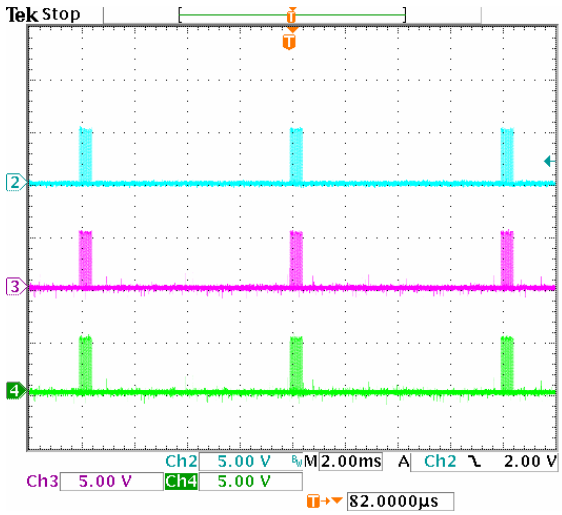

Figure 7- Gate signals during digital dimming with 5% duty cycle CH2= A_{OUT}(Master), CH3=A_{OUT}(Slave1), CH4=A_{OUT}(Slave2)

Output currents

Figure 8 shows the output current of master and slaves during digital dimming with 5% duty cycle. The lamp currents are operating in phase and frequency synchronization. This prevents random interface between controllers and reduces EMI.

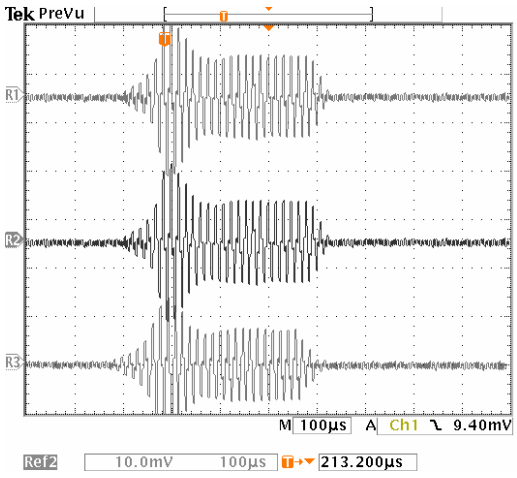

Figure 8- Output current during digital dimming with 5% duty cycle R1= out(Master)
R2=Iout(Slave1)
R3=Iout(Slave2)
Lamp Current at 10mA/Div

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LX1688 MODULE BOARD LIST OF MATERIAL

Reference Designator	Part Description	Manufacture	Part Number
U1	Backlight Controller	**Microsemi**	LX1688
U2	Dual N-Channel MOSFET	**Siliconix**	Si9945AEY
Q1, Q2	NPN Transistor	**Motorola**	BC847ALT1
D1, D2	Dual Diode	**Motorola**	BAW56
D3	Dual Diode	**Philips**	BAV99
LED1	LED		
R1	80.6K 1% 1/16 W		
R2	47 ohm 5% 1/8 W		
R3	220 ohm 5% 1/8 W		
R4, R5	39 ohm 5% 1/16 W		
R6	82 ohm 5% 1/16 W		
R7	10K 5% 1/16 W		
R8	100K 5% 1/16 W		
R9	1K 5% 1/16 W		
R10	1 M 5% 1/16 W		
R11, R12	2.74K 1% 1/16 W		
C1, C2	470nF 16V 10% X7R 1206		
C3	10nF 16V 10% 0805	**NOVACAP**	
C4	220nF 16V 10% X7R 1206		
C5	220nF 16V 20% 0805	**AVX**	0805YC224MAT2A
C6	82nF 16V 10% X7R 0603	**AVX**	0603YC823KAT2A
C7	100nF 16V 20% X7R	**AVX**	0603YC104MAT2A
C8	2.2nF 50V 10%	**NOVACAP**	0603B22K500NT
C9	4.7nF 16V 10% X7R	**AVX**	0603YC472KAT2A
C10, C11	10nF 16V 10% X7R	**AVX**	0603YC103KAT2A
C12	220µF Tantalum 7343	**AVX**	
C13	220pF 2KV 5% COG	**NOVACAP**	1206N221J202NT
C14	2.2pF PCB		
C15	2.2nF 50V 5% COG	**AVX**	08055A222JAT2A
C16	3.3nF 50V 5% COG	**NOVACAP**	0805N332J500NT
T1	Low profile, High voltage xfmr, turns ratio 1:75	**Microsemi**	SGE2645-1
CN1	Connector, 10 pin	**Molex**	53261-1090
CN2	Connector, 2 pin	**Molex**	

Table 2- List of material for LX1688 inverter module

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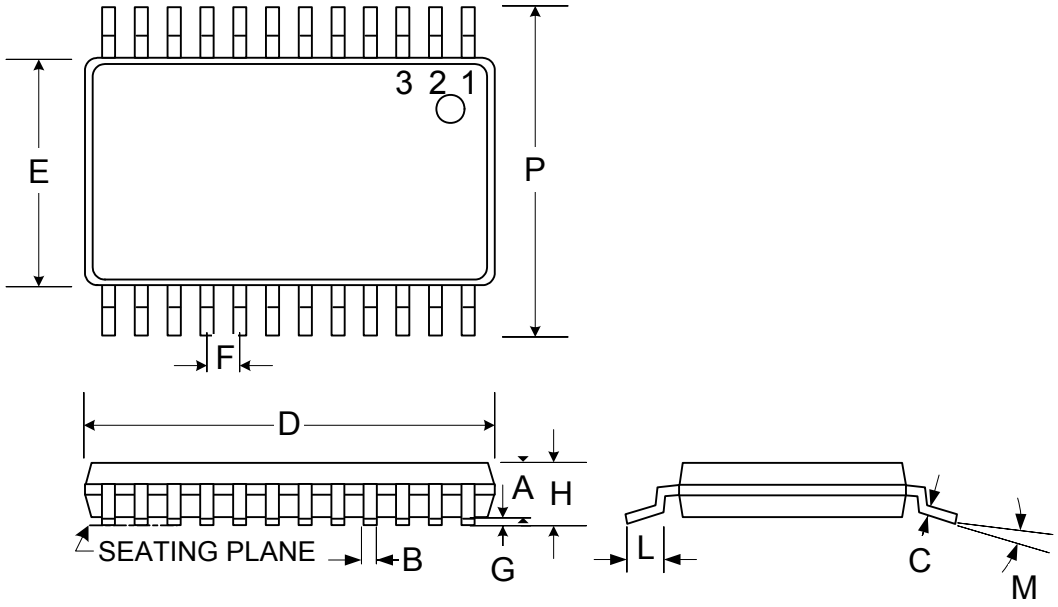
PACKAGE DIMENSIONS

PW 24-Pin Thin Small Shrink Outline (TSSOP) Package



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.85	0.95	0.033	0.037
B	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	7.70	7.90	0.303	0.311
E	4.30	4.50	0.169	0.177
F	0.65 BSC		0.025 BSC	
G	0.05	0.15	0.002	0.005
H	–	1.10	–	.0433
L	0.50	0.75	0.020	0.030
M	0°	8°	0°	8°
P	6.25	6.55	0.246	0.258
*LC	–	0.10	–	0.004

* Lead Coplanarity

Note: Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.

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NOTES