

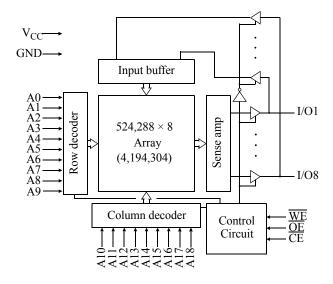
5V/3.3V 512K × 8 CMOS SRAM

Features

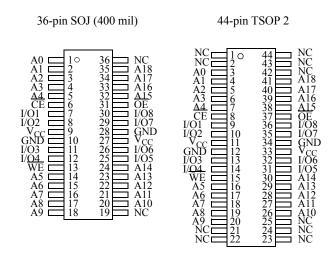
- AS7C4096 (5V version)
- AS7C34096 (3.3V version)
- Industrial and commercial temperature
- Organization: 524,288 words × 8 bits
- Center power and ground pins
- High speed
 - 10/12/15/20 ns address access time
- 5/6/7/8 ns output enable access time
- Low power consumption: ACTIVE
 - 1375 mW (AS7C4096) / max @ 12 ns
 - 576 mW (AS7C34096) / max @ 10 ns

- Low power consumption: STANDBY
- 110 mW (AS7C4096) / max CMOS
- 72 mW (AS7C34096) / max CMOS
- Equal access and cycle times
- Easy memory expansion with \overline{CE} , \overline{OE} inputs
- TTL-compatible, three-state I/O
- JEDEC standard packages
 - 400 mil 36-pin SOJ
 - 44-pin TSOP 2
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 100 mA

Logic block diagram



Pin arrangements



Selection guide

		-10	-12	-15	-20	Unit
Maximum address access time		10	12	15	20	ns
Maximum outputenable access time	5	6	7	8	ns	
Mariana anantina amant	AS7C4096	_	250	220	180	mA
Maximum operating current	AS7C34096	160	130	110	100	mA
Marianum CMOS atondhy aumant	AS7C4096	_	20	20	20	mA
Maximum CMOS standby current	AS7C34096	20	20	20	20	mA



Functional description

The AS7C4096 and AS7C34096 are high-performance CMOS 4,194,304-bit Static Random Access Memory (SRAM) devices organized as 524,288 words × 8 bits. They are designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 10/12/15/20 ns with output enable access times (t_{OE}) of 5/6/7/8 ns are ideal for high-performance applications. The chip enable input \overline{CE} permits easy memory expansion with multiple-bank memory systems.

When $\overline{\text{CE}}$ is high the device enters standby mode. The AS7C4096/AS7C34096 is guaranteed not to exceed 110/72 mW power consumption in CMOS standby mode.

A write cycle is accomplished by asserting write enable ($\overline{\text{WE}}$) and chip enable ($\overline{\text{CE}}$). Data on the input pins I/O1–I/O8 is written on the rising edge of $\overline{\text{WE}}$ (write cycle 1) or $\overline{\text{CE}}$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{\text{OE}}$) or write enable ($\overline{\text{WE}}$).

A read cycle is accomplished by asserting output enable (\overline{OE}) and chip enable (\overline{CE}) , with write enable (\overline{WE}) high. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible, and operation is from either a single 5V(AS7C4096) or 3.3V(AS7C34096) supply. Both devices are available in the JEDEC standard 400-mil 36-pin SOJ and 44-pin TSOP 2 packages.

Absolute maximum ratings

Parameter	Device	Symbol	Min	Max	Unit
Voltage on V _{CC} relative to GND	AS7C4096	V _{t1}	-1	+7.0	V
voltage on vec relative to GND	AS7C34096	V _{t1}	-0.5	+5.0	V
Voltage on any pin relative to GND		V_{t2}	-0.5	V _{CC} +0.5	V
Power dissipation		P_{D}	_	1.0	W
Storage temperature		T_{stg}	-65	+150	°C
Temperature with V _{CC} applied		T _{bias}	-55	+125	°C
DC current unto output (low)		I_{OUT}	_	20	mA

NOTE: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

CE	WE	OE	Data	Mode
Н	X	X	High Z	Standby (I _{SB} , I _{SB1})
L	Н	Н	High Z	Output disable (I _{CC})
L	Н	L	D_{OUT}	Read (I _{CC})
L	L	X	$\mathrm{D_{IN}}$	Write (I _{CC})

Key: X = Don't care, L = Low, H = High



Recommended operating condition

Parame	eter	Device	Symbol	Min	Nominal	Max	Unit
			V _{CC} (12/15/20)	4.5	5.0	5.5	V
Supply voltage		AS7C34096	V _{CC} (10)	3.15	3.30	3.6	V
		AS7C34096	V _{CC} (12/15/20)	3.0	3.3	3.6	V
		AS7C4096	V_{IH}	2.2	_	$V_{CC} + 0.5$	V
Input voltage		AS7C34096	V_{IH}	2.0	_	$V_{CC} + 0.5$	V
			V _{IL} ¹	-0.5	_	0.8	V
Ambient operating	commercial		$T_{\mathbf{A}}$	0	_	70	°C
temperature	industrial		$T_{\mathbf{A}}$	-40	_	85	°C

¹ V_{IL} min = -1.0V for pulse width less than 5ns.

DC operating characteristics (over the operating range) 1

				-1	10	-12		-15		-20		
Parameter	Symbol	Test conditions	Device	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Input leakage current	$ I_{LI} $	$V_{CC} = Max$, $V_{IN} = GND$ to V_{CC}	AS7C4096/ AS7C34096	ı	1	ı	1	ı	1	ı	1	μΑ
Output leakage current	$ I_{LO} $	$V_{CC} = Max, \overline{CE} = V_{IH}$ $V_{OUT} = GND \text{ to } V_{CC}$	AS7C4096/ AS7C34096	ı	1	-	1	1	1	_	1	μΑ
Operating power supply current	I _{CC}	$V_{CC} = Max, \overline{CE} < V_{IL}$ $f = f_{Max}, I_{OUT} = 0mA$	AS7C4096 AS7C34096	-	160	-	250 130	1	220 110	<u> </u>	180	mA
Standby	I_{SB}	$V_{CC} = Max, \overline{CE} = V_{IH}$ $f = f_{Max}, I_{OUT} = 0mA$	AS7C4096 AS7C34096	_ _	- 60	_ _	60 60		60	_ _	60	mA
power supply	_	$V_{CC} = Max,$	AS7C4096	_	_	-	20	-	20	-	20	
current	I_{SB1}	$\overline{CE} \ge V_{CC} - 0.2V, V_{IN} \le 0.2V \text{ or } V_{IN}$ $\ge V_{CC} - 0.2V, f = 0$	AS7C34096	ı	20	l	20	I	20	I	20	mA
Output	V_{OL}	$I_{OL} = 8 \text{ mA}, V_{CC} = \text{Min}$	AS7C4096/	_	0.4	-	0.4	_	0.4		0.4	V
voltage	V_{OH}	$I_{OH} = -4 \text{ mA}, V_{CC} = \text{Min}$	AS7C34096	2.4	_	2.4	_	2.4	_	2.4	_	V

Capacitance (f = 1MHz, T_A = 25° C, V_{CC} = NOMINAL)²

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, CE, WE, OE	$V_{IN} = 0V$	5	pF
I/O capacitance	C _{I/O}	I/O	$V_{IN} = V_{OUT} = 0V$	7	pF



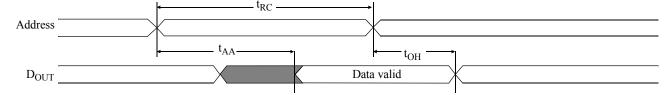
Read cycle (over the operating range)^{3,9}

	Symbo	-1	-10		12	-15		-2	20		
Parameter	1	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Read cycle time	t _{RC}	10	_	12	_	15	_	20	_	ns	
Address access time	t _{AA}	_	10	_	12	_	15	_	20	ns	3
Chip enable (\overline{CE}) access time	t _{ACE}	_	10	_	12	_	15	_	20	ns	3
Output enable (OE) access time	t _{OE}	_	5	_	6	_	7	_	8	ns	
Output hold from address change	t _{OH}	3	_	3	_	3	_	3	_	ns	5
CE Low to output in low Z	t_{CLZ}	3	_	3	_	0	_	0	_	ns	4, 5
CE High to output in high Z	t _{CHZ}	_	5	_	6	_	7	_	9	ns	4, 5
OE Low to output in low Z	t _{OLZ}	0	_	0	_	0	_	0	_	ns	4, 5
OE High to output in high Z	t _{OHZ}	_	5	_	6	_	7	_	9	ns	4, 5
Power up time	t_{PU}	0	_	0	_	0	_	0	_	ns	4, 5
Power down time	t _{PD}	1	10	_	12	_	15	_	20	ns	4, 5

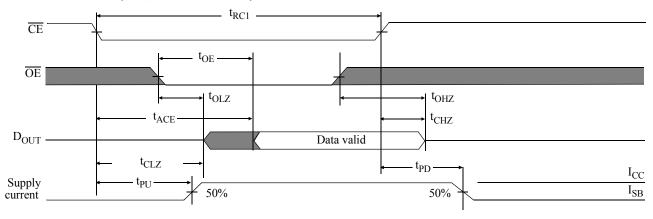
Key to switching waveforms

Rising input Falling input Undefined/don't care

Read waveform 1 (address controlled)^{3,6,7,9}



Read waveform 2 (CE, OE controlled)^{3,6,8,9}



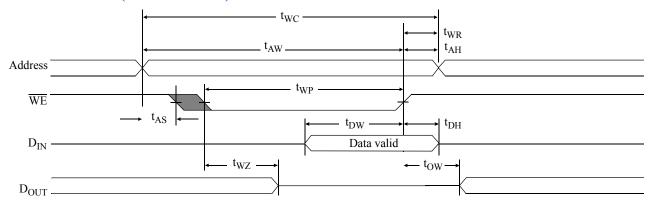
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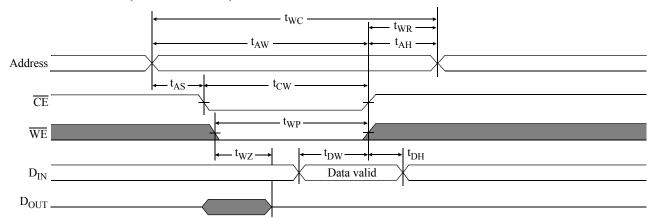
Write cycle (over the operating range) II

		-	-10		12		15	-2	20		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Write cycle time	t_{WC}	10	_	12	_	15	_	20	_	ns	
Chip enable (CE) to write end	t_{CW}	7	_	8	_	10	_	12	_	ns	
Address setup to write end	t _{AW}	7	_	8	_	10	_	12	_	ns	
Address setup time	t_{AS}	0	_	0	_	0	_	0	_	ns	
Write pulse width $(\overline{OE} = high)$	t_{WP1}	7	_	8	_	10	_	12	_	ns	
Write pulse width $(\overline{OE} = low)$	t _{WP2}	10	_	12	_	15	_	20	_	ns	
Address hold from end of write	t_{AH}	0	_	0	_	0	_	0	_	ns	
Write recovery time	t_{WR}	0	_	0	_	0	_	0	_	ns	
Data valid to write end	t_{DW}	5	_	6	_	7	_	9	_	ns	
Data hold time	t_{DH}	0	_	0	_	0	_	0	_	ns	4, 5
Write enable to output in high Z	t_{WZ}	0	5	0	6	0	7	0	9	ns	4, 5
Output active from write end	t_{OW}	3	-	3	-	3	-	3	-	ns	4, 5

Write waveform 1 (WE controlled)^{10,11}



Write waveform 2 (CE controlled)^{10,11}





AC test conditions

- Output load: see Figure B or Figure C.

- Input pulse level: GND to 3.0V. See Figures A, B, and C.

- Input rise and fall times: 2 ns. See Figure A.

- Input and output timing reference levels: 1.5V.

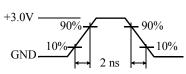


Figure A: Input pulse

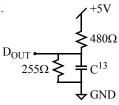


Figure B: 5V Output load

Thevenin equivalent:

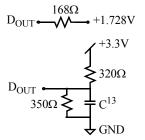


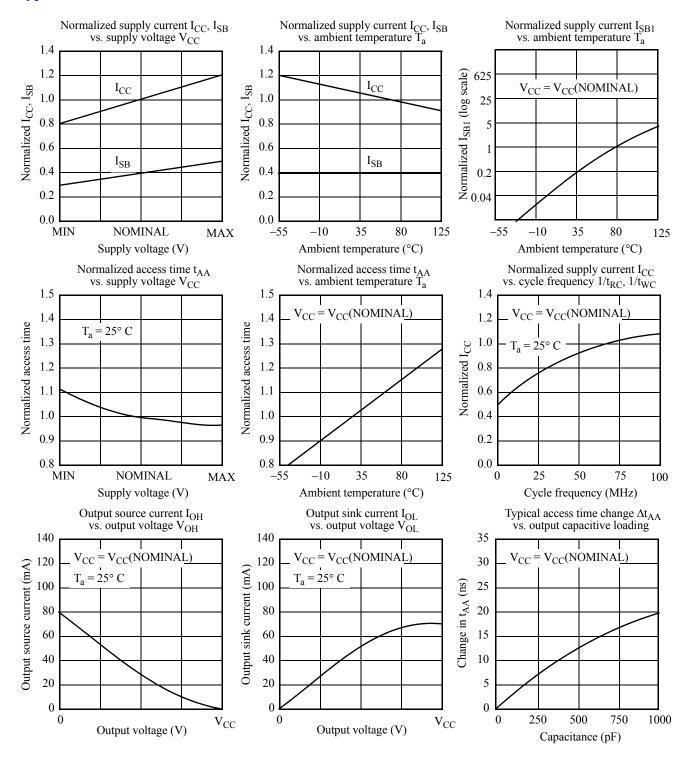
Figure C: 3.3V Output load

Notes

- During V_{CC} power-up, a pull-up resistor to V_{CC} on \overline{CE} is required to meet I_{SB} specification. 1
- This parameter is sampled, but not 100% tested. 2
- 3 For test conditions, see AC Test Conditions.
- 4 t_{CLZ} and t_{CHZ} are specified with C_L = 5pF as in Figure C. Transition is measured ± 500 mV from steady-state voltage.
- This parameter is guaranteed, but not tested. 5
- 6 WE is HIGH for read cycle.
- $\overline{\text{CE}}$ and $\overline{\text{OE}}$ are LOW for read cycle. 7
- Address valid prior to or coincident with $\overline{\text{CE}}$ transition Low. 8
- 9 All read cycle timings are referenced from the last valid address to the first transitioning address.
- $\overline{\text{CE}}$ or $\overline{\text{WE}}$ must be HIGH during address transitions. Either $\overline{\text{CE}}$ or $\overline{\text{WE}}$ asserting high terminates a write cycle.
- 11 All write cycle timings are referenced from the last valid address to the first transitioning address.
- 12 Not applicable.
- 13 C = 30pF, except at high Z and low Z parameters, where C = 5pF.

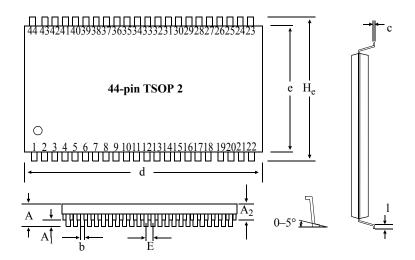


Typical DC and AC characteristics 12

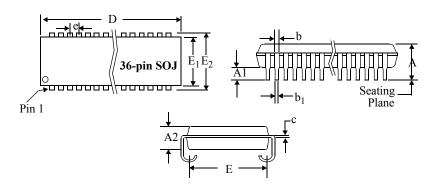




Package dimensions



	44-pin '	TSOP 2					
	Min (mm)	Max (mm)					
A		1.2					
$\mathbf{A_1}$	0.05	0.15					
A ₂	0.95	1.05					
b	0.30	0.45					
c	0.12	0.21					
d	18.31	18.52					
e	10.06	10.26					
H _e	11.68	11.94					
E	0.80 (typical)						
l	0.40	0.60					



	36-pin	SOJ 400
	Min(mm)	Max(mm)
A	.128	0.148
$\mathbf{A_1}$	0.025	_
A ₂	0.105	0.115
b	0.015	0.020
b ₁	0.026	0.032
c	0.007	0.013
D	.920	.930
e	0.045	0.055
E 1	0.395	0.405
E2	0.435	0.445
E	0.370	BSC



Ordering codes

Package	Version	10 ns	12 ns	15 ns	20 ns
	5V commercial	NA	AS7C4096-12JC	AS7C4096-15JC	AS7C4096-20JC
SOJ	5V industrial	NA	AS7C4096-12JI	AS7C4096-15JI	AS7C4096-20JI
303	3.3V commercial	AS7C34096-10JC	AS7C34096-12JC	AS7C34096-15JC	AS7C34096-20JC
	3.3V industrial	NA	AS7C34096-12JI	AS7C34096-15JI	AS7C34096-20JI
	5V commercial	NA	AS7C4096-12TC	AS7C4096-15TC	AS7C4096-20TC
TSOP 2	5V industrial	NA	AS7C4096-12TI	AS7C4096-15TI	AS7C4096-20TI
1501 2	3.3V commercial	AS7C34096-10TC	AS7C34096-12TC	AS7C34096-15TC	AS7C34096-20TC
	3.3V industrial	NA	AS7C34096-12TI	AS7C34096-15TI	AS7C34096-20TI

Note:

Add suffix "N" to the above part number for lead free devices, Ex. AS7C4096-12JCN

Part numbering system

AS7C	X	4096	-XX	J or T	X	N
SRAM prefix	Voltage: Blank: 5V CMOS 3: 3.3V CMOS	Device number	Access time	Packages: J: SOJ 400 mil T: TSOP 2	Temperature ranges: C: Commercial, 0°C to 70°C I: Industrial, –40°C to 85°C	

1/13/05; **v.1.9**

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