



# ESD Protected, EMC Compliant, 3.3 V, 20 Mbps, EIA RS-485 Transceiver

## ADM3485E

### FEATURES

- Operates with +3.3 V Supply
- ESD Protection: 8 kV Meets IEC1000-4-2
- EFT Protection: 2 kV Meets IEC1000-4-4
- EIA RS-422 and RS-485 Compliant Over Full CM Range
- 19 k $\Omega$  Input Impedance
- Up to 50 Transceivers on Bus
- 20 Mbps Data Rate
- Short Circuit Protection
- Specified Over Full Temperature Range
- Thermal Shutdown
- Interoperable with 5 V Logic
- 1 mA Supply Current
- 2 nA Shutdown Current
- 8 ns Skew

### APPLICATIONS

- Telecommunications
- DTE-DCE Interface
- Packet Switching
- Local Area Networks
- Data Concentration
- Data Multiplexers
- Integrated Services Digital Network (ISDN)
- AppleTalk
- Industrial Controls

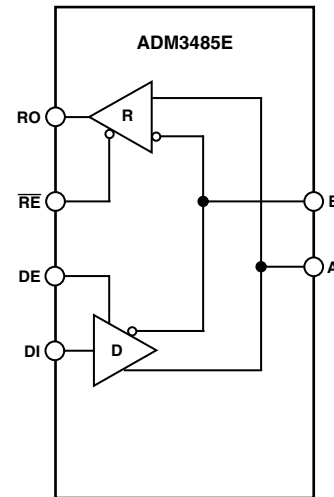
### GENERAL DESCRIPTION

The ADM3485E is a low power differential line transceiver designed to operate using a single +3.3 V power supply. Low power consumption makes it ideal for power sensitive applications. It is suitable for communication on multipoint bus transmission lines. Internal protection against electrostatic discharge (ESD) and electrical fast transient (EFT) allows operation in electrically harsh environments.

It is intended for balanced data transmission and complies with both EIA Standards RS-485 and RS-422. It contains a differential line driver and a differential line receiver, and is suitable for half duplex data transfer.

The input impedance is 19 k $\Omega$  allowing up to 50 transceivers to be connected on the bus.

### FUNCTIONAL BLOCK DIAGRAM



Excessive power dissipation caused by bus contention or by output shorting is prevented by a thermal shutdown circuit. This feature forces the driver output into a high impedance state if, during fault conditions, a significant temperature increase is detected in the internal driver circuitry.

The receiver contains a fail-safe feature that results in a logic high output state if the inputs are unconnected (floating).

The ADM3485E is fabricated on BiCMOS, an advanced mixed technology process combining low power CMOS with fast switching bipolar technology.

The ADM3485E is fully specified over the industrial temperature range and is available in 8-lead DIP and SOIC packages.

### REV. A

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# ADM3485E—SPECIFICATIONS ( $V_{CC} = +3.3\text{ V} \pm 0.3\text{ V}$ . All specifications $T_{MIN}$ to $T_{MAX}$ unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
<b>DRIVER</b>					
Differential Output Voltage, $V_{OD}$	2.0			V	$R_L = 100\ \Omega$ , Figure 1, $V_{CC} > 3.1\text{ V}$
	1.5			V	$R_L = 54\ \Omega$ , Figure 1
	1.5			V	$R_L = 60\ \Omega$ , Figure 2, $-7\text{ V} < V_{TST} < +12\text{ V}$
$\Delta V_{OD} $ for Complementary Output States			0.2	V	$R = 54\ \Omega$ or $100\ \Omega$ , Figure 1
Common-Mode Output Voltage $V_{OC}$			3	V	$R = 54\ \Omega$ or $100\ \Omega$ , Figure 1
$\Delta V_{OC} $ for Complementary Output States			0.2	V	$R = 54\ \Omega$ or $100\ \Omega$ , Figure 1
CMOS Input Logic Threshold Low, $V_{INL}$			0.8	V	
CMOS Input Logic Threshold High, $V_{INH}$	2.0			V	
Logic Input Current (DE, DI, $\overline{RE}$ )			$\pm 1.0$	$\mu\text{A}$	
Output Short Circuit Current			$\pm 250$	mA	$V_O = -7\text{ V}$ or $+12\text{ V}$
<b>RECEIVER</b>					
Differential Input Threshold Voltage, $V_{TH}$	-0.2		+0.2	V	$-7\text{ V} < V_{CM} < +12\text{ V}$
Input Voltage Hysteresis, $\Delta V_{TH}$		50		mV	$V_{CM} = 0\text{ V}$
Input Resistance	12	19		k $\Omega$	$-7\text{ V} < V_{CM} < +12\text{ V}$
Input Current (A, B)			+1	mA	$V_{IN} = +12\text{ V}$
			-0.8	mA	$V_{IN} = -7\text{ V}$
Logic Enable Input Current ( $\overline{RE}$ )			$\pm 1$	$\mu\text{A}$	
Output Voltage Low, $V_{OL}$			0.4	V	$I_{OUT} = +2.5\text{ mA}$
Output Voltage High, $V_{OH}$	$V_{CC} - 0.4\text{ V}$			V	$I_{OUT} = -1.5\text{ mA}$
Short Circuit Output Current			$\pm 60$	mA	$V_{OUT} = \text{GND}$ or $V_{CC}$
Three-State Output Leakage Current			$\pm 1.0$	$\mu\text{A}$	$V_{CC} = 3.6\text{ V}$ , $0\text{ V} < V_{OUT} < V_{CC}$
<b>POWER SUPPLY CURRENT</b>					
$I_{CC}$					Outputs Unloaded,
		1	1.2	mA	DE = $V_{CC}$ , $\overline{RE} = 0\text{ V}$
		1	1.2	mA	DE = $0\text{ V}$ , $\overline{RE} = 0\text{ V}$
Supply Current in Shutdown		0.002	1	$\mu\text{A}$	DE = $0\text{ V}$ , $\overline{RE} = V_{CC}$
<b>ESD/EFT IMMUNITY</b>					
ESD Protection		$\pm 8$		kV	IEC1000-4-2 A, B Pins Contact Discharge
EFT Protection		$\pm 2$		kV	IEC1000-4-4, A, B Pins

Specifications subject to change without notice.

**TIMING SPECIFICATIONS** ( $V_{CC} = +3.3\text{ V}$ ,  $T_A = +25^\circ\text{C}$ )

Parameter	Min	Typ	Max	Units	Test Conditions/ Comments
<b>DRIVER</b>					
Differential Output Delay $T_{DD}$	1		35	ns	$R_L = 60\ \Omega$ , $C_{L1} = C_{L2} = 15\ \text{pF}$ , Figure 3
Differential Output Transition Time	1	8	15	ns	$R_L = 60\ \Omega$ , $C_{L1} = C_{L2} = 15\ \text{pF}$ , Figure 3
Propagation Delay Input to Output $T_{PLH}$ , $T_{PHL}$	7	22	35	ns	$R_L = 27\ \Omega$ , $C_{L1} = C_{L2} = 15\ \text{pF}$ , Figure 7
Driver O/P to O/P $T_{SKEW}$			8	ns	$R_L = 54\ \Omega$ , $C_{L1} = C_{L2} = 15\ \text{pF}$ , Figure 3
<b>ENABLE/DISABLE</b>					
Driver Enable to Output Valid		45	90	ns	$R_L = 110\ \Omega$ , $C_L = 50\ \text{pF}$ , Figure 2
Driver Disable Timing		40	80	ns	$R_L = 110\ \Omega$ , $C_L = 50\ \text{pF}$ , Figure 2
Driver Enable from Shutdown		650	110	ns	$R_L = 110\ \Omega$ , $C_L = 15\ \text{pF}$ , Figure 2
<b>RECEIVER</b>					
Time to Shutdown	80	190	300	ns	
Propagation Delay Input to Output $T_{PLH}$ , $T_{PHL}$	25	65	90	ns	$C_L = 15\ \text{pF}$ , Figure 8
Skew $T_{PLH} - T_{PHL}$			10	ns	$C_L = 15\ \text{pF}$ , Figure 8
Receiver Enable $T_{EN}$		25	50	ns	$C_L = 15\ \text{pF}$ , Figure 6
Receiver Disable $T_{DEN}$		25	45	ns	$C_L = 15\ \text{pF}$ , Figure 6
Receiver Enable from Shutdown			500	ns	$C_L = 15\ \text{pF}$ , Figure 6

Specifications subject to change without notice.

**TIMING SPECIFICATIONS** ( $V_{CC} = +3.3\text{ V} \pm 0.3\text{ V}$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ )

Parameter	Min	Typ	Max	Units	Test Conditions/ Comments
<b>DRIVER</b>					
Differential Output Delay $T_{DD}$	1		70	ns	$R_L = 60\ \Omega$ , $C_{L1} = C_{L2} = 15\ \text{pF}$ , Figure 3
Differential Output Transition Time	2	8	15	ns	$R_L = 60\ \Omega$ , $C_{L1} = C_{L2} = 15\ \text{pF}$ , Figure 3
Propagation Delay Input to Output $T_{PLH}$ , $T_{PHL}$	7	22	70	ns	$R_L = 27\ \Omega$ , $C_{L1} = C_{L2} = 15\ \text{pF}$ , Figure 7
Driver O/P to O/P $T_{SKEW}$			10	ns	$R_L = 54\ \Omega$ , $C_{L1} = C_{L2} = 15\ \text{pF}$ , Figure 3
<b>ENABLE/DISABLE</b>					
Driver Enable to Output Valid		45	110	ns	$R_L = 110\ \Omega$ , $C_L = 50\ \text{pF}$ , Figure 2
Driver Disable Timing		40	110	ns	$R_L = 110\ \Omega$ , $C_L = 50\ \text{pF}$ , Figure 2
Driver Enable from Shutdown		650	110	ns	$R_L = 110\ \Omega$ , $C_L = 15\ \text{pF}$ , Figure 2
<b>RECEIVER</b>					
Time to Shutdown	50	190	500	ns	
Propagation Delay Input to Output $T_{PLH}$ , $T_{PHL}$	25	65	115	ns	$C_L = 15\ \text{pF}$ , Figure 8
Skew $T_{PLH} - T_{PHL}$			20	ns	$C_L = 15\ \text{pF}$ , Figure 8
Receiver Enable $T_{EN}$		25	50	ns	$C_L = 15\ \text{pF}$ , Figure 6
Receiver Disable $T_{DEN}$		25	50	ns	$C_L = 15\ \text{pF}$ , Figure 6
Receiver Enable from Shutdown			600	ns	$C_L = 15\ \text{pF}$ , Figure 6

Specifications subject to change without notice.

# ADM3485E

## ABSOLUTE MAXIMUM RATINGS\*

(T<sub>A</sub> = +25°C unless otherwise noted)

V <sub>CC</sub> .....	+7 V
<b>Inputs</b>	
Driver Input (DI) .....	-0.3 V to V <sub>CC</sub> + 0.3 V
Control Inputs (DE, $\overline{RE}$ ) .....	-0.3 V to V <sub>CC</sub> + 0.3 V
Receiver Inputs (A, B) .....	-7.5 V to +12.5 V
<b>Outputs</b>	
Driver Outputs .....	-7.5 V to +12.5 V
Receiver Output .....	-0.5 V to V <sub>CC</sub> + 0.5 V
Power Dissipation 8-Lead DIP .....	800 mW
$\theta_{JA}$ , Thermal Impedance .....	140°C/W
Power Dissipation 8-Lead SOIC .....	650 mW
$\theta_{JA}$ , Thermal Impedance .....	115°C/W

## Operating Temperature Range

Industrial (A Version) .....	-40°C to +85°C
Storage Temperature Range .....	-65°C to +150°C
Lead Temperature (Soldering, 10 sec) .....	+300°C
Vapor Phase (60 sec) .....	+215°C
Infrared (15 sec) .....	+220°C
ESD Rating: Air (Human Body Model, All Pins) .....	>4 kV
ESD Rating: IEC1000-4-2 Contact (A, B Pins) .....	>8 kV
EFT Rating: IEC1000-4-4 (A, B Pins) .....	>2 kV

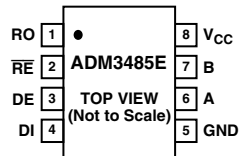
\*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
ADM3485EAN	-40°C to +85°C	Plastic DIP	N-8
ADM3485EAR	-40°C to +85°C	Small Outline (SOIC)	SO-8

## PIN CONFIGURATION

### DIP/SOIC



## PIN FUNCTION DESCRIPTIONS

Mnemonic Pin	DIP/SOIC	Function
RO	1	Receiver Output. High when A > B by 200 mV or low when A < B by 200 mV.
$\overline{RE}$	2	Receiver Output Enable. With $\overline{RE}$ low, the receiver output RO is enabled. With $\overline{RE}$ high, the output goes high impedance. If $\overline{RE}$ is high and DE low, the ADM3485E enters a shutdown state.
DE	3	Driver Output Enable. A high level enables the driver differential outputs, A and B. A low level places it in a high impedance state.
DI	4	Driver Input. When the driver is enabled, a logic low on DI forces A low and B high, while a logic high on DI forces A high and B low.
GND	5	Ground Connection, 0 V.
A	6	Noninverting Receiver Input A/Driver Output A.
B	7	Inverting Receiver Input B/Driver Output B.
V <sub>CC</sub>	8	Power Supply, 3.3 V ± 0.3 V.

## Test Circuits

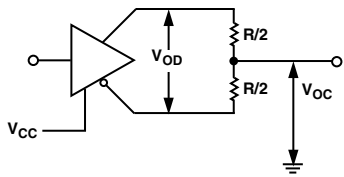


Figure 1. Driver Voltage Measurement Test Circuit

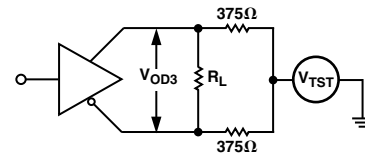


Figure 5. Driver Voltage Measurement Test Circuit 2

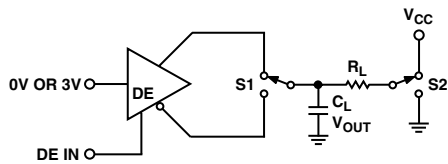


Figure 2. Driver Enable/Disable Test Circuit

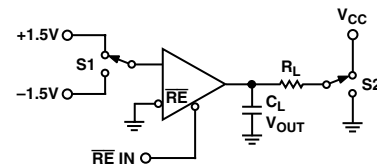


Figure 6. Receiver Enable/Disable Test Circuit

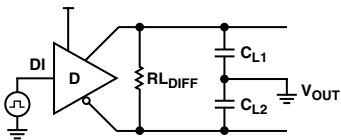


Figure 3. Driver Differential Output Delay Test Circuit

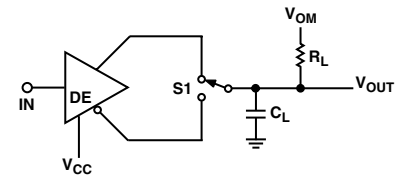


Figure 7. Driver Propagation Delay Test Circuit

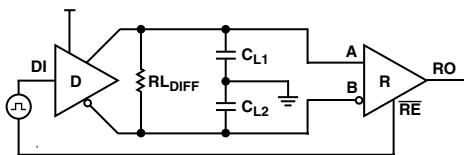


Figure 4. Driver/Receiver Propagation Delay Test Circuit

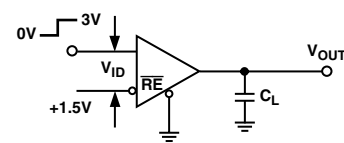


Figure 8. Receiver Propagation Delay Test Circuit

# ADM3485E

## Switching Characteristics

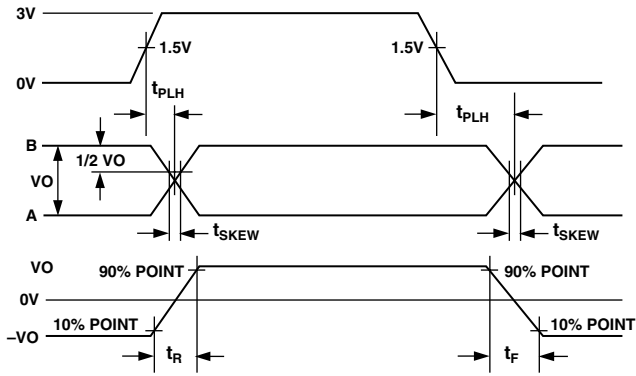


Figure 9. Driver Propagation Delay, Rise/Fall Timing

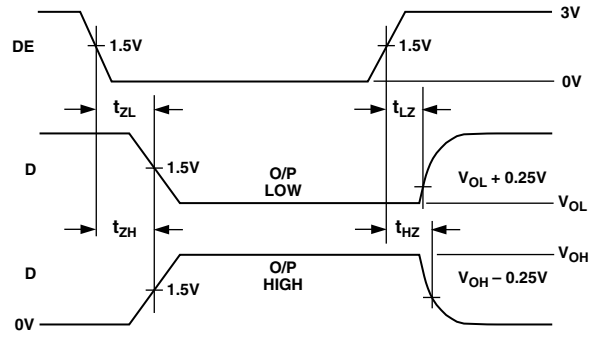


Figure 11. Driver Enable/Disable Timing

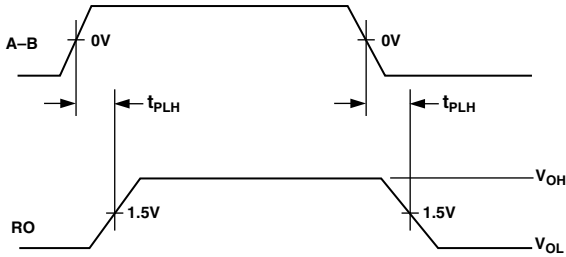


Figure 10. Receiver Propagation Delay

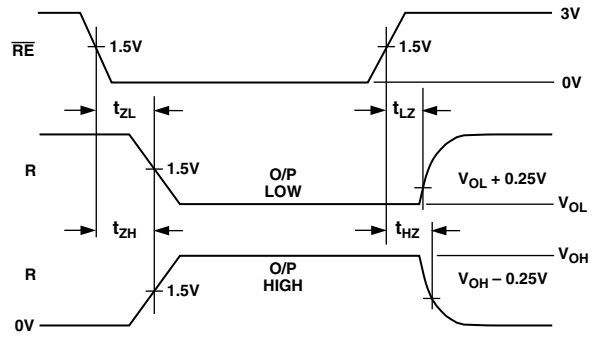


Figure 12. Receiver Enable/Disable Timing

# Typical Performance Characteristics—ADM3485E

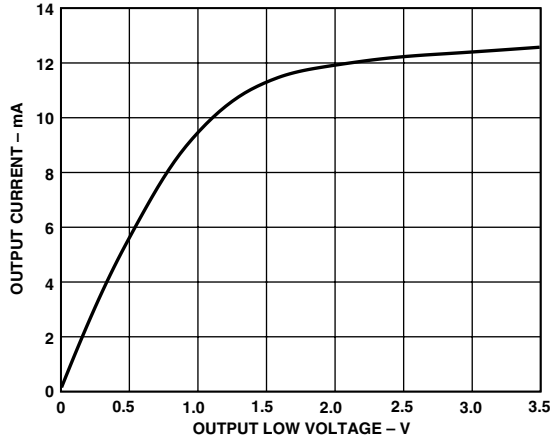


Figure 13. Output Current vs. Receiver Output Low Voltage

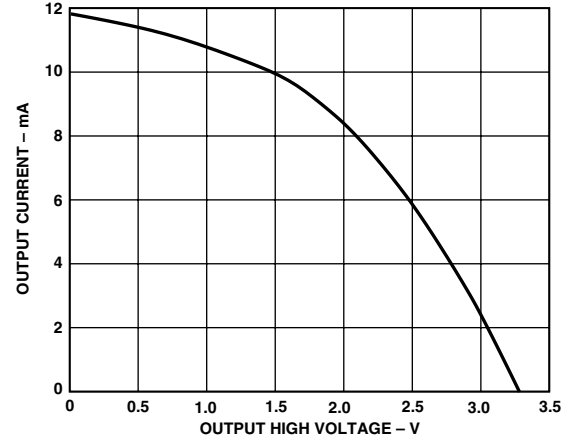


Figure 16. Output Current vs. Receiver Output High Voltage

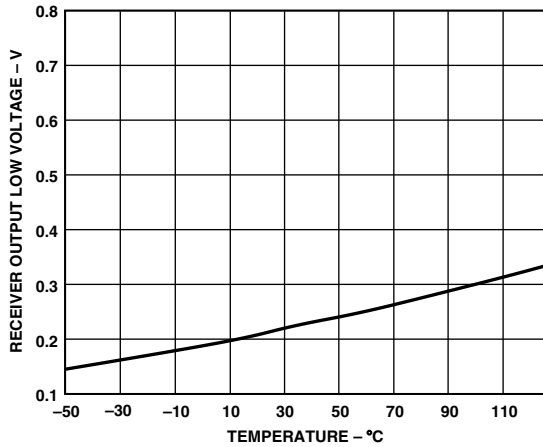


Figure 14. Receiver Output Low Voltage vs. Temperature

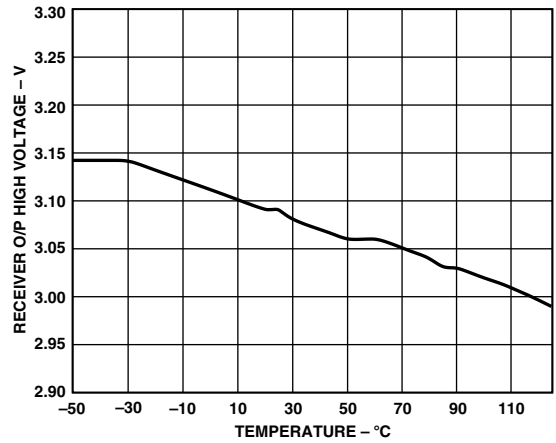


Figure 17. Receiver Output High Voltage vs. Temperature

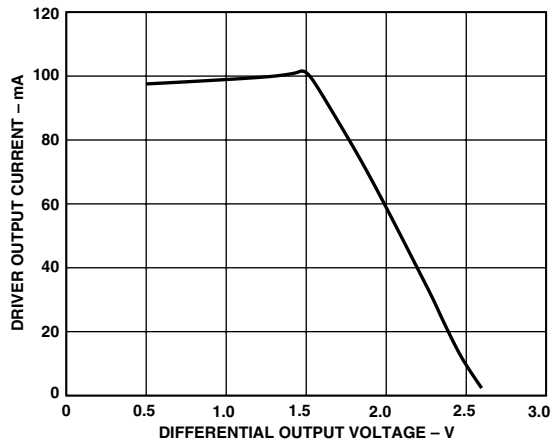


Figure 15. Driver Output Current vs. Differential Output Voltage

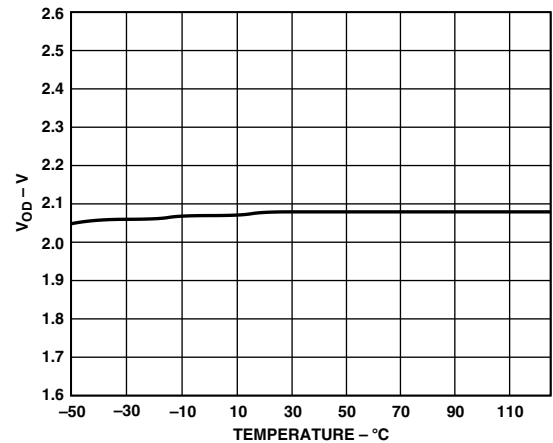


Figure 18. Driver Differential Output Voltage vs. Temperature

# ADM3485E

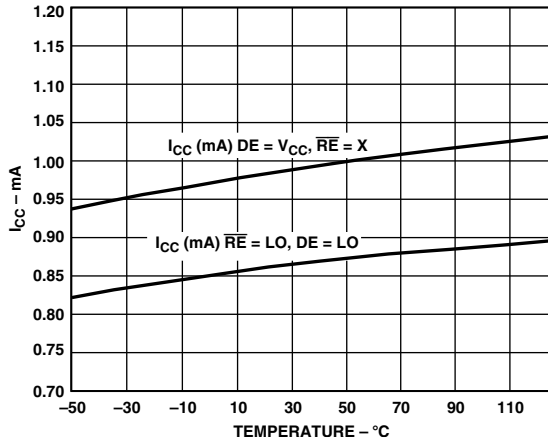


Figure 19. Supply Current vs. Temperature

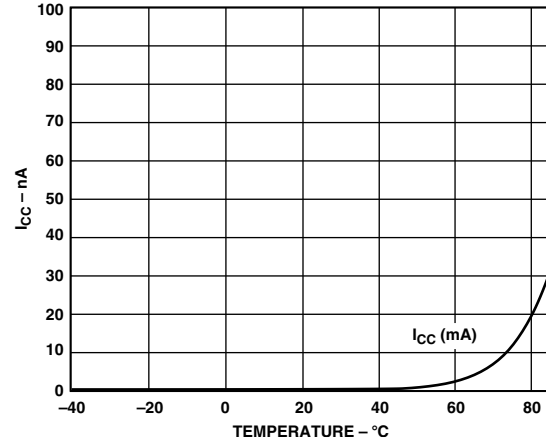


Figure 20. Shutdown Current vs. Temperature

Table I. Comparison of RS-422 and RS-485 Interface Standards

Specification	RS-422	RS-485
Transmission Type	Differential	Differential
Maximum Data Rate	10 MB/s	10 MB/s
Maximum Cable Length	4000 ft.	4000 ft.
Minimum Driver Output Voltage	±2 V	±1.5 V
Driver Load Impedance	100 Ω	54 Ω
Receiver Input Resistance	4 kΩ min	12 kΩ min
Receiver Input Sensitivity	±200 mV	±200 mV
Receiver Input Voltage Range	-7 V to +7 V	-7 V to +12 V
No. of Drivers/Receivers Per Line	1/10	32/32

Table II. Transmitting Truth Table

Transmitting				
Inputs			Outputs	
$\overline{RE}$	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
0	0	X	Hi-Z	Hi-Z
1	0	X	Hi-Z	Hi-Z

Table III. Receiving Truth Table

Receiving			
Inputs			Outputs
$\overline{RE}$	DE	A-B	RO
0	X	> +0.2 V	1
0	X	< -0.2 V	0
0	X	Inputs O/C	1
1	X	X	Hi-Z

## ESD/EFT TRANSIENT PROTECTION SCHEME

The ADM3485E uses protective clamping structures on its inputs and outputs that clamp the voltage to a safe level and dissipate the energy present in ESD (Electrostatic) and EFT (Electrical Fast Transients) discharges.

The protection structure achieves ESD protection up to ±8 kV according to IEC1000-4-2, and EFT protection up to ±2 kV on all I-O lines.

## ESD TESTING

Two coupling methods are used for ESD testing, contact discharge and air-gap discharge. Contact discharge calls for a direct connection to the unit being tested. Air-gap discharge uses a higher test voltage but does not make direct contact with the unit under test. With air discharge, the discharge gun is moved toward the unit under test, developing an arc across the air gap, hence the term air-discharge. This method is influenced by humidity, temperature, barometric pressure, distance and rate of closure of the discharge gun. The contact-discharge method, while less realistic, is more repeatable and is gaining acceptance and preference over the air-gap method.

Although very little energy is contained within an ESD pulse, the extremely fast rise time, coupled with high voltages, can cause failures in unprotected semiconductors. Catastrophic destruction can occur immediately as a result of arcing or heating. Even if catastrophic failure does not occur immediately, the device may suffer from parametric degradation, which may result in degraded performance. The cumulative effects of continuous exposure can eventually lead to complete failure.

I-O lines are particularly vulnerable to ESD damage. Simply touching or plugging in an I-O cable can result in a static discharge that can damage or completely destroy the interface product connected to the I-O port.

It is extremely important, therefore, to have high levels of ESD protection on the I-O lines.

It is possible that the ESD discharge could induce latchup in the device under test, so it is important that ESD testing on the I-O pins be carried out while device power is applied. This type of testing is more representative of a real-world I-O discharge where the equipment is operating normally when the discharge occurs.



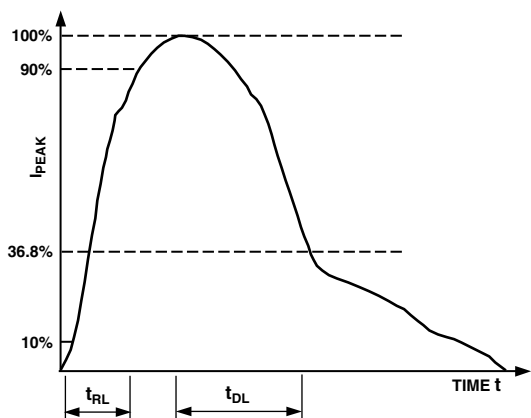


Figure 21. Human Body Model Current Waveform

Table IV. ESD Test Results

ESD Test Method	I-O Pins
IEC1000-4-2: Contact	± 8 kV

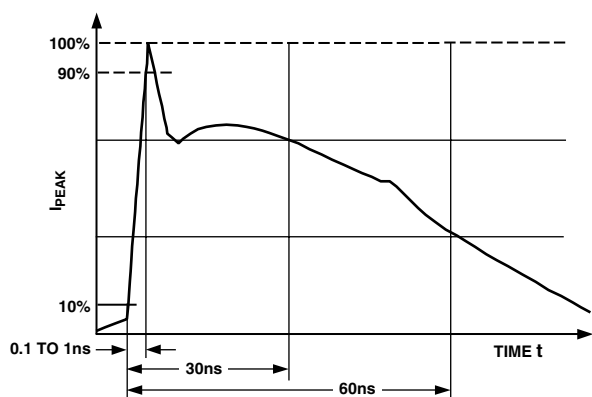


Figure 22. IEC1000-4-2 ESD Current Waveform

### FAST TRANSIENT BURST IMMUNITY (IEC1000-4-4)

IEC1000-4-4 (previously 801-4) covers electrical fast-transient/burst (EFT) immunity. Electrical fast transients occur as a result of arcing contacts in switches and relays. The tests simulate the interference generated when, for example, a power relay disconnects an inductive load. A spark is generated due to the well known back EMF effect. In fact, the spark consists of a burst of sparks as the relay contacts separate. The voltage appearing on the line, therefore, consists of a burst of extremely fast transient impulses. A similar effect occurs when switching on fluorescent lights.

The fast transient burst test, defined in IEC1000-4-4, simulates this arcing and its waveform is illustrated in Figure 23. It consists of a burst of 2.5 kHz to 5 kHz transients repeating at 300 ms intervals. It is specified for both power and data lines.

Four severity levels are defined in terms of an open-circuit voltage as a function of installation environment. The installation environments are defined as

1. Well-Protected
2. Protected
3. Typical Industrial
4. Severe Industrial

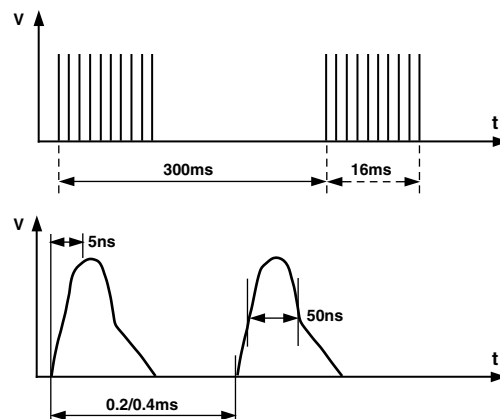


Figure 23. IEC1000-4-4 Fast Transient Waveform

Table V shows the peak voltages for each of the environments.

Table V. Peak Voltages

Level	V <sub>PEAK</sub> (kV) PSU	V <sub>PEAK</sub> (kV) I-O
1	0.5	0.25
2	1	0.5
3	2	1
4	4	2

A simplified circuit diagram of the actual EFT generator is illustrated in Figure 24.

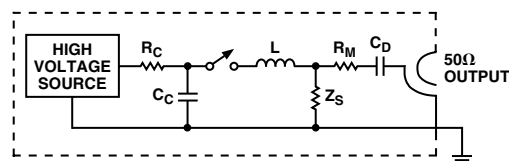


Figure 24. EFT Generator

These transients are coupled onto the signal lines using an EFT coupling clamp. The clamp is 1 m long and completely surrounds the cable, providing maximum coupling capacitance (50 pF to 200 pF typ) between the clamp and the cable. High energy transients are capacitively coupled onto the signal lines. Fast rise times (5 ns) as specified by the standard result in very effective coupling. This test is very severe since high voltages are coupled onto the signal lines. The repetitive transients can often cause problems, where single pulses do not. Destructive latchup may be induced due to the high energy content of the transients. Note that this stress is applied while the interface products are powered up and are transmitting data. The EFT test applies hundreds of pulses with higher energy than ESD. Worst case transient current on an I-O line can be as high as 40 A.

# ADM3485E

Test results are classified according to the following

1. Normal performance within specification limits.
2. Temporary degradation or loss of performance that is self-recoverable.
3. Temporary degradation or loss of function or performance that requires operator intervention or system reset.
4. Degradation or loss of function that is not recoverable due to damage.

## APPLICATIONS INFORMATION

### Differential Data Transmission

Differential data transmission is used to reliably transmit data at high rates over long distances and through noisy environments. Differential transmission nullifies the effects of ground shifts and noise signals that appear as common-mode voltages on the line.

Two main standards are approved by the Electronics Industries Association (EIA) which specify the electrical characteristics of transceivers used in differential data transmission. The RS-422 standard specifies data rates up to 10 MBaud and line lengths up to 4000 ft. A single driver can drive a transmission line with up to 10 receivers.

The RS-485 standard was defined to cater to true multipoint communications. This standard meets or exceeds all the requirements of RS-422, but also allows multiple drivers and receivers to be connected to a single bus. An extended common-mode range of  $-7\text{ V}$  to  $+12\text{ V}$  is defined.

The most significant difference between RS-422 and RS-485 is the fact that the drivers may be disabled thereby allowing more than one to be connected to a single line. Only one driver should be enabled at a time, but the RS-485 standard contains additional specifications to guarantee device safety in the event of line contention.

### Cable and Data Rate

The transmission line of choice for RS-485 communications is a twisted pair. Twisted pair cable tends to cancel common-mode noise and also causes cancellation of the magnetic fields generated by the current flowing through each wire, thereby reducing the effective inductance of the pair.

The ADM3485E is designed for bidirectional data communications on multipoint transmission lines. A typical application showing a multipoint transmission network is illustrated in Figure 23. Only one driver can transmit at a particular time, but multiple receivers may be enabled simultaneously.

As with any transmission line, it is important that reflections are minimized. This may be achieved by terminating the extreme ends of the line using resistors equal to the characteristic impedance of the line. Stub lengths of the main line should also be kept as short as possible. A properly terminated transmission line appears purely resistive to the driver.

### Receiver Open-Circuit Fail-Safe

The receiver input includes a fail-safe feature that guarantees a logic high on the receiver when the inputs are open circuit or floating.

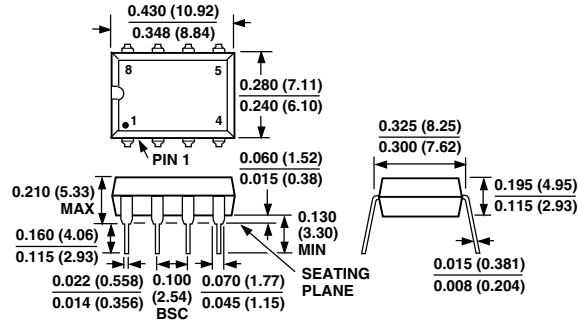
**Table VI. Comparison of RS-422 and RS-485 Interface Standards**

Specification	RS-422	RS-485
Transmission Type	Differential	Differential
Maximum Cable Length	4000 ft.	4000 ft.
Minimum Driver Output Voltage	$\pm 2\text{ V}$	$\pm 1.5\text{ V}$
Driver Load Impedance	100 $\Omega$	54 $\Omega$
Receiver Input Resistance	4 k $\Omega$ min	12 k $\Omega$ min
Receiver Input Sensitivity	$\pm 200\text{ mV}$	$\pm 200\text{ mV}$
Receiver Input Voltage Range	$-7\text{ V}$ to $+7\text{ V}$	$-7\text{ V}$ to $+12\text{ V}$

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Plastic DIP  
(N-8)



8-Lead SOIC  
(SO-8)

