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**REVISION HISTORY****8/08—Rev. C to Rev. D**

Changes to Features Section .....	1
Changes to General Description Section .....	1
Changes to Figure 1 .....	1
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Change to Figure 2 .....	5
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**3/06—Rev. B to Rev. C**

Updated Format .....	Universal
Changed Product Description to General Description .....	1
Changes to General Description .....	1
Changes to Table 1 .....	3
Changes to Table 2 .....	5
Added Pin Configurations and Function Descriptions .....	6
Changed Standard Connection to Typical Connections .....	8
Changed Single Supply Connection to Single Supply Operation .....	9
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**6/99—Rev. A to Rev. B****1/76—Revision 0: Initial Version**

# SPECIFICATIONS

T<sub>A</sub> = +25°C and ±15 V dc, unless otherwise noted.

Table 1.

Parameter	AD536AJ			AD536AK			AD536AS			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TRANSFER FUNCTION	$V_{OUT} = \sqrt{\text{Avg}(V_{IN})^2}$			$V_{OUT} = \sqrt{\text{Avg}(V_{IN})^2}$			$V_{OUT} = \sqrt{\text{Avg}(V_{IN})^2}$			
CONVERSION ACCURACY										
Total Error, Internal Trim <sup>1</sup> (See Figure 6)	±5 ± 0.5			±2 ± 0.2			±5 ± 0.5			mV ± % of rdg
vs. Temperature										
T <sub>MIN</sub> to +70°C	±0.1 ± 0.01			±0.05 ± 0.005			±0.1 ± 0.005			mV ± % of rdg/°C
+70°C to +125°C							±0.3 ± 0.005			mV ± % of rdg/°C
vs. Supply Voltage	±0.1 ±0.01			±0.1 ± 0.01			±0.1 ±0.01			mV ± % of rdg/°C
dc Reversal Error	±0.2			±0.1			±0.2			mV ± % of rdg
Total Error, External Trim <sup>1</sup> (See Figure 9)	±3 ± 0.3			±2 ± 0.1			±3 ± 0.3			mV ± % of rdg
ERROR VS. CREST FACTOR <sup>2</sup>										
Crest Factor 1 to Crest Factor 2	Specified accuracy			Specified accuracy			Specified accuracy			
Crest Factor = 3	-0.1			-0.1			-0.1			% of rdg
Crest Factor = 7	-1.0			-1.0			-1.0			% of rdg
FREQUENCY RESPONSE <sup>3</sup>										
Bandwidth for 1% Additional Error (0.09 dB)										
V <sub>IN</sub> = 10 mV	5			5			5			kHz
V <sub>IN</sub> = 100 mV	45			45			45			kHz
V <sub>IN</sub> = 1 V	120			120			120			kHz
±3 dB Bandwidth										
V <sub>IN</sub> = 10 mV	90			90			90			kHz
V <sub>IN</sub> = 100 mV	450			450			450			kHz
V <sub>IN</sub> = 1 V	2.3			2.3			2.3			MHz
AVERAGING TIME CONSTANT (See Figure 12)	25			25			25			ms/μF
INPUT CHARACTERISTICS										
Signal Range, ±15 V Supplies										
Continuous RMS Level	0 to 7			0 to 7			0 to 7			V rms
Peak Transient Input	±20			±20			±20			V peak
Continuous RMS Level, V <sub>S</sub> = ±5 V	0 to 2			0 to 2			0 to 2			V rms
Peak Transient Input, V <sub>S</sub> = ±5 V	±7			±7			±7			V peak
Maximum Continuous Nondestructive Input Level (All Supply Voltages)	±25			±25			±25			V peak
Input Resistance	13.33	16.67	20	13.33	16.67	20	13.33	16.67	20	kΩ
Input Offset Voltage	0.8 ±2			0.5 ±1			0.8 ±2			mV
OUTPUT CHARACTERISTICS										
Offset Voltage, V <sub>IN</sub> = COM (See Figure 6)	±1 ±2			±0.5 ±1			±2			mV
vs. Temperature	±0.1			±0.1			±0.2			mV/°C
vs. Supply Voltage	±0.1			±0.1			±0.2			mV/V
Voltage Swing, ±15 V Supplies	0 to +11	+12.5		0 to +11	+12.5		0 to +11	+12.5		V
±5 V Supply	0 to +2			0 to +2			0 to +2			V
dB OUTPUT, 0 dB = 1 V rms (See Figure 17)										
Error, 7 mV < V <sub>IN</sub> < 7 V rms	±0.4 ±0.6			±0.2 ±0.3			±0.5 ±0.6			dB
Scale Factor	-3			-3			-3			mV/dB
Scale Factor Temperature Coefficient	-0.033			-0.033			-0.033			dB/°C
Uncompensated	+0.33			+0.33			+0.33			% of rdg/°C
I <sub>REF</sub> for 0 dB = 1 V rms	5	20	80	5	20	80	5	20	80	μA
I <sub>REF</sub> Range	1		100	1		100	1		100	μA

# AD536A

Parameter	AD536AJ			AD536AK			AD536AS			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
<b>OUTPUT TERMINAL</b>										
$I_{OUT}$ Scale Factor		40			40			40		$\mu\text{A/V rms}$
$I_{OUT}$ Scale Factor Tolerance		$\pm 10$	$\pm 20$		$\pm 10$	$\pm 20$		$\pm 10$	$\pm 20$	%
Output Resistance	20	25	30	20	25	30	20	25	30	$\text{k}\Omega$
Voltage Compliance		$-V_S$ to ( $+V_S - 2.5\text{ V}$ )			$-V_S$ to ( $+V_S - 2.5\text{ V}$ )			$-V_S$ to ( $+V_S - 2.5\text{ V}$ )		V
<b>BUFFER AMPLIFIER</b>										
Input and Output Voltage Range	$-V_S$ to ( $+V_S - 2.5\text{ V}$ )			$-V_S$ to ( $+V_S - 2.5\text{ V}$ )			$-V_S$ to ( $+V_S - 2.5\text{ V}$ )			V
Input Offset Voltage, $R_S = 25\text{ k}\Omega$		$\pm 0.5$	$\pm 4$		$\pm 0.5$	$\pm 4$		$\pm 0.5$	$\pm 4$	mV
Input Bias Current		20	60		20	60		20	60	nA
Input Resistance		$10^8$			$10^8$			$10^8$		$\Omega$
Output Current	(+5 mA, $-130\text{ }\mu\text{A}$ )			(+5 mA, $-130\text{ }\mu\text{A}$ )			(+5 mA, $-130\text{ }\mu\text{A}$ )			
Short-Circuit Current		20			20			20		mA
Output Resistance			0.5			0.5			0.5	$\Omega$
Small-Signal Bandwidth		1			1			1		MHz
Slew Rate <sup>4</sup>		5			5			5		$\text{V}/\mu\text{s}$
<b>POWER SUPPLY</b>										
Voltage Rated Performance		$\pm 15$			$\pm 15$			$\pm 15$		V
Dual Supply	$\pm 3.0$		$\pm 18$	$\pm 3.0$		$\pm 18$	$\pm 3.0$		$\pm 18$	V
Single Supply	+5		+36	+5		+36	+5		+36	V
Quiescent Current										
Total $V_S$ , 5 V to 36 V, $T_{MIN}$ to $T_{MAX}$		1.2	2		1.2	2		1.2	2	mA
<b>TEMPERATURE RANGE</b>										
Rated Performance	0		+70	0		+70	-55		+125	$^{\circ}\text{C}$
Storage	-55		+150	-55		+150	-55		+150	$^{\circ}\text{C}$
NUMBER OF TRANSISTORS		65			65			65		

<sup>1</sup> Accuracy is specified for 0 V to 7 V rms, dc or 1 kHz sine wave input with the AD536A connected as in the figure referenced.

<sup>2</sup> Error vs. crest factor is specified as an additional error for 1 V rms rectangular pulse input, pulse width = 200  $\mu\text{s}$ .

<sup>3</sup> Input voltages are expressed in volts rms, and error is expressed as a percentage of the reading.

<sup>4</sup> With 2k $\Omega$  external pull-down resistor.

## ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	
Dual Supply	±18 V
Single Supply	+36 V
Internal Power Dissipation	500 mW
Maximum Input Voltage	±25 V peak
Buffer Maximum Input Voltage	±V <sub>S</sub>
Maximum Input Voltage	±25 V peak
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	
AD536AJ/AD536AK	0°C to +70°C
AD536AS	−55°C to +125°C
Lead Temperature (Soldering, 60 sec)	300°C
ESD Rating	1000 V
Thermal Resistance $\theta_{JA}$ <sup>1</sup>	
10-Pin Header (H-10 Package)	150°C/W
20-Terminal LCC (E-20 Package)	95°C/W
14-Lead SBDIP (D-14 Package)	95°C/W
14-Lead CERDIP (Q-14 Package)	95°C/W

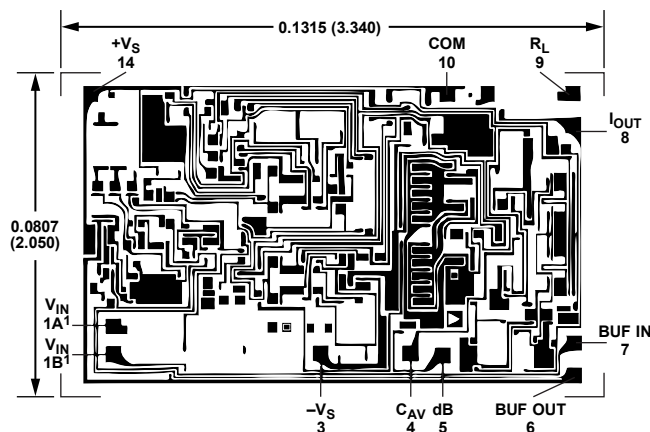
<sup>1</sup>  $\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-100 14-LEAD CERAMIC DIP PACKAGE.

<sup>1</sup>BOTH PADS SHOWN MUST BE CONNECTED TO V<sub>IN</sub>. THE AD536A IS AVAILABLE IN LASER-TRIMMED CHIP FORM. SUBSTRATE CONNECTED TO −V<sub>S</sub>.

00504-002

Figure 2. Die Dimensions and Pad Layout  
Dimensions shown in inches and (millimeters)

# AD536A

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

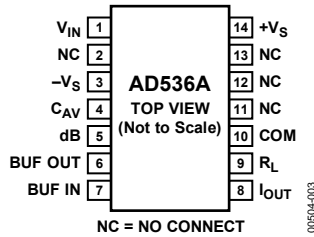


Figure 3. D-14 and Q-14 Packages Pin Configuration

Table 3. D-14 and Q-14 Packages Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$V_{IN}$	Input Voltage
2	NC	No Connection
3	$-V_S$	Negative Supply Voltage
4	$C_{AV}$	Averaging Capacitor
5	dB	Log (dB) Value of the RMS Output Voltage
6	BUF OUT	Buffer Output
7	BUF IN	Buffer Input
8	$I_{OUT}$	RMS Output Current
9	$R_L$	Load Resistor
10	COM	Common
11	NC	No Connection
12	NC	No Connection
13	NC	No Connection
14	$+V_S$	Positive Supply Voltage

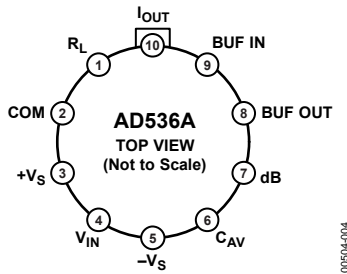


Figure 4. H-10 Package Pin Configuration

Table 4. H-10 Package Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$R_L$	Load Resistor
2	COM	Common
3	$+V_S$	Positive Supply Voltage
4	$V_{IN}$	Input Voltage
5	$-V_S$	Negative Supply Voltage
6	$C_{AV}$	Averaging Capacitor
7	dB	Log (dB) Value of the RMS Output Voltage
8	BUF OUT	Buffer Output
9	BUF IN	Buffer Input
10	$I_{OUT}$	RMS Output Current

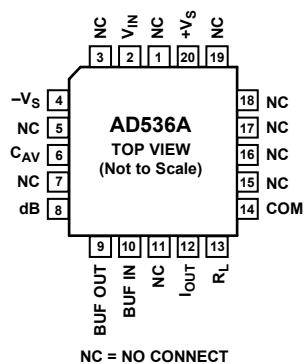


Figure 5. E-20 Package Pin Configuration

Table 5. E-20 Package Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NC	No Connection
2	$V_{IN}$	Input Voltage
3	NC	No Connection
4	$-V_S$	Negative Supply Voltage
5	NC	No Connection
6	$C_{AV}$	Averaging Capacitor
7	NC	No Connection
8	dB	Log (dB) Value of the RMS Output Voltage
9	BUF OUT	Buffer Output
10	BUF IN	Buffer Input
11	NC	No Connection
12	$I_{OUT}$	RMS Output Current
13	$R_L$	Load Resistor
14	COM	Common
15	NC	No Connection
16	NC	No Connection
17	NC	No Connection
18	NC	No Connection
19	NC	No Connection
20	$+V_S$	Positive Supply Voltage

## APPLICATIONS INFORMATION

### TYPICAL CONNECTIONS

The AD536A is simple to connect to for the majority of high accuracy rms measurements, requiring only an external capacitor to set the averaging time constant. The standard connection is shown in Figure 6 through Figure 8. In this configuration, the AD536A measures the rms of the ac and dc levels present at the input, but shows an error for low frequency input as a function of the filter capacitor,  $C_{AV}$ , as shown in Figure 12. Thus, if a 4  $\mu\text{F}$  capacitor is used, the additional average error at 10 Hz is 0.1%; at 3 Hz, the additional average error is 1%.

The accuracy at higher frequencies is according to specification. To reject the dc input, add a capacitor in series with the input, as shown in Figure 10. Note that the capacitor must be nonpolar. If the AD536A supply rails contain a considerable amount of high frequency ripple, it is advisable to bypass both supply pins to ground with 0.1  $\mu\text{F}$  ceramic capacitors, located as close to the device as possible.

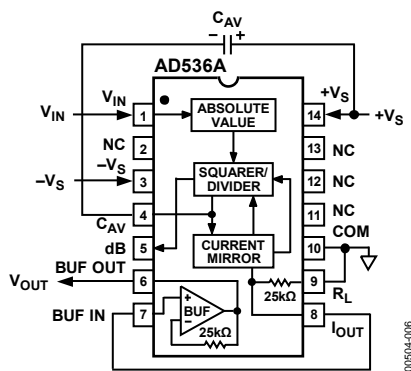


Figure 6. 14-Lead Standard RMS Connection

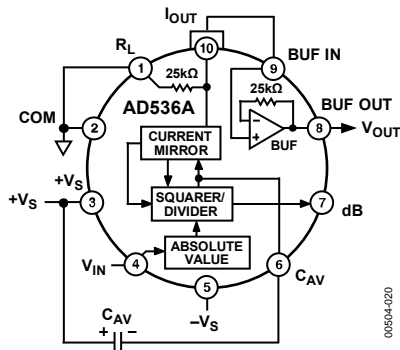


Figure 7. 10-Pin Standard RMS Connection

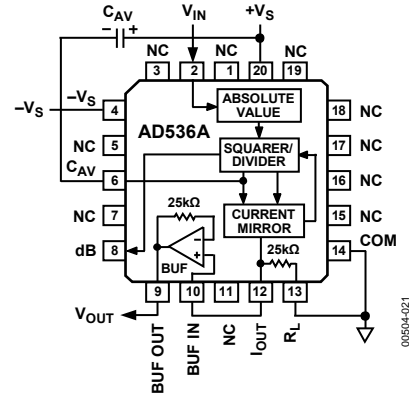


Figure 8. 20-Terminal Standard RMS Connection

The input and output signal ranges are a function of the supply voltages; these ranges are shown in Figure 21 and Figure 22. The AD536A can also be used in an unbuffered voltage output mode by disconnecting the input to the buffer. The output then appears unbuffered across the 25 k $\Omega$  resistor. The buffer amplifier can then be used for other purposes. Further, the AD536A can be used in a current output mode by disconnecting the 25 k $\Omega$  resistor from ground. The output current is available at Pin 8 ( $I_{OUT}$ , Pin 10 on the H-10 package) with a nominal scale of 40  $\mu\text{A}$  per V rms input positive output.

### OPTIONAL EXTERNAL TRIMS FOR HIGH ACCURACY

The accuracy and offset voltage of the AD536A is adjustable with external trims, as shown in Figure 9. R4 trims the offset. Note that the offset trim circuit adds 365  $\Omega$  in series with the internal 25 k $\Omega$  resistor. This causes a 1.5% increase in scale factor, which is compensated for by R1. The scale factor adjustment range is  $\pm 1.5\%$ .

The trimming procedure is as follows:

1. Ground the input signal,  $V_{IN}$ , and adjust R4 to provide 0 V output from Pin 6. Alternatively, adjust R4 to provide the correct output with the lowest expected value of  $V_{IN}$ .
2. Connect the desired full-scale input level to  $V_{IN}$ , either dc or a calibrated ac signal (1 kHz is the optimum frequency).
3. Trim R1 to provide the correct output at Pin 6. For example, 1.000 V dc input provides 1.000 V dc output. A  $\pm 1.000$  V peak-to-peak sine wave should provide a 0.707 V dc output. Any residual errors are caused by device nonlinearity.

The major advantage of external trimming is to optimize device performance for a reduced signal range; the AD536A is internally trimmed for a 7 V rms full-scale range.



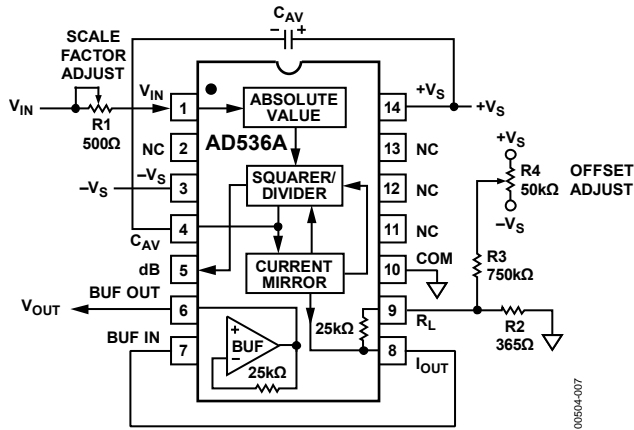


Figure 9. Optional External Gain and Output Offset Trims

## SINGLE-SUPPLY OPERATION

Dual power supplies are shown in Figure 6, Figure 7, Figure 8, and Figure 9. The AD536A can also be powered by a single supply greater than 5 V, as shown in Figure 10. When using the AD536A with a single supply, the differential input stage must be biased above ground, and the input must be ac coupled. Biasing the device between the supply and ground is simply a matter of connecting Pin 10 (COM, Pin 2 on the H-10 package) to a resistor divider and bypassing the pin to ground. To minimize power consumption, the values of the resistors may be large, as Pin 10 current is only 5  $\mu$ A.

AC input coupling requires only Capacitor C2. A dc return is not necessary because it is provided internally. C2 is selected for the proper low frequency breakpoint with the input resistance of 16.7 k $\Omega$ ; for a cutoff at 10 Hz, C2 should be 1  $\mu$ F. The signal ranges in this connection are slightly more restricted than in the dual-supply connection. The input and output signal ranges are shown in Figure 21 and Figure 22. The load resistor, R<sub>L</sub>, is necessary to provide output sink current.

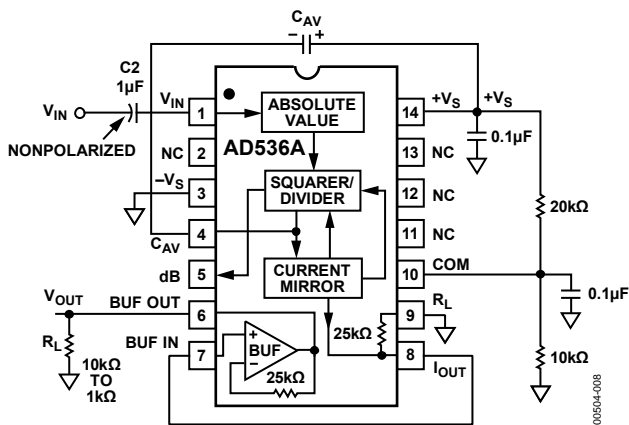


Figure 10. Single-Supply Connection

## CHOOSING THE AVERAGING TIME CONSTANT

The AD536A computes the rms of both ac and dc signals. If the input is a slowly varying dc signal, the output of the AD536A tracks the input exactly.

At higher frequencies, the average output of the AD536A approaches the rms value of the input signal. The actual output of the AD536A differs from the ideal output by a dc (or average) error and some amount of ripple, as shown in Figure 11.

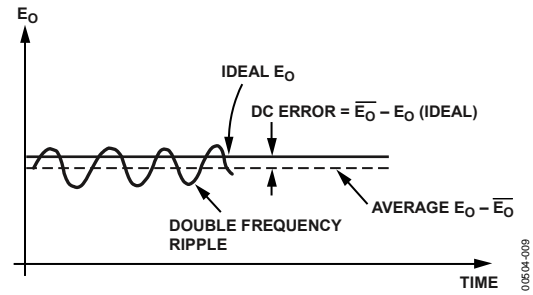


Figure 11. Typical Output Waveform for Sinusoidal Input

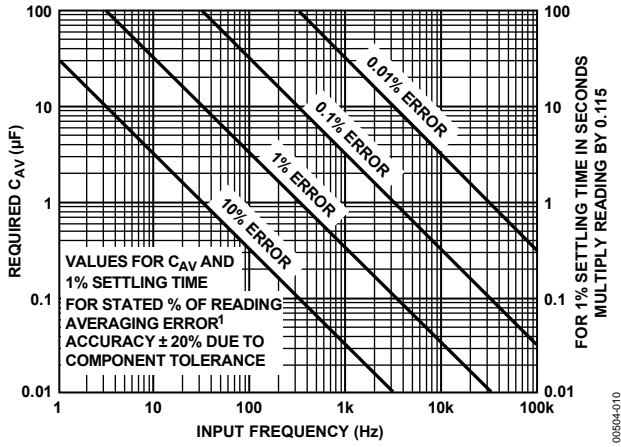
The dc error is dependent on the input signal frequency and the value of C<sub>AV</sub>. Use Figure 12 to determine the minimum value of C<sub>AV</sub>, which yields a given percentage of dc error above a given frequency using the standard rms connection.

The ac component of the output signal is the ripple. There are two ways to reduce the ripple. The first method involves using a large value of C<sub>AV</sub>. Because the ripple is inversely proportional to C<sub>AV</sub>, a tenfold increase in this capacitance affects a tenfold reduction in ripple.

When measuring waveforms with high crest factors, such as low duty cycle pulse trains, the averaging time constant should be at least 10 times the signal period. For example, a 100 Hz pulse rate requires a 100 ms time constant, which corresponds to a 4  $\mu$ F capacitor (time constant = 25 ms per  $\mu$ F).

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The primary disadvantage in using a large  $C_{AV}$  to remove ripple is that the settling time for a step change in input level is increased proportionately. Figure 12 illustrates that the relationship between  $C_{AV}$  and 1% settling time is 115 ms for each microfarad of  $C_{AV}$ . The settling time is twice as great for decreasing signals as it is for increasing signals. The values in Figure 12 are for decreasing signals. Settling time also increases for low signal levels, as shown in Figure 13.



1PERCENT DC ERROR AND PERCENT RIPPLE (PEAK)  
 Figure 12. Error/Settling Time Graph for Use with the Standard RMS Connection (See Figure 6 Through Figure 8)

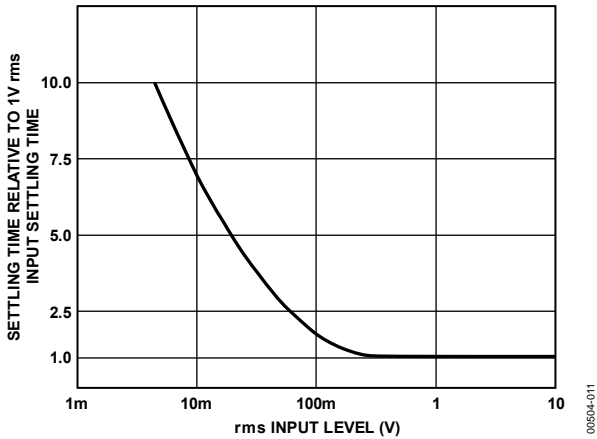


Figure 13. Settling Time vs. Input Level

A better method to reduce output ripple is the use of a postfilter. Figure 14 shows a suggested circuit. If a single-pole filter is used ( $C_3$  removed,  $R_x$  shorted) and  $C_2$  is approximately twice the value of  $C_{AV}$ , the ripple is reduced, as shown in Figure 15, and settling time is increased. For example, with  $C_{AV} = 1 \mu\text{F}$  and  $C_2 = 2.2 \mu\text{F}$ , the ripple for a 60 Hz input is reduced from 10% of reading to approximately 0.3% of reading.

The settling time, however, is increased by approximately a factor of 3. Therefore, the values of  $C_{AV}$  and  $C_2$  can be reduced to permit faster settling times while still providing substantial ripple reduction.

The two-pole postfilter uses an active filter stage to provide even greater ripple reduction without substantially increasing the settling times over a circuit with a one-pole filter. The values of  $C_{AV}$ ,  $C_2$ , and  $C_3$  can then be reduced to allow extremely fast settling times for a constant amount of ripple. Caution should be exercised in choosing the value of  $C_{AV}$ , because the dc error is dependent on this value and is independent of the postfilter.

For a more detailed explanation of these topics, refer to the *RMS to DC Conversion Application Guide*, 2nd Edition, available online from Analog Devices, Inc., at [www.analog.com](http://www.analog.com).

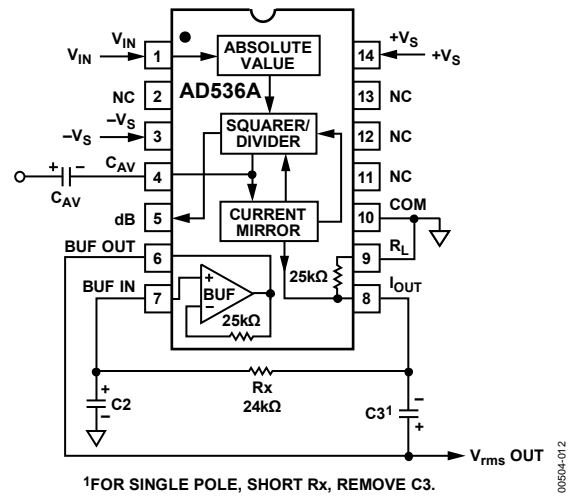


Figure 14. Two-Pole Postfilter

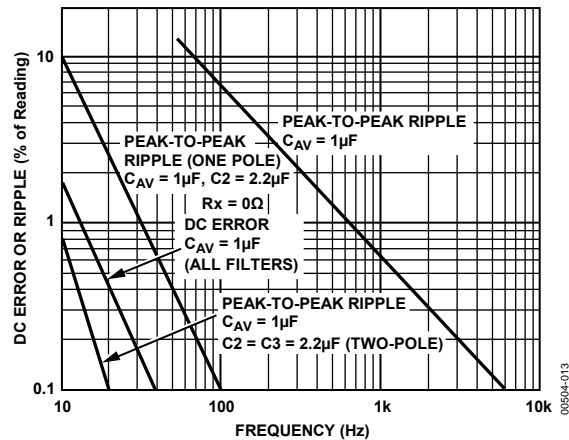


Figure 15. Performance Features of Various Filter Types (See Figure 6 to Figure 8 for Standard RMS Connection)



# AD536A

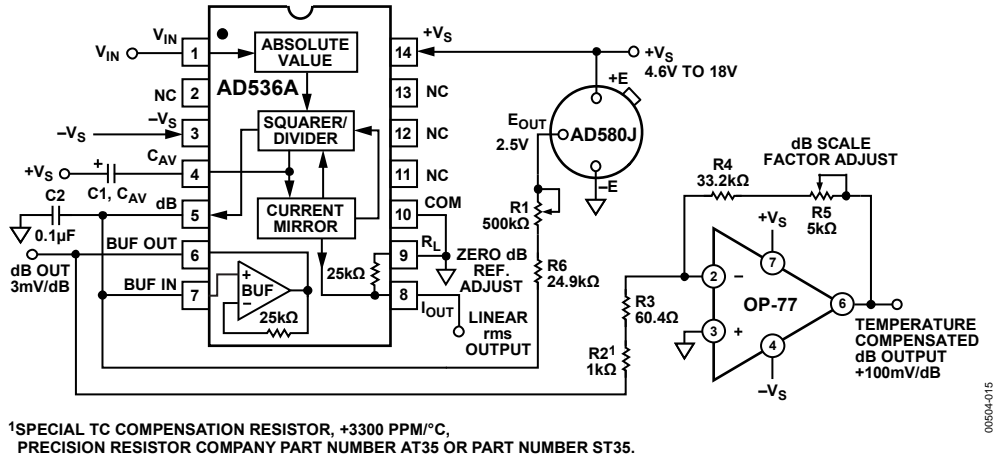


Figure 17. dB Connection

## FREQUENCY RESPONSE

The AD536A utilizes a logarithmic circuit in performing the implicit rms computation. As with any log circuit, bandwidth is proportional to signal level. The solid lines in the graph of Figure 18 represent the frequency response of the AD536A at input levels from 10 mV rms to 7 V rms. The dashed lines indicate the upper frequency limits for 1%, 10%, and  $\pm 3$  dB of reading additional error. For example, note that a 1 V rms signal produces less than 1% of reading additional error up to 120 kHz. A 10 mV rms signal can be measured with 1% of reading additional error (100  $\mu$ V) up to only 5 kHz.

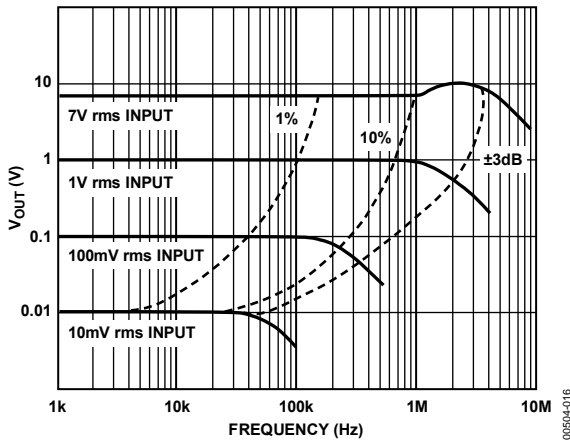


Figure 18. High Frequency Response

## AC MEASUREMENT ACCURACY AND CREST FACTOR

Crest factor is often overlooked when determining the accuracy of an ac measurement. The definition of crest factor is the ratio of the peak signal amplitude to the rms value of the signal ( $CF = V_P/V_{rms}$ ). Most common waveforms, such as sine and triangle waves, have relatively low crest factors ( $<2$ ). Waveforms that resemble low duty cycle pulse trains, such as those occurring in switching power supplies and SCR circuits, have high crest factors. For example, a rectangular pulse train with a 1% duty cycle has a crest factor of 10 ( $CF = 1/\eta$ ).

Figure 19 illustrates a curve of reading error for the AD536A for a 1 V rms input signal with crest factors from 1 to 11. A rectangular pulse train (pulse width = 100  $\mu$ s) was used for this test because it is the worst-case waveform for rms measurement (all of the energy is contained in the peaks). The duty cycle and peak amplitude were varied to produce crest factors from 1 to 11 while maintaining a constant 1 V rms input amplitude.

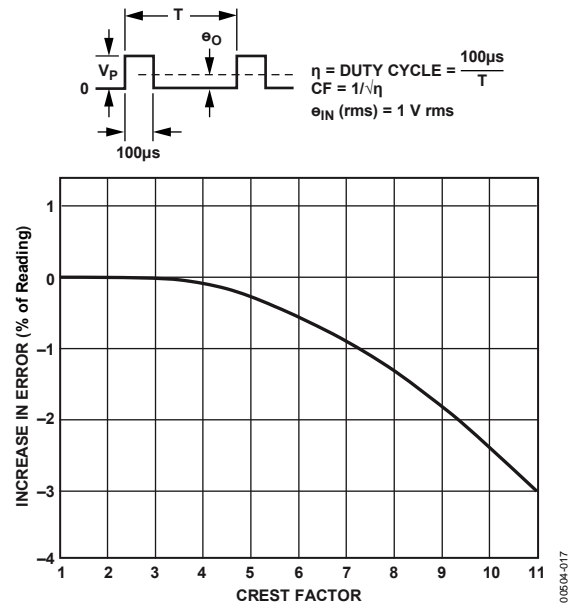


Figure 19. Error vs. Crest Factor

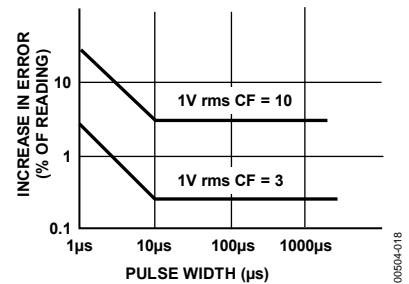


Figure 20. Error vs. Pulse Width Rectangular Pulse

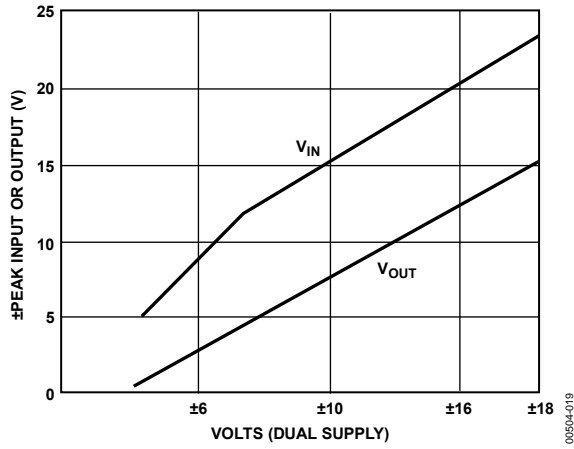


Figure 21. Input and Output Voltage Ranges vs. Dual Supply

00804-019

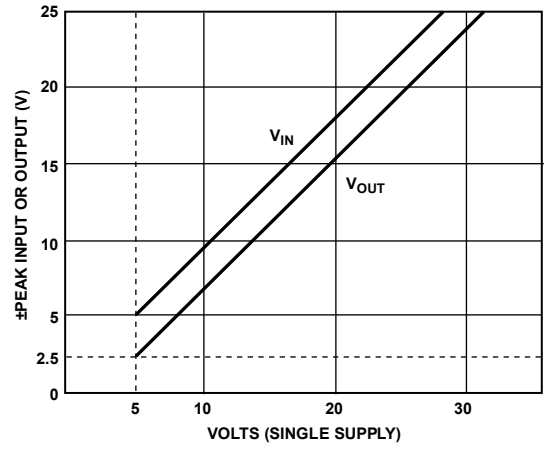
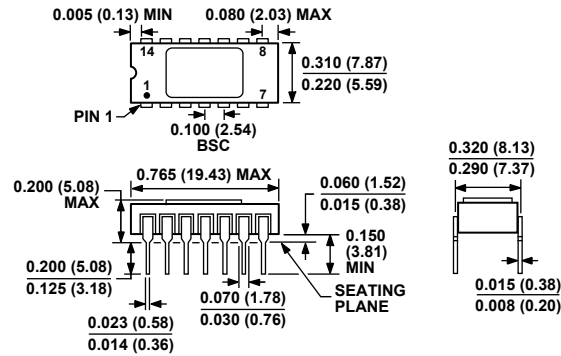


Figure 22. Input and Output Voltage Ranges vs. Single Supply

00804-022

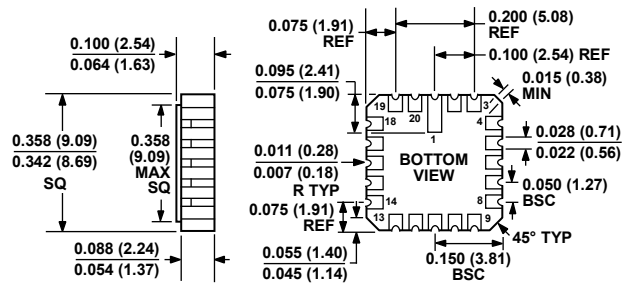
OUTLINE DIMENSIONS



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 23. 14-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP] (D-14)

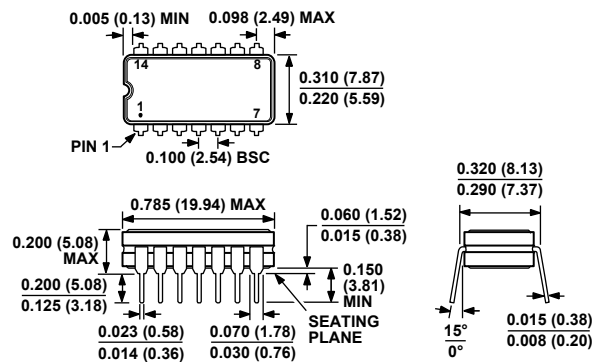
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 24. 20-Terminal Ceramic Leadless Chip Carrier [LCC] (E-20)

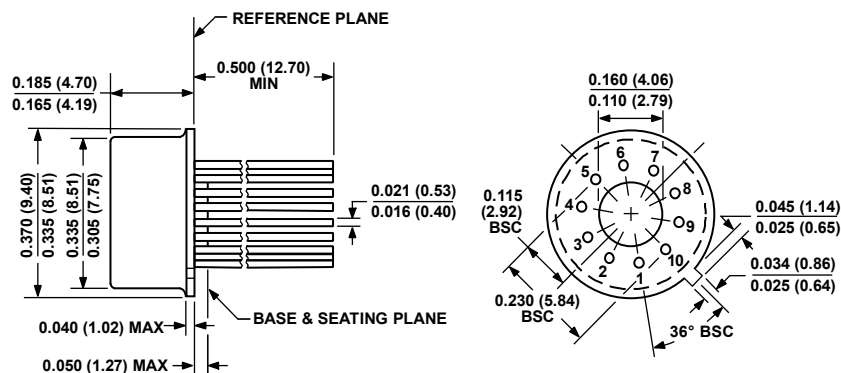
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 25. 14-Lead Ceramic Dual In-Line Package [CERDIP] (Q-14)

Dimensions shown in inches and (millimeters)



DIMENSIONS PER JEDEC STANDARDS MO-006-AF  
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

022306-A

Figure 26. 10-Pin Metal Header Package [TO-100]  
 (H-10)

Dimensions shown in inches and (millimeters)

**ORDERING GUIDE**

Model	Temperature Range	Package Description	Package Option
AD536AJD	0°C to +70°C	14-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-14
AD536AJDZ <sup>1</sup>	0°C to +70°C	14-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-14
AD536AKD	0°C to +70°C	14-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-14
AD536AKDZ <sup>1</sup>	0°C to +70°C	14-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-14
AD536AJH	0°C to +70°C	10-Pin Metal Header Package [TO-100]	H-10
AD536AJHZ <sup>1</sup>	0°C to +70°C	10-Pin Metal Header Package [TO-100]	H-10
AD536AKH	0°C to +70°C	10-Pin Metal Header Package [TO-100]	H-10
AD536AKHZ <sup>1</sup>	0°C to +70°C	10-Pin Metal Header Package [TO-100]	H-10
AD536AJQ	0°C to +70°C	14-Lead Ceramic Dual In-Line Package [CERDIP]	Q-14
AD536AKQ	0°C to +70°C	14-Lead Ceramic Dual In-Line Package [CERDIP]	Q-14
AD536ASD	-55°C to +125°C	14-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-14
AD536ASD/883B	-55°C to +125°C	14-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-14
AD536ASE/883B	-55°C to +125°C	20-Terminal Ceramic Leadless Chip Carrier [LCC]	E-20
AD536ASH	-55°C to +125°C	10-Pin Metal Header Package [TO-100]	H-10
AD536ASH/883B	-55°C to +125°C	10-Pin Metal Header Package [TO-100]	H-10
AD536ASCHIPS	-55°C to +125°C	Die	
5962-89805012A	-55°C to +125°C	20-Terminal Ceramic Leadless Chip Carrier [LCC]	E-20
5962-8980501CA	-55°C to +125°C	14-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]	D-14
5962-8980501IA	-55°C to +125°C	10-Pin Metal Header Package [TO-100]	H-10

<sup>1</sup> Z = RoHS Compliant Part.

**AD536A**

**NOTES**