1-/2-Channel +15V Digital Potentiometers

AD5260/AD5262

FEATURES
256 Position
AD5260 – 1-Channel
AD5262 – 2-Channel (Independently Programmable)
Potentiometer Replacement
20K, 50K, 200K Ohm
3-Wire SPI Compatible Serial Data Input
+5 to +15V Single-Supply; ±5.5V Dual-Supply Operation
Power ON Mid-Scale Preset

APPLICATIONS
Mechanical Potentiometer Replacement
Instrumentation: Gain, Offset Adjustment
Programmable Voltage to Current Conversion
Programmable Filters, Delays, Time Constants
Line Impedance Matching

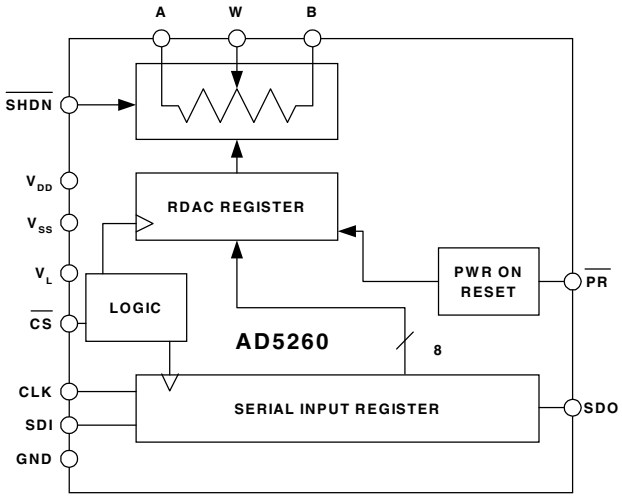
GENERAL DESCRIPTION

The AD5260/AD5262 provides a single or dual channel, 256 position, digitally-controlled variable resistor (VR) device. These devices perform the same electronic adjustment function as a potentiometer or variable resistor. Each Channel of the AD5260/AD5262 contains a fixed resistor with a wiper contact that taps the fixed resistor value at a point determined by a digital code loaded into the SPI compatible serial-input register. The resistance between the wiper and either end point of the fixed resistor varies linearly with respect to the digital code transferred into the VR latch. The variable resistor offers a completely programmable value of resistance, between the A terminal and the wiper or the B terminal and the wiper. The fixed A to B terminal resistance of 20K, 50K or 200KΩ has a nominal temperature coefficient of 30 ppm/°C.

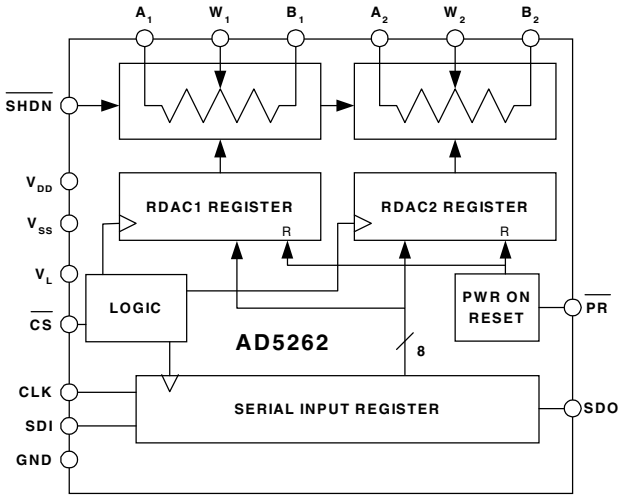
Each VR has its own VR latch, which holds its programmed resistance value. These VR latches are updated from an internal serial-to-parallel shift register, which is loaded from a standard 3-wire serial-input digital interface. The AD5260 contains an 8-bit serial register while the AD5262 contains a 9-bit serial register. Each bit is clocked into the register on the positive edge of the CLK. The AD5262 address bit determines the corresponding VR latch to be loaded with the last 8-bits of the data word during the positive edging of $\overline{CS}$ strobe. A serial data output pin at the opposite end of the serial register enables simple daisy-chaining in multiple VR applications without additional external decoding logic.

An optional reset ($\overline{PR}$) pin forces the wiper to the midscale position by loading 80_H into the VR latch.

The AD5260/AD5262 are available ultra compact thin surface mount TSSOP-14 and 16. All parts are guaranteed to operate over the extended industrial temperature range of -40°C to +85°C.



AD5260 FUNCTIONAL BLOCK DIAGRAM



AD5262 FUNCTIONAL BLOCK DIAGRAM

ORDERING GUIDE

Model	Kilo Ohms	Temp	Package Description	Package Option
AD5260BRU20	20	-40/+85°C	TSSOP-14	RU-14
AD5260BRU50	50	-40/+85°C	TSSOP-14	RU-14
AD5260BRU200	200	-40/+85°C	TSSOP-14	RU-14
AD5262BRU20	20	-40/+85°C	TSSOP-16	RU -16
AD5262BRU50	50	-40/+85°C	TSSOP-16	RU -16
AD5262BRU200	200	-40/+85°C	TSSOP-16	RU -16

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106 U.S.A.
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ELECTRICAL CHARACTERISTICS 20K, 50K, 200K OHM VERSION (V_{DD} = +5V, V_{SS} = -5V, V_L = +5V, V_A = +V_{DD}, V_B = 0V, -40°C < T_A < +85°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Units
DC CHARACTERISTICS RHEOSTAT MODE Specifications apply to all VRs						
Resistor Differential NL[2]	R-DNL	R_{WB}, V_A=NC	-1	±1/4	+1	LSB
Resistor Nonlinearity[2]	R-INL	R_{WB}, V_A=NC	-2	±1/2	+2	LSB
Nominal resistor tolerance[3]	ΔR	T_A = 25°C	-30		30	%
Resistance Temperature Coefficient	R_{AB}/ΔT	V_{AB} = V_{DD}, Wiper = No Connect		50		ppm/°C
Wiper Resistance	R_W	I_W = 1 V/R, V_{DD} = +5V		50	100	Ω
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE Specifications apply to all VRs						
Resolution	N		8			Bits
Differential Nonlinearity[4]	DNL		–1	±1/4	+1	LSB
Integral Nonlinearity[4]	INL		–2	±1/2	+2	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 40_H		5		ppm/°C
Full-Scale Error	V_{WFSE}	Code = FF_H	–2	-1	+0	LSB
Zero-Scale Error	V_{WZSE}	Code = 00_H	0	+1	+2	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A,B,W}$		V_{SS}		V_{DD}	V
Capacitance[6] Ax, Bx	$C_{A,B}$	f = 1 MHz, measured to GND, Code = 40_H		45		pF
Capacitance[6] Wx	C_W	f = 1 MHz, measured to GND, Code = 40_H		60		pF
Common-Mode Leakage	I_{CM}	V_A =V_B = V_{DD} / 2		1		nA
DIGITAL INPUTS & OUTPUTS						
Input Logic High	V_{IH}		2.4			V
Input Logic Low	V_{IL}				0.8	V
Input Logic High	V_{IH}	V_L = +3V, V_{SS} = 0V	2.1			V
Input Logic Low	V_{IL}	V_L = +3V, V_{SS} = 0V			0.6	V
Output Logic High	V_{OH}	R_L = 1KΩ to +5V	4.9			V
Output Logic Low	V_{OL}	I_{OL} = 1.6mA, V_{LOGIC} = +5V			0.4	V
Input Current	I_{IL}	V_{IN} = 0V or +5V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Logic Supply	V_L		2.7		5.5	V
Power Single-Supply Range	$V_{DD\ RANGE}$	V_{SS} = 0V	5		16.5	V
Power Dual-Supply Range	$V_{DD/SS\ RANGE}$		±4.5		±5.5	V
Logic Supply Current	I_L	V_L = +5V			60	µA
Positive Supply Current	I_{DD}	V_{IH} = +5V or V_{IL} = 0V			1	µA
Negative Supply Current	I_{SS}	V_{SS} = -5V			1	µA
Power Dissipation[9]	P_{DISS}	V_{IH} = +5V or V_{IL} = 0V, V_{DD} = +5V, V_{SS} = -5V			0.6	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = +5V ±10%		0.0002	0.005	%/%
DYNAMIC CHARACTERISTICS[6, 10]						
Bandwidth –3dB	BW_20K	R_{AB} = 20KΩ		400		KHz
Total Harmonic Distortion	THD_W	V_A =1Vrms, V_B = 0V, f=1KHz, R_{AB} = 20KΩ		0.008		%
V_W Settling Time	t_S	V_A= 10V, V_B=0V, ±1 LSB error band		2		µs
Resistor Noise Voltage	e_{N_WB}	R_{WB} = 10KΩ, f = 1KHz, RS = 0		9		nV√Hz

ELECTRICAL CHARACTERISTICS 20K, 50K, 200K OHM VERSION (V_{DD} = +5V, V_{SS} = -5V, V_L = +5V, V_A = +V_{DD}, V_B = 0V, -40°C < T_A < +85°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Units
INTERFACE TIMING CHARACTERISTICS applies to all parts (Notes 6,12)						
Input Clock Pulse Width	t_{CH},t_{CL}	Clock level high or low	50			ns
Data Setup Time	t_{DS}		20			ns
Data Hold Time	t_{DH}		20			ns
CLK to SDO Propagation Delay[13]	t_{PD}	R_L = 1KΩ, C_L < 20pF	1		150	ns
$\overline{CS}$ Setup Time	t_{CSS}		20			ns
$\overline{CS}$ High Pulse Width	t_{CSW}		40			ns
Reset Pulse Width	t_{RS}		90			ns
CLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
$\overline{CS}$ Rise to Clock Rise Setup	t_{CS1}		10			ns

NOTES:

1. Typicals represent average readings at +25°C and V_{DD} = +5V, V_{SS} = -5V.
2. Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic. I_W = V_{DD}/R for both V_{DD}=+5V, V_{SS}=-5V.
3. V_{AB} = V_{DD}, Wiper (V_W) = No connect
4. INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. VA = V_{DD} and V_B = 0V. DNL specification limits of ±1LSB maximum are Guaranteed Monotonic operating conditions.
5. Resistor terminals A, B, W have no limitations on polarity with respect to each other.
6. Guaranteed by design and not subject to production test.
7. Measured at the Ax terminals. All Ax terminals are open circuited in shutdown mode.
8. Worst case supply current consumed when input all logic-input levels set at 2.4V, standard characteristic of CMOS logic.
9. P_{DISS} is calculated from (I_{DD} x V_{DD}). CMOS logic level inputs result in minimum power dissipation.
10. All dynamic characteristics use V_{DD} = +5V, V_{SS} = -5V, V_L = +5V
11. Measured at a V_W pin where an adjacent V_W pin is making a full-scale voltage change.
12. See timing diagram for location of measured values. All input control voltages are specified with t_R=t_F=2ns(10% to 90% of +3V) and timed from a voltage level of 1.5V. Switching characteristics are measured using V_L = +5V.
13. Propagation delay depends on value of V_{DD}, R_L, and C_L see applications text.
14. The AD5260/AD5262 contains 1,968 transistors. Die Size: 89mil x 105mil, 9,345sq. mil.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted)

V_{DD} to GND ..... -0.3, +15V
V_{SS} to GND .....0V, -7V
V_{DD} to V_{SS} .....+15V
V_A, V_B, V_W to GND.....V_{SS}, V_{DD}
$A_X – B_X$, $A_X – W_X$, $B_X – W_X$ .....±20mA
Digital Inputs & Output Voltage to GND.....0V, +7V
Operating Temperature Range.....-40°C to +85°C
Maximum Junction Temperature ($T_{J\ MAX}$).....+150°C
Storage Temperature.....-65°C to +150°C
Lead Temperature (Soldering, 10 sec).....+300°C
Thermal Resistance* θ_{JA},
TSSOP-14.....206°C/W
TSSOP-16.....180°C/W
*Package Power Dissipation = (T_JMAX - T_A) / θ_{JA}

TABLE 1A: AD5260 Serial-Data Word Format

				DATA			
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
D7	D6	D5	D4	D3	D2	D1	D0
MSB							LSB
2^7							2^0

TABLE 1B: AD5262 Serial-Data Word Format

ADDR				DATA				
B8	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
A0	D7	D6	D5	D4	D3	D2	D1	D0
	MSB							LSB
2^8	2^7							2^0

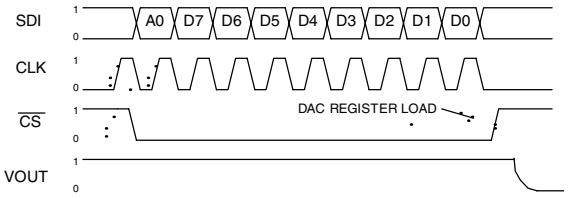


Figure 1A. Timing Diagram

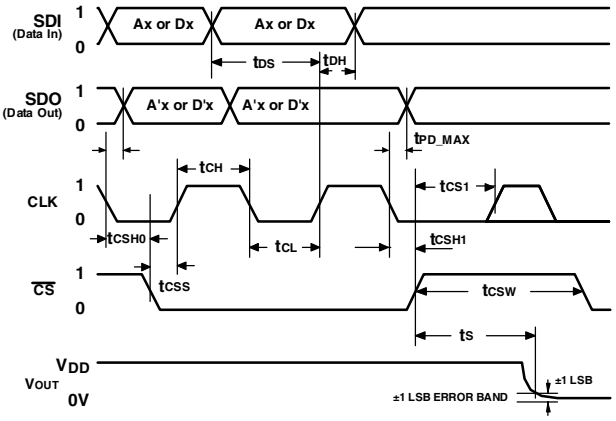


Figure 1B. Detail Timing Diagram

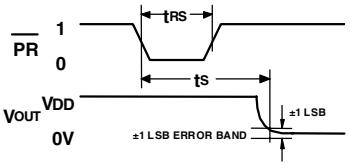
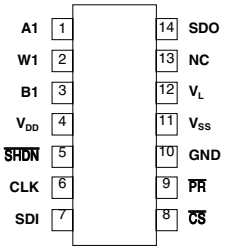


Figure 1C. AD5260 Preset Timing Diagram

AD5260 PIN CONFIGURATION



AD5262 PIN CONFIGURATION

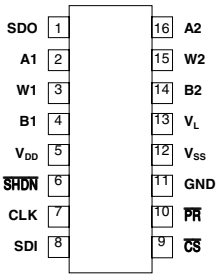


TABLE 2: AD5260 PIN Descriptions

Pin	Name	Description
1	A	A Terminal
2	W	Wiper, addr=0_2
3	B	B Terminal
4	V_{DD}	Positive power supply, specified for operation at both +5V or 15V. (Sum of $\|V_{DD}\| + \|V_{SS}\| \leq 15V$)
5	$\overline{SHDN}$	Active low input. Terminal A open-circuit. Shutdown controls Variable Resistors of RDAC
6	CLK	Serial Clock Input, positive edge triggered
7	SDI	Serial Data Input
8	$\overline{CS}$	Chip Select Input, Active Low. When $\overline{CS}$ returns high, data will be loaded into the DAC register.
9	$\overline{PR}$	Active low preset to mid-scale; sets RDAC registers to 80_H
10	GND	Ground
11.	V_{SS}	Negative Power Supply, specified for operation from 0V to -5V
12	V_L	Logic Supply Voltage, needs to be same voltage as the digital logic controlling the AD5260.
13	NC	No Connect
14	SDO	Serial Data Output, Open Drain transistor requires pull-up resistor.

TABLE 3: AD5262 PIN Descriptions

Pin	Name	Description
1	SDO	Serial Data Output, Open Drain transistor requires pull-up resistor.
2	A1	A Terminal RDAC #1
3	W1	Wiper RDAC #1, address A0=0_2
4	B1	B Terminal RDAC #1
5	V_{DD}	Positive power supply, specified for operation at both +5V or +15V. (Sum of $\|V_{DD}\| + \|V_{SS}\| \leq 15V$)
6	$\overline{SHDN}$	Active low input. Terminal A open-circuit. Shutdown controls Variable Resistors #1 through #2
7	CLK	Serial Clock Input, positive edge triggered
8	SDI	Serial Data Input
9	$\overline{CS}$	Chip Select Input, Active Low. When $\overline{CS}$ returns high, data in the serial input register is decoded based on the address bits and loaded into the target DAC register.
10	$\overline{PR}$	Active low preset to mid-scale; sets RDAC registers to 80_H
11	GND	Ground
12	V_{SS}	Negative Power Supply, specified for operation at both 0V or -5V (Sum of $\|V_{DD}\| + \|V_{SS}\| < 15V$)
13	V_L	Logic Supply Voltage, needs to be same voltage as the digital logic controlling the AD5262.
14	B2	B Terminal RDAC #2
15	W2	Wiper RDAC #2, address A0=1_2
16	A2	A Terminal RDAC #2

OPERATION

The AD5260/AD5262 provide a single/dual channel, 256-position digitally-controlled variable resistor (VR) device. Changing the programmed VR settings is accomplished by clocking in a 9-bit serial data word into the SDI (Serial Data Input) pin. The format of this data word is one address bit A0 represents the first bit B8, then followed by eight data bits B7-B0 with MSB first. Table 1 provides the serial register data word format. See Table 5 for the AD5260/AD5262 address assignments to decode the location of VR latch receiving the serial register data in bits B7 through B0. VR outputs can be changed one at a time in random sequence. The AD5260/AD5262 presets to a mid-scale by asserting the $\overline{PR}$ pin, simplifying fault condition recovery at power up. Both parts have an internal power ON preset that places the wiper in a midscale preset condition at power ON. Operation of the power on preset function depends only on the logic pin (V_L).

The AD5260/AD5262 contains a power shutdown $\overline{SHDN}$ pin, which places the RDAC in a zero power consumption state where terminals Ax are open circuited, and the wiper W is connected to B resulting in only leakage currents being consumed in the VR structure. In shutdown mode the VR latch settings are maintained, so that, returning to operational mode from power shutdown, the VR settings return to their previous resistance values.

DIGITAL INTERFACING

The AD5260/AD5262 contain a standard three-wire serial input control interface. The three inputs are clock (CLK), $\overline{CS}$ and serial data input (SDI). The positive-edge sensitive CLK input requires clean transitions to avoid clocking incorrect data into the serial input register. Standard logic families work well. If mechanical switches are used for product evaluation they should be debounced by a flip-flop or other suitable means. Figure 3 block diagram shows more detail of the internal digital circuitry. When $\overline{CS}$ is low, the clock loads data into the serial register on each positive clock edge, see Table 4.

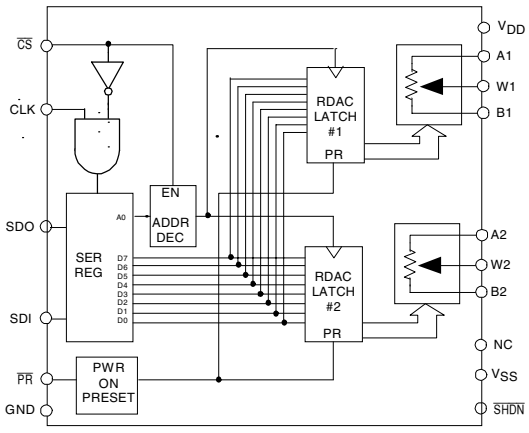


Figure 3. Block Diagram

TABLE 4: Input Logic Control Truth Table

CLK	$\overline{CS}$	$\overline{PR}$	$\overline{SHDN}$	Register Activity
L	L	H	H	No SR effect, enables SDO pin
P	L	H	H	Shift One bit in from the SDI pin. The eighth previously entered bit is shifted out of the SDO pin.
X	P	H	H	Load SR data into RDAC latch based on A0 decode (Table 5).
X	H	H	H	No Operation
X	X	L	H	Sets all RDAC latches to midscale, wiper centered, & SDO latch cleared.
X	H	P	H	Latches all RDAC latches to 80_H.
X	H	H	L	Open circuits all resistor A–terminals, connects W to B, turns off SDO output transistor.

NOTE: P = positive edge, X = don't care, SR = shift register

The serial-data-output (SDO) pin contains an open drain n-channel FET. This output requires a pull-up resistor in order to transfer data to the next package's SDI pin. The pull-up resistor termination voltage may be larger than the V_{DD} supply of the AD5260/AD5262 SDO output device, e.g., the AD5260/AD5262 could operate at V_{DD} = 3.3V and the pull-up for interface to the next device could be set at +5V. This allows for daisy chaining several RDACs from a single processor serial-data line. Clock period needs to be increased when using a pull-up resistor to the SDI pin of the following device in series. Capacitive loading at the daisy chain node SDO-SDI between devices may induce time delay to subsequent devices. User should be aware of this potential problem in order to achieve data transfer successfully. When daisy chaining is used, the $\overline{CS}$ should be kept low until all the bits of every package are clocked into their respective serial registers insuring that the address bit and data bits are in the proper decoding location, see Figure 4. This would require 18 bits of address and data complying to the word format provided in Table 1 if two AD5262 RDACs are daisy chained. During shutdown ($\overline{SHDN}$) the SDO output pin is forced to the off (logic high state) to disable power dissipation in the pull up resistor. See figure 6 for equivalent SDO output circuit schematic.

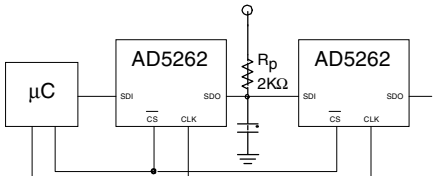


Figure 4. Daisy Chain Configuration

TABLE 5. Address Decode Table

A0	Latch Loaded	
0	RDAC#1	AD5262
1	RDAC#2	AD5262
X	RDAC#1	AD5260

The data setup and data hold times in the specification table determine the data valid time requirements. The AD5260 uses an 8-bit serial input data register word that is transferred to the internal RDAC register when the CS line returns to logic high. For AD5262 the last 9 bits of the data word entered into the serial register are held when $\overline{CS}$ returns high. Any extra bits are ignored. At the same time $\overline{CS}$ goes high it gates the address decoder enabling AD5262 one of two positive edge triggered AD5262 RDAC latches, see figure 5 detail.

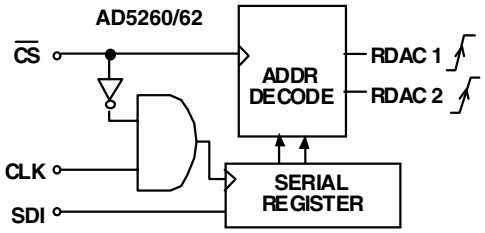


Figure 5. Equivalent Input Control Logic

The target RDAC latch is loaded with the last eight bits of the serial data word completing one DAC update. For AD5262, two separate 9 bit data words must be clocked in to change both VR settings.

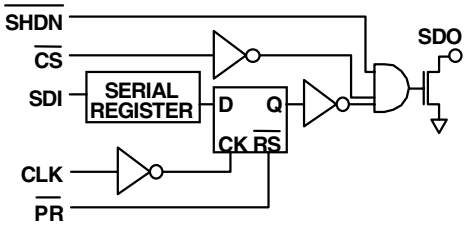


Figure 6. Detail SDO output schematic of the AD5260

All digital inputs are protected with a series input resistor and parallel Zener ESD structure shown in figure 8. Applies to digital input pins $\overline{CS}$, SDI, SDO, $\overline{PR}$, $\overline{SHDN}$, CLK

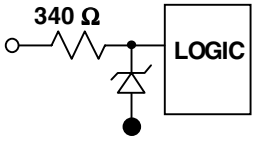


Figure 7. ESD Protection of digital pins

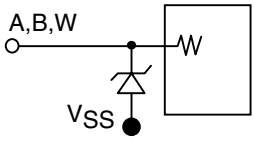


Figure 8. ESD Protection of Resistor Terminals

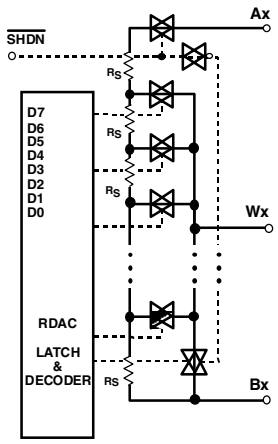


Figure 9. AD5260/AD5262 Equivalent RDAC Circuit

PROGRAMMING THE VARIABLE RESISTOR
Rheostat Operation

The nominal resistances of the RDAC between terminals A and B are available with values of 20KΩ, 50KΩ, and 200KΩ. The final three digits of the part number determine the nominal resistance value, e.g. 20KΩ = 20; 50KΩ = 50; 200KΩ = 200. The nominal resistance (R_{AB}) of the VR has 256 contact points accessed by the wiper terminal, plus the B terminal contact. The eight bit data in the RDAC latch is decoded to select one of the 256 possible settings. Assume a 20KΩ part is used, the wiper's first connection starts at the B terminal for data 00_H. Since there is a 60Ω wiper contact resistance, such connection yields a minimum of 60Ω resistance between terminals W and B. The second connection is the first tap point corresponds to 138Ω ($R_{WB} = R_{AB}/256 + R_W = 78Ω+60Ω$) for data 01_H. The third connection is the next tap point representing 216Ω (78x2+60) for data 02_H and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 19982Ω [R_{AB}–1LSB+R_W]. The wiper does not directly connect to the B terminal. See Figure 9 for a simplified diagram of the equivalent RDAC circuit.

The general equation determining the digitally programmed output resistance between W and B is:

$$R_{WB}(D) = \frac{D}{256} \cdot R_{AB} + R_W \qquad \text{eqn.1}$$

where D is the decimal equivalent of the binary code which is loaded in the 8-bit RDAC register, and R_{AB} is the nominal end-to-end resistance.

For example, R_{AB}=20KΩ, when V_B = 0V and A–terminal is open circuit, the following output resistance values R_{WB} will be set for the following RDAC latch codes. Result will be the same if terminal A is tied to W:

D (DEC)	R_{WB} (Ohms)	Output State
256	199826Ω	Full-Scale (R_{AB} - 1LSB + R_W)
128	10060Ω	Mid-Scale
1	138Ω	1 LSB
0	60Ω	Zero-Scale (Wiper contact resistance)

In the zero-scale condition a finite wiper resistance of 60Ω is present. Care should be taken to limit the current flow between W and B in this state to a maximum current of no more than 5mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the wiper W and terminal A also produces a digitally controlled resistance R_{WA}. When these terminals are used the B–terminal should be let open or tied to the wiper terminal. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch is increased in value. The general equation for this operation is:

$$R_{WA}(D) = \frac{256 - D}{256} \cdot R_{AB} + R_W \qquad \text{eqn. 2}$$

For example, R_{AB}=20KΩ, when V_A = 0V and B–terminal is open, the following output resistance R_{WA} will be set for the following RDAC latch codes. Result will be the same if terminal B is tied to W:

D (DEC)	R_{WA} (Ω)	Output State
256	60	Full-Scale
128	10060	Mid-Scale
1	19982	1 LSB
0	20060	Zero-Scale

The typical distribution of the nominal resistance R_{AB} from channel-to-channel matches within ±1%. Device to device matching is process lot dependent and is possible to have ±30% variation. Since the resistance element is processed in thin film technology, the change in R_{AB} with temperature has a 30 ppm/°C temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER
Voltage Output Operation

The digital potentiometer easily generates output voltages at wiper-to-B and wiper-to-A to be proportional to the input voltage at A-to-B. Let's ignore the effect of the wiper resistance at the moment. For example connecting A–terminal to +5V and B–terminal to ground produces an output voltage at the wiper-to-B starting at zero volts up to 1 LSB less than +5V. Each LSB of voltage is equal to the voltage applied across terminal AB divided by the 256 position of the potentiometer divider. Since the AD5260/AD5262 operates from dual supplies, the general equation defining the output voltage at V_W with respect to ground for any given input voltage applied to terminals AB is:

$$V_W(D) = \frac{D}{256} V_A + \frac{256 - D}{256} V_B \qquad \text{eqn. 3}$$

where D is decimal equivalent of the binary code, which is loaded in the 8-bit RDAC register.

Operation of the digital potentiometer in the divider mode results in more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent on the ratio of the internal resistors R_{WA} and R_{WB} and not the absolute values, therefore, the drift reduces to 5ppm/°C.

TEST CIRCUITS

Figures 10 to 18 define the test conditions used in product specification table.

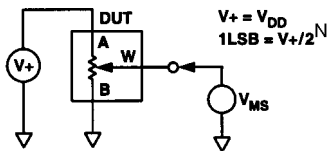


Figure 10. Potentiometer Divider Nonlinearity error test circuit (INL, DNL)

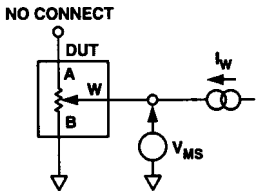


Figure 11. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

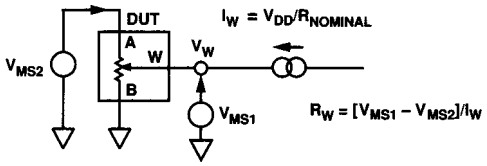


Figure 12. Wiper Resistance test Circuit

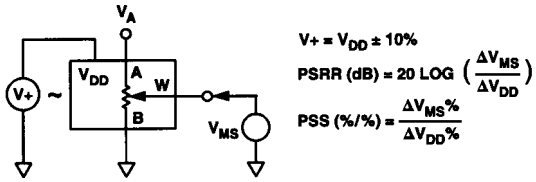


Figure 13. Power supply sensitivity test circuit (PSS, PSSR)

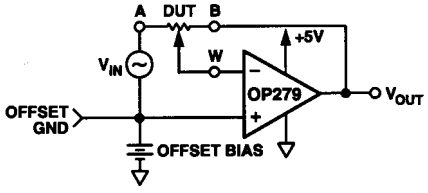


Figure 14. Inverting Gain test Circuit

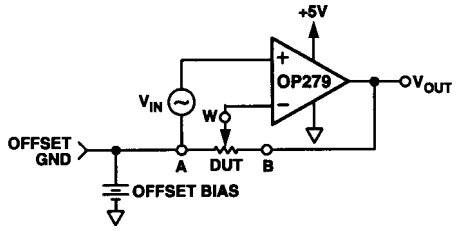


Figure 15. Non-Inverting Gain test circuit

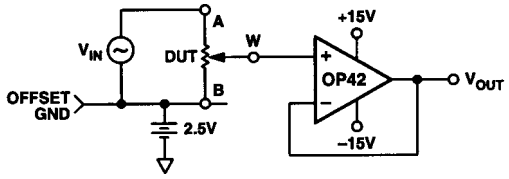


Figure 16. Gain Vs Frequency test circuit

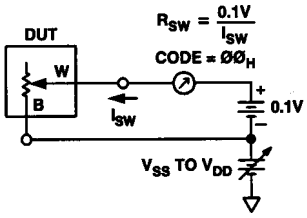


Figure 17. Incremental ON Resistance Test Circuit

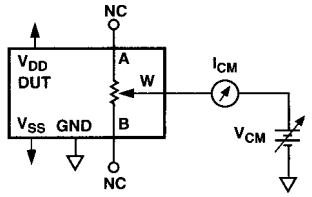
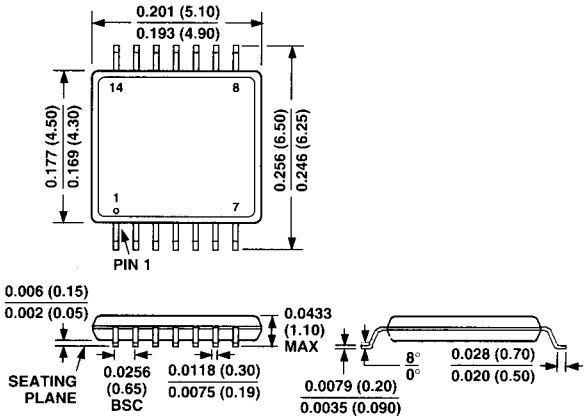


Figure 18. Common Mode Leakage current test circuit

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)

14-Lead TSSOP
(RU-14)



16-Lead TSSOP
(RU-16)