3 Mbit / 4 Mbit / 8 Mbit LPC Flash

SST49LF030A / SST49LF040A / SST49LF080A

Advance Information

FEATURES:

- **LPC Interface Flash**
  - SST49LF030A: 384K x8 (3 Mbit)
    SST49LF040A: 512K x8 (4 Mbit)
    SST49LF080A: 1024K x8 (8 Mbit)
- **Conforms to Intel LPC Interface Specification 1.0**
- **Flexible Erase Capability**
  - Uniform 4 KByte sectors
  - Uniform 64 KByte overlay blocks
  - 64 KByte Top boot block protection
  - Chip-Erase for PP Mode Only
- **Single 3.0-3.6V Read and Write Operations**
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption**
  - Active Read Current: 6 mA (typical)
  - Standby Current: 10 µA (typical)
- **Fast Sector-Erase/Byte-Program Operation**
  - Sector-Erase Time: 18 ms (typical)
  - Block-Erase Time: 18 ms (typical)
  - Chip-Erase Time: 70 ms (typical)
  - Byte-Program Time: 14 µs (typical)
  - Chip Rewrite Time:
    SST49LF030A: 6 seconds (typical)
    SST49LF040A: 8 seconds (typical)
    SST49LF080A: 16 seconds (typical)
  - Single-pulse Program or Erase
  - Internal timing generation
- **Two Operational Modes**
  - Low Pin Count (LPC) Interface mode for in-system operation
  - Parallel Programming (PP) Mode for fast production programming
- **LPC Interface Mode**
  - 5-signal communication interface supporting byte Read and Write
  - 33 MHz clock frequency operation
  - WP# and TBL# pins provide hardware write protect for entire chip and/or top boot block
  - Standard SDP Command Set
  - Data# Polling and Toggle Bit for End-of-Write detection
  - 5 GPI pins for system design flexibility
  - 4 ID pins for multi-chip selection
- **Parallel Programming (PP) Mode**
  - 11-pin multiplexed address and 8-pin data I/O interface
  - Supports fast programming In-System on programmer equipment
- **CMOS and PCI I/O Compatibility**
- **Packages Available**
  - 32-lead PLCC
  - 32-lead TSOP (8mm x 14mm)

PRODUCT DESCRIPTION

The SST49LF0x0A flash memory devices are designed to interface with the LPC bus for PC and Internet Appliance application in compliance with Intel Low Pin Count (LPC) Interface Specification 1.0. Two interface modes are supported by the SST49LF0x0A: LPC mode for In-System operations and Parallel Programming (PP) mode to interface with programming equipment.

The SST49LF0x0A flash memory devices are manufactured with SST's proprietary, high performance SuperFlash Technology. The split-gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST49LF0x0A devices significantly improve performance and reliability, while lowering power consumption. The SST49LF0x0A devices write (Program or Erase) with a single 3.0-3.6V power supply. It uses less energy during Erase and Program than alternative flash memory technologies. The total energy consumed is a function of the applied voltage, current and time of application. Since for any give voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash memory technologies. The SST49LF0x0A products provide a maximum Byte-Program time of 20 µsec. The entire memory can be erased and programmed byte-by-byte typically in 6 seconds for SST49LF030A, 8 seconds for the SST49LF040A and 16 seconds for the SST49LF080A, when using status detection features such as Toggle Bit or Data# Polling to indicate the completion of Program operation. The SuperFlash technology provides fixed Erase and Program time, independent of the number of Erase/Program cycles that have performed. Therefore the system software or hardware does not have to be calibrated or correlated to the cumulative number of Erase cycles as is necessary with alternative flash memory technologies, whose Erase and Program time increase with accumulated Erase/Program cycles.

To meet high density, surface mount requirements, the SST49LF0x0A devices are offered in 32-lead TSOP and 32-lead PLCC packages. See Figures 1 and 2 for pin assignments and Table 1 for pin descriptions.

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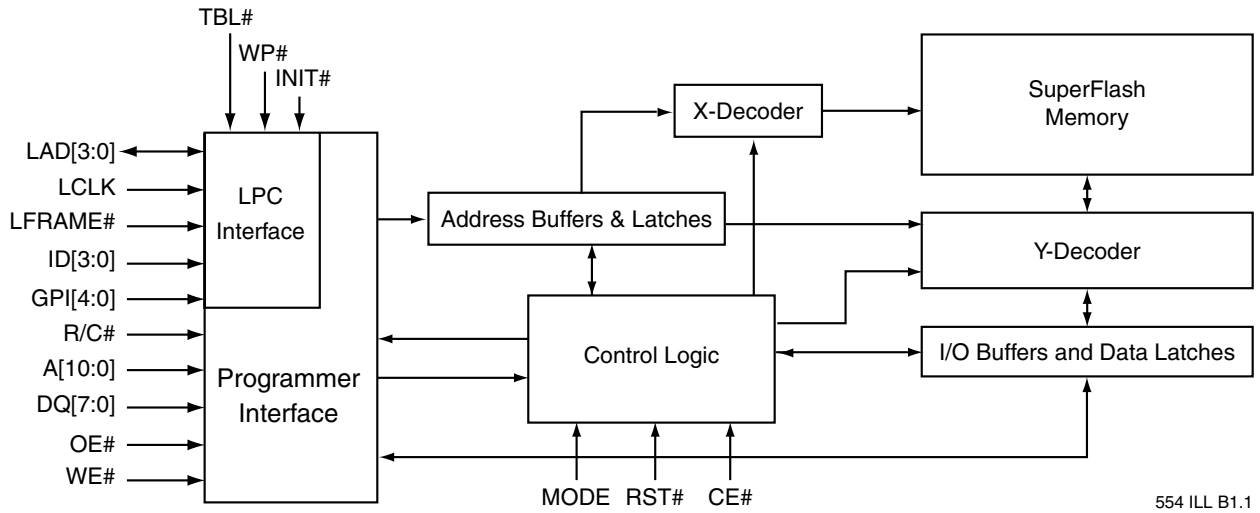
FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENTS

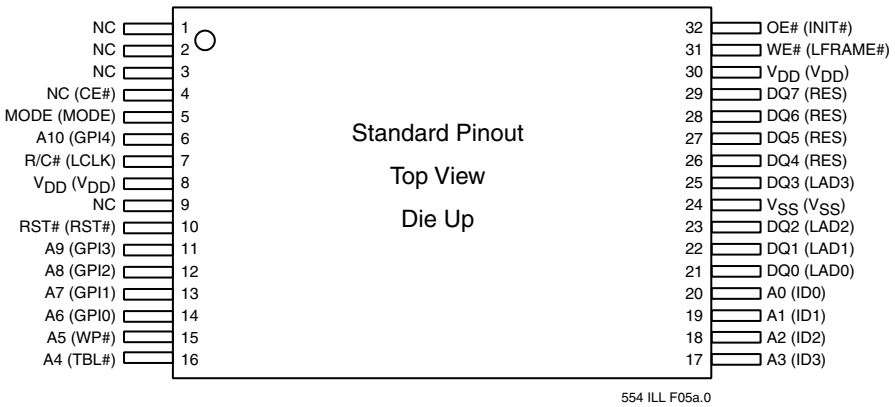


FIGURE 1: PIN ASSIGNMENTS FOR 32-LEAD TSOP (8MM X 14MM)

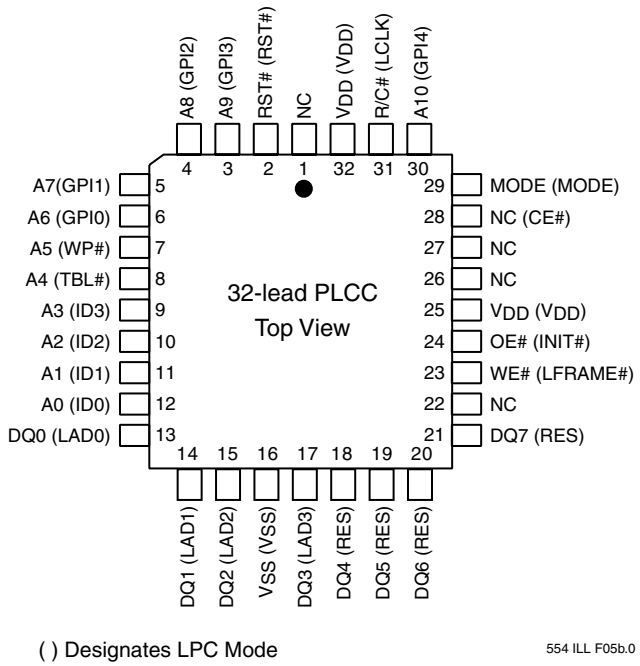


FIGURE 2: PIN ASSIGNMENTS FOR 32-LEAD PLCC

Advance Information

TABLE 1: PIN DESCRIPTION

Symbol	Pin Name	Type[1]	Interface		Functions
			PP	LPC	
A_{10}-A_0	Address	I	X		Inputs for low-order addresses during Read and Write operations. Addresses are internally latched during a Write cycle. For the programming interface, these addresses are latched by R/C# and share the same pins as the high-order address inputs.
DQ_7-DQ_0	Data	I/O	X		To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# is high.
OE#	Output Enable	I	X		To gate the data output buffers.
WE#	Write Enable	I	X		To control the Write operations.
MODE	Interface Mode Select	I	X	X	This pin determines which interface is operational. When held high, programmer mode is enabled and when held low, LPC mode is enabled. This pin must be setup at power-up or before return from reset and not change during device operation. This pin must be held high (V_{IH}) for PP mode and low (V_{IL}) for LPC mode.
INIT#	Initialize	I		X	This is the second reset pin for in-system use. This pin is internally combined with the RST# pin; If this pin or RST# pin is driven low, identical operation is exhibited.
ID[3:0]	Identification Inputs	I		X	These four pins are part of the mechanism that allows multiple parts to be attached to the same bus. The strapping of these pins is used to identify the component.The boot device must have ID[3:0]=0000 for all subsequent devices should use sequential up-count strapping. These pins are internally pulled-down with a resistor between 20-100 KΩ
GPI[4:0]	General Purpose Inputs	I		X	These individual inputs can be used for additional board flexibility. The state of these pins can be read through LPC registers. These inputs should be at their desired state before the start of the PCI clock cycle during which the read is attempted, and should remain in place until the end of the Read cycle. Unused GPI pins must not be floated.
TBL#	Top Block Lock	I		X	When low, prevents programming to the boot block sectors at top of memory. When TBL# is high it disables hardware write protection for the top block sectors. This pin cannot be left unconnected.
LAD[3:0]	Address and Data	I/O		X	To provide LPC control signals, as well as addresses and Command Inputs/Outputs data.
LCLK	Clock	I		X	To provide a clock input to the control unit
LFRAME#	Frame	I		X	To indicate start of a data transfer operation; also used to abort an LPC cycle in progress.
RST#	Reset	I	X	X	To reset the operation of the device
WP#	Write Protect	I		X	When low, prevents programming to all but the highest addressable blocks. When WP# is high it disables hardware write protection for these blocks. This pin cannot be left unconnected.
R/C#	Row/Column Select	I	X		Select for the Programming interface, this pin determines whether the address pins are pointing to the row addresses, or to the column addresses.
RES	Reserved			X	These pins must be left unconnected.
V_{DD}	Power Supply	PWR	X	X	To provide power supply (3.0-3.6V)
V_{SS}	Ground	PWR	X	X	Circuit ground (0V reference)
CE#	Chip Enable	I		X	This signal must be asserted to select the device. When CE# is low, the device is enabled. When CE# is high, the device is placed in low power standby mode.
NC	No Connection	I	X	X	Unconnected pins.

T1.6 554

1. I=Input, O=Output

DEVICE MEMORY MAPS

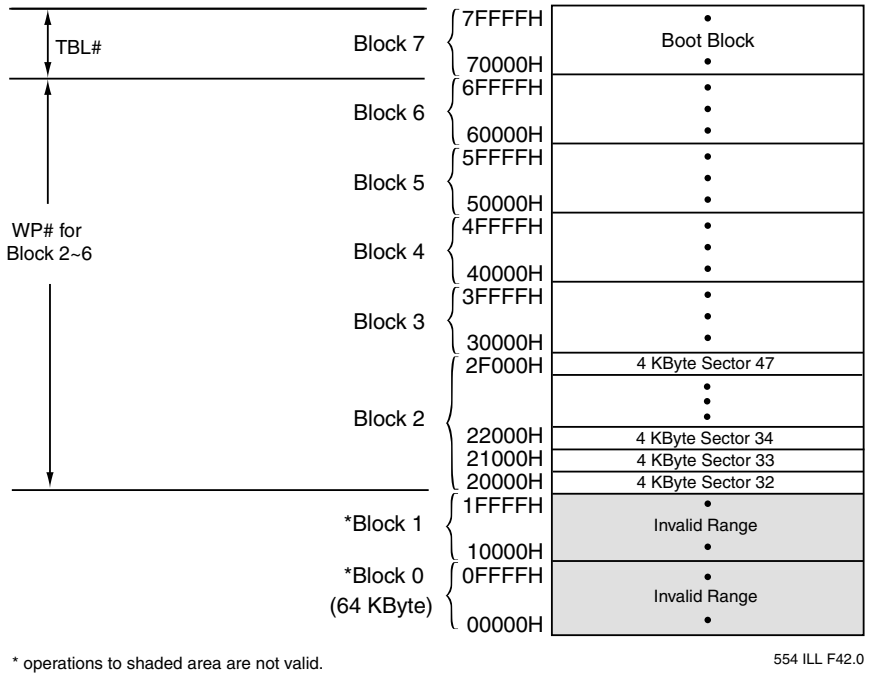


FIGURE 3: DEVICE MEMORY MAP FOR SST49LF030A

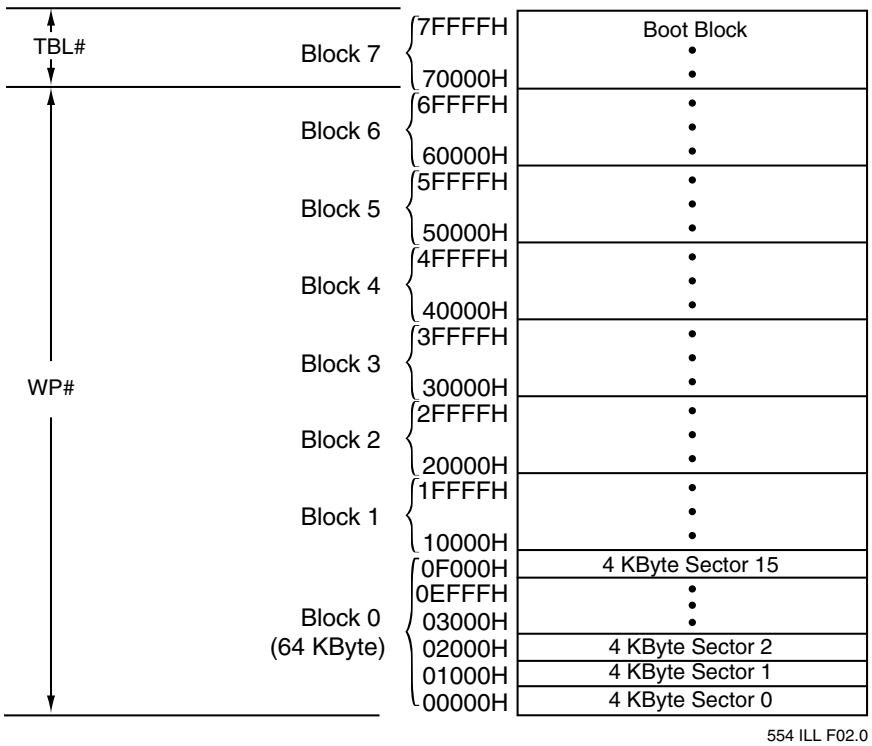


FIGURE 4: DEVICE MEMORY MAP FOR SST49LF040A

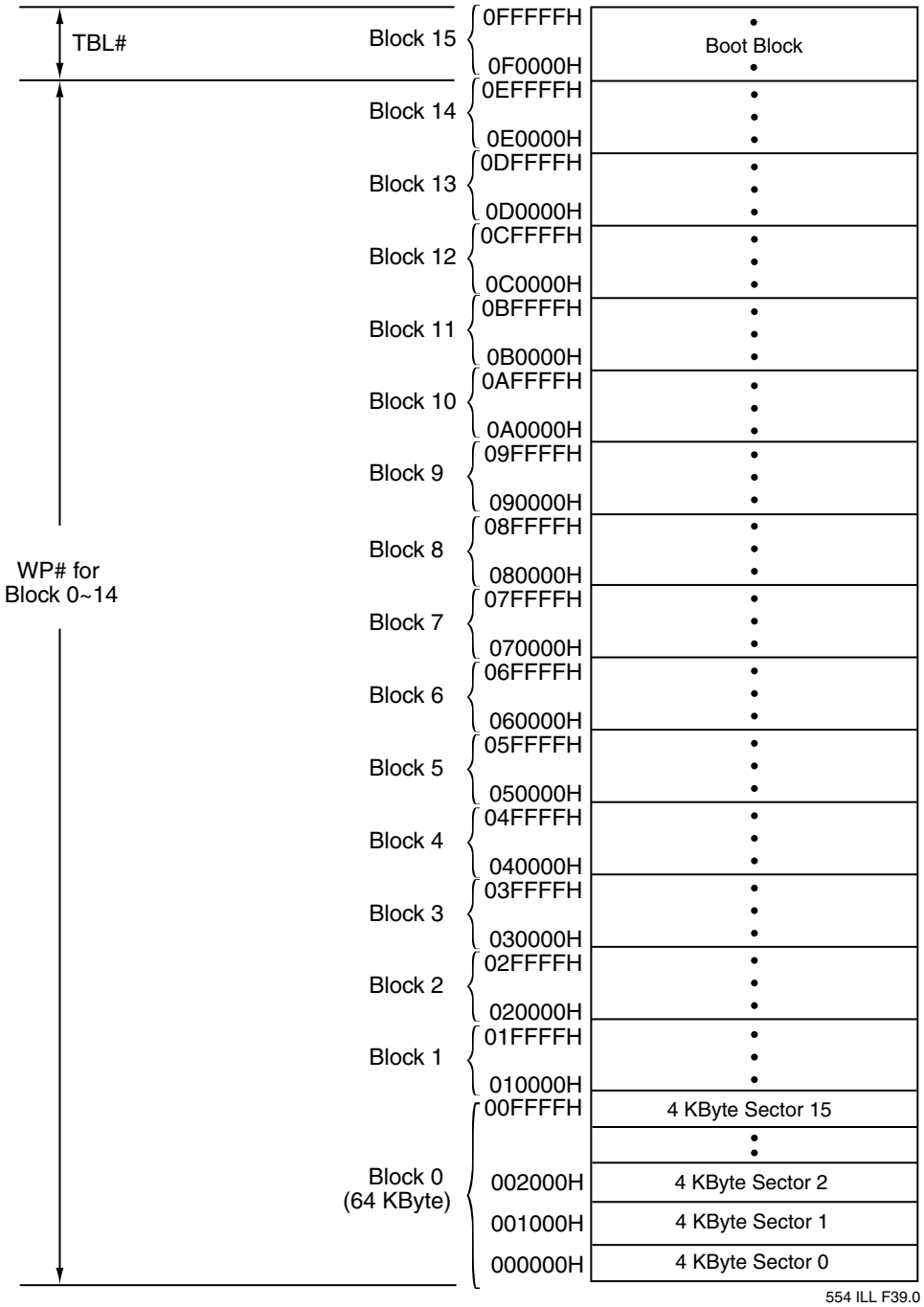


FIGURE 5: DEVICE MEMORY MAP FOR SST49LF080A

DESIGN CONSIDERATIONS

SST recommends a high frequency 0.1 µF ceramic capacitor to be placed as close as possible between V_{DD} and V_{SS} less than 1 cm away from the V_{DD} pin of the device. Additionally, a low frequency 4.7 µF electrolytic capacitor from V_{DD} to V_{SS} should be placed within 5 cm of the V_{DD} pin. If you use a socket for programming purposes add an additional 1-10 µF next to each socket.

PRODUCT IDENTIFICATION

The Product Identification mode identifies the device as the SST49LF0x0A and manufacturer as SST.

TABLE 2: PRODUCT IDENTIFICATION

	Address	Data
Manufacturer's ID	0000H	BFH
Device ID		
SST49LF030A	0001H	1CH
SST49LF040A	0001H	53H
SST49LF080A	0001H	5BH

T2.4 554

MODE SELECTION

The SST49LF0x0A flash memory devices can operate in two distinct interface modes: the LPC mode and the Parallel Programming (PP) mode. The mode pin is used to set the interface mode selection. If the mode pin is set to logic High, the device is in PP mode. If the mode pin is set Low, the device is in the LPC mode. The mode selection pin must be configured prior to device operation. The mode pin is internally pulled down if the pin is left unconnected. In LPC mode, the device is configured to its host using standard LPC interface protocol. Communication between Host and the SST49LF0x0A occurs via the 4-bit I/O communication signals, LAD [3:0] and LFRAME#. In PP mode, the device is programmed via an 11-bit address and an 8-bit data I/O parallel signals. The address inputs are multiplexed in row and column selected by control signal R/C# pin. The row addresses are mapped to the lower internal addresses (A_{10-0}), and the column addresses are mapped to the higher internal addresses (A_{MS-11}). See Figures 3 through 5, the Device Memory Maps, for address assignments.

LPC MODE

Device Operation

The LPC mode uses a 5-signal communication interface, a 4-bit address/data bus, LAD[3:0], and a control line, LFRAME#, to control operations of the SST49LF0x0A. Cycle type operations such as Memory Read and Memory Write are defined in Intel Low Pin Count Interface Specification, Revision 1.0. JEDEC Standard SDP (Software Data Protection) Program and Erase commands sequences are incorporated into the standard LPC memory cycles. See Figures 8 through 13 for command sequences.

LPC signals are transmitted via the 4-bit Address/Data bus (LAD[3:0]), and follow a particular sequence, depending on whether they are Read or Write operations. LPC memory Read and Write cycle is defined in Table 7.

Both LPC Read and Write operations start in a similar way as shown in Figures 6 and 7. The host (which is the term used here to describe the device driving the memory) asserts LFRAME# for one or more clocks and drives a start value on the LAD[3:0] bus.

At the beginning of an operation, the host may hold the LFRAME# active for several clock cycles, and even change the Start value. The LAD[3:0] bus is latched every rising edge of the clock. On the cycle in which LFRAME# goes inactive, the last latched value is taken as the Start value. CE# must be asserted one cycle before the start cycle to select the SST49LF0x0A for Read and Write operations.

Once the SST49LF0x0A identify the operation as valid (a start value of all zeros), it next expects a nibble that indicates whether this is a memory Read or Write cycle. Once this is received, the device is now ready for the Address cycles. The LPC protocol supports a 32-bit address phase. The SST49LF0x0A encode ID and register space access in the address field. See Tables 3 and 4 for address bits definition.

For Write operation the Data cycle will follow the Address cycle, and for Read operation TAR and SYNC cycles occur between the Address and Data cycles. At the end of every operation, the control of the bus must be returned to the host by a 2-clock TAR cycle.

TABLE 3: SST49LF030A[1] / SST49LF040A ADDRESS BITS DEFINITION

A_{31}: A_{24}	A_{23}	A_{22}	A_{21}: A_{19}	A_{18}:A_0
1111 1111b	ID[3][2]	1 = Memory Access 0 = Register access	ID[2:0][2]	Device Memory address

T3.5 554

1. The SST49LF030A features are equivalent to the SST49LF040A with 128 KByte less memory. For the SST49LF030A, operations beyond the 3 Mbit boundary (below 20000H) are not valid (see Device Memory Map).
2. See Table 9 for multiple device selection configuration.

TABLE 4: SST49LF080A ADDRESS BITS DEFINITION

A_{31}: A_{25}[1]	A_{24}:A_{23}	A_{22}	A_{21}: A_{20}	A_{19}:A_0
1111 111b or 0000 000b	ID[3:2][2]	1 = Memory Access 0 = Register access	ID[1:0][2]	Device Memory address

T4.6 554

1. For SST49LF080A, the top 32MByte address range FFFF FFFFH to FF00 0000H and the bottom 128 KByte memory access address 000F FFFFH to 000E 0000H are decoded.
2. See Table 9 for multiple device selection configuration

CE#

The CE# pin, enables and disables the SST49LF0x0A, controlling read and write access of the device. To enable the SST49LF0x0A, the CE# pin must be driven low one clock cycle prior to LFRAME# being driven low. The device will enter standby mode when internal Write operations are completed and CE# is high.

LFRAME#

The LFRAME# signifies the start of a (frame) bus cycle or the termination of an undesired cycle. Asserting LFRAME# for one or more clock cycle and driving a valid START value on LAD[3:0] will initiate device operation. The device will enter standby mode when internal operations are completed and LFRAME# is high.

TBL#, WP#

The Top Boot Lock (TBL#) and Write Protect (WP#) pins are provided for hardware write protection of device memory in the SST49LF0x0A. The TBL# pin is used to write protect 16 boot sectors (64 KByte) at the highest memory address range for the SST49LF0x0A. WP# pin write protects the remaining sectors in the flash memory.

An active low signal at the TBL# pin prevents Program and Erase operations of the top boot sectors. When TBL# pin is held high, the write protection of the top boot sectors is disabled. The WP# pin serves the same function for the remaining sectors of the device memory. The TBL# and WP# pins write protection functions operate independently of one another.

Both TBL# and WP# pins must be set to their required protection states prior to starting a Program or Erase operation. A logic level change occurring at the TBL# or WP# pin during a Program or Erase operation could cause unpredictable results.

INIT#, RST#

A V_{IL} on INIT# or RST# pin initiates a device reset. INIT# and RST# pins have the same function internally. It is required to drive INIT# or RST# pins low during a system reset to ensure proper CPU initialization. During a Read operation, driving INIT# or RST# pins low deselects the device and places the output drivers, LAD[3:0], in a high-impedance state. The reset signal must be held low for a minimal duration of time T_{RSTP}. A reset latency will occur if a reset procedure is performed during a Program or Erase operation. See Table 20, Reset Timing Parameters for more information. A device reset during an active Program or Erase will abort the operation and memory contents may become invalid due to data being altered or corrupted from an incomplete Erase or Program operation.

System Memory Mapping

The LPC interface protocol has address length of 32-bit or 4 GByte. The SST49LF0x0A will respond to addresses in the range as specified in Tables 5 and 6.

Refer to "Multiple Device Selection" section for more detail on strapping multiple SST49LF0x0A devices to increase memory densities in a system and "Registers" section on valid register addresses.

TABLE 5: ADDRESS DECODING RANGE FOR SST49LF030A[1] / SST49LF040A

ID Strapping	Device Access	Address Range	Memory Size
Device #0 - 7	Memory Access	FFFF FFFFH : FFC0 0000H	4 MByte
	Register Access	FFBF FFFFH : FF80 0000H	4 MByte
Device #8 - 15	Memory Access	FF7F FFFFH : FF40 0000H	4 MByte
	Register Access	FF3F FFFFH : FF00 0000H	4 MByte

T5.4 554

1. The SST49LF030A features are equivalent to the SST49LF040A with 128 KByte less memory. For the SST49LF030A, operations beyond the 3 Mbit boundary (below 20000H) are not valid (see Device Memory Map).

TABLE 6: ADDRESS DECODING RANGE FOR SST49LF080A

ID Strapping	Device Access	Address Range	Memory Size
Device #0 - 3	Memory Access	FFFF FFFFH : FFC0 0000H	4 MByte
	Register Access	FFBF FFFFH : FF80 0000H	4 MByte
Device #4 - 7	Memory Access	FF7F FFFFH : FF40 0000H	4 MByte
	Register Access	FF3F FFFFH : FF00 0000H	4 MByte
Device #8 - 11	Memory Access	FEFF FFFFH : FEC0 0000H	4 MByte
	Register Access	FEBF FFFFH : FE80 0000H	4 MByte
Device #12 - 15	Memory Access	FE7F FFFFH : FE40 0000H	4 MByte
	Register Access	FE3F FFFFH : FE00 0000H	4 MByte
Device #0[1]	Memory Access	000F FFFFH : 000E 0000H	128 KByte

T6.4 554

1. For device #0 (Boot Device), SST49LF080A decodes the 128KByte Bios ROM space 000F FFFFH through 000E 0000H and remaps those address locations to the same physical location for address range FFFF FFFFH through FFFE 0000H.

TABLE 7: LPC READ CYCLE

Clock Cycle	Field Name	Field Contents LAD[3:0][1]	LAD[3:0] Direction	Comments
1	START	0000	IN	LFRAME# must be active (low) for the SST49LF040A to respond. Only the last start field (before LFRAME# transitioning high) should be recognized.
2	CYCTYPE + DIR	010X	IN	Indicates the type of cycle. Bits 3:2 must be "01b" for memory cycle. Bit 1 indicates the type of transfer "0" for Read. Bit 0 is reserved.
3-10	ADDRESS	YYYY	IN	Address Phase for Memory Cycle. LPC protocol supports a 32-bit address phase. YYYY is one nibble of the entire address. Addresses are transferred most-significant nibble fist. See Tables 3 and 4 for address bits definition and Tables 5 and 6 for valid memory address range.
11	TAR0	1111	IN then Float	In this clock cycle, the host has driven the bus to all 1s and then floats the bus. This is the first part of the bus "turnaround cycle."
12	TAR1	1111 (float)	Float then OUT	The SST49LF0x0A takes control of the bus during this cycle
13	SYNC	0000	OUT	The SST49LF0x0A outputs the value 0000b indicating that data will be available during the next clock cycle.
14	DATA	ZZZZ	OUT	This field is the least-significant nibble of the data byte.
15	DATA	ZZZZ	OUT	This field is the most-significant nibble of the data byte.
16	TAR0	1111	IN then Float	In this clock cycle, the host has driven the bus to all 1s and then floats the bus. This is the first part of the bus "turnaround cycle."
17	TAR1	1111 (float)	Float then OUT	The SST49LF0x0A takes control of the bus during this cycle

T7.3 554

1. Field contents are valid on the rising edge of the present clock cycle.

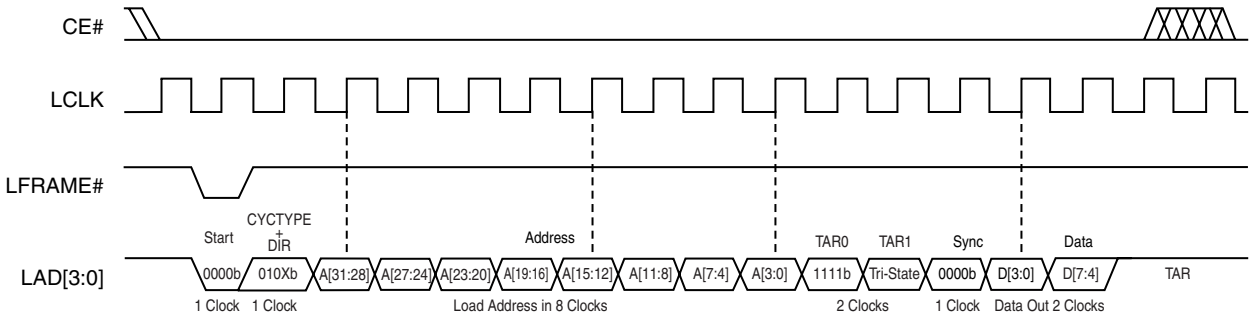


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FIGURE 6: LPC READ CYCLE WAVEFORM

TABLE 8: LPC WRITE CYCLE

Clock Cycle	Field Name	Field Contents LAD[3:0][1]	LAD[3:0] Direction	Comments
1	START	0000	IN	LFRAME# must be active (low) for the part to respond. Only the last start field (before LFRAME# transitioning high) should be recognized.
2	CYCTYPE + DIR	011X	IN	Indicates the type of cycle. Bits 3:2 must be “01b” for memory cycle. Bit 1 indicates the type of transfer “1” for Write. Bit 0 is reserved.
3-10	ADDRESS	YYYY	IN	Address Phase for Memory Cycle. LPC protocol supports a 32-bit address phase. YYYY is one nibble of the entire address. Addresses are transferred most-significant nibble first. See Tables 3 and 4 for address bit definition and Tables 5 and 6 for valid memory address range.
11	DATA	ZZZZ	IN	This field is the least-significant nibble of the data byte.
12	DATA	ZZZZ	IN	This field is the most-significant nibble of the data byte.
13	TAR0	1111	IN then Float	In this clock cycle, the host has driven the bus to all ‘1’s and then floats the bus. This is the first part of the bus “turnaround cycle.”
14	TAR1	1111 (float)	Float then OUT	The SST49LF0x0A takes control of the bus during this cycle.
15	SYNC	0000	OUT	The SST49LF0x0A outputs the values 0000, indicating that it has received data or a flash command.
16	TAR0	1111	OUT then Float	In this clock cycle, the SST49LF0x0A has driven the bus to all ‘1’s and then floats the bus. This is the first part of the bus “turnaround cycle.”
17	TAR1	1111 (float)	Float then IN	Host resumes control of the bus during this cycle.

T8.3 554

1. Field contents are valid on the rising edge of the present clock cycle.

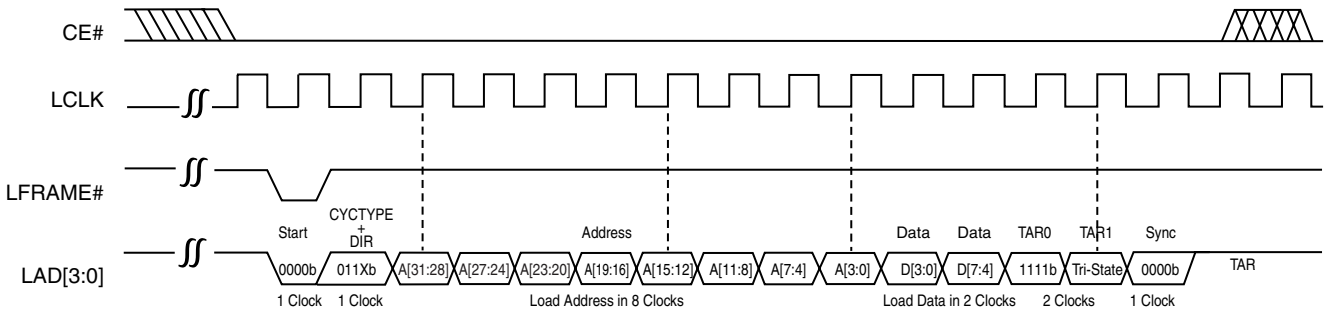

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FIGURE 7: LPC WRITE CYCLE WAVEFORM

Response To Invalid Fields

During LPC Read/Write operations, the SST49LF0x0A will not explicitly indicate that it has received invalid field sequences. The response to specific invalid fields or sequences is as follows:

Address out of range: The SST49LF0x0A will only response to address range as specified in Tables 5 and 6.

The SST49LF030A features are equivalent to the SST49LF040A with 128 KByte less memory. For the SST49LF030A, operations beyond the 3 Mbit boundary (below 20000H) are not valid (see Device Memory Map).

ID mismatch: ID information is included in every address cycle. The SST49LF0x0A will compare ID bits in the address field with the hardware ID strapping. If there is a mis-match, the device will ignore the cycle. See Multiple Device Selection section for details.

Once valid START, CYCTYPE + DIR, valid address range and ID bits are received, the SST49LF0x0A will always complete the bus cycle. However, if the device is busy performing a flash Erase or Program operation, no new internal Write command (memory write or register write) will be executed. As long as the states of LAD[3:0] and LAD[4] are known, the response of the ST49LF0x0A to signals received during the LPC cycle should be predictable.

Abort Mechanism

If LFRAME# is driven low for one or more clock cycles after the start of an LPC cycle, the cycle will be terminated. The host may drive the LAD[3:0] with '1111b' (ABORT nibble) to return the interface to ready mode. The ABORT only affects the current bus cycle. For a multi-cycle command sequence, such as the Erase or Program SDP commands, ABORT doesn't interrupt the entire command sequence, but only the current bus cycle of the command sequence. The host can re-send the bus cycle and continue the SDP command sequence after the device is ready again.

Write Operation Status Detection

The SST49LF0x0A device provides two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: Data# Polling, D[7], and Toggle Bit, D[6]. The End-of-Write detection mode is incorporated into the LPC Read Cycle. The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either D[7] or D[6]. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Data# Polling

When the SST49LF0x0A device is in the internal Program operation, any attempt to read D[7] will produce the complement of the true data. Once the Program operation is completed, D[7] will produce true data. Note that even though D[7] may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1 µs. During internal Erase operation, any attempt to read D[7] will produce a '0'. Once the internal Erase operation is completed, D[7] will produce a '1'. Proper status will not be given using Data# Polling if the address is in the invalid range.

Toggle Bit

During the internal Program or Erase operation, any consecutive attempts to read D[6] will produce alternating 0s and 1s, i.e., toggling between 0 and 1. When the internal Program or Erase operation is completed, the toggling will stop.

Multiple Device Selection

Multiple LPC flash devices may be strapped to increase memory densities in a system. The four ID pins, ID[3:0], allow up to 16 devices to be attached to the same bus by using different ID strapping in a system. BIOS support, bus loading, or the attaching bridge may limit this number. The boot device must have an ID of 0 (determined by ID[3:0]); subsequent devices use incremental numbering. Equal density must be used with multiple devices.

When used as a boot device, ID[3:0] must be strapped as 0000; all subsequent devices should use a sequential up-count strapping (i.e. 0001, 0010, 0011, etc.). With the hardware strapping, ID information is included in every LPC address memory cycle. The ID bits in the address field are inverse of the hardware strapping. The address bits [A_{23}, A_{21}:A_{19}] for SST49LF030A and SST49LF040A and [A_{24}:A_{23}, A_{21}:A_{20}] for SST49LF080A are used to select the device with proper IDs. See Table 9 for IDs. The SST49LF0x0A will compare these bits with ID[3:0]'s strapping values. If there is a mismatch, the device will ignore the reminder of the cycle.

TABLE 9: MULTIPLE DEVICE SELECTION CONFIGURATION

Device #	Hardware Strapping ID[3:0]	Address Bits Decoding							
		SST49LF030A[1] / SST49LF040A				SST49LF080A			
		A_{23}	A_{21}	A_{20}	A_{19}	A_{24}	A_{23}	A_{21}	A_{20}
0 (Boot device)	0000	1	1	1	1	1	1	1	1
1	0001	1	1	1	0	1	1	1	0
2	0010	1	1	0	1	1	1	0	1
3	0011	1	1	0	0	1	1	0	0
4	0100	1	0	1	1	1	0	1	1
5	0101	1	0	1	0	1	0	1	0
6	0110	1	0	0	1	1	0	0	1
7	0111	1	0	0	0	1	0	0	0
8	1000	0	1	1	1	0	1	1	1
9	1001	0	1	1	0	0	1	1	0
10	1010	0	1	0	1	0	1	0	1
11	1011	0	1	0	0	0	1	0	0
12	1100	0	0	1	1	0	0	1	1
13	1101	0	0	1	0	0	0	1	0
14	1110	0	0	0	1	0	0	0	1
15	1111	0	0	0	0	0	0	0	0

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1. The SST49LF030A features are equivalent to the SST49LF040A with 128 KByte less memory. For the SST49LF030A, operations beyond the 3 Mbit boundary (below 20000H) are not valid (see Device Memory Map).

Registers

There are two registers available on the SST49LF0x0A, the General Purpose Inputs Registers (GPI_REG) and the JEDEC ID Registers. Since multiple LPC memory devices may be used to increase memory densities, these registers appear at its respective address location in the 4 GByte system memory map. Unused register locations will read as 00H. Any attempt to read registers during internal Write operation will respond as "Write operation status detection" (Data# Polling or Toggle Bit). Any attempt to write any registers during internal Write operation will be ignored. Tables 11 and 12 list GPI_REG and JEDEC ID address locations for SST49LF0x0A with its respective device strapping.

TABLE 10: GENERAL PURPOSE INPUTS REGISTER

Bit	Function	Pin #	
		32-PLCC	32-TSOP
7:5	Reserved	-	-
4	GPI[4] Reads status of general purpose input pin	30	6
3	GPI[3] Reads status of general purpose input pin	3	11
2	GPI[2] Reads status of general purpose input pin	4	12
1	GPI[1] Reads status of general purpose input pin	5	13
0	GPI[0] Reads status of general purpose input pin	6	14

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General Purpose Inputs Register

The GPI_REG (General Purpose Inputs Register) passes the state of GPI[4:0] pins at power-up on the SST49LF0x0A. It is recommended that the GPI[4:0] pins be in the desired state before LFRAME# is brought low for the beginning of the next bus cycle, and remain in that state until the end of the cycle. There is no default value since this is a pass-through register. See General Purpose Inputs Register table for the GPI_REG bits and function, and Tables 11 and 12 for memory address location for its respective device strapping.

JEDEC ID Registers

The JEDEC ID registers identify the device as SST49LF0x0A and manufacturer as SST in LPC mode. See Tables 11 and 12 for memory address location for its respective JEDEC ID location.

TABLE 11: MEMORY MAP REGISTER ADDRESSES FOR SST49LF030A[1] / SST49LF040A

Device #	GPI_REG	JEDEC ID	
		Manufacturer	Device
0 (Boot device)	FFBC 0100H	FFBC 0000H	FFBC 0001H
1	FFB4 0100H	FFB4 0000H	FFB4 0001H
2	FFAC 0100H	FFAC 0000H	FFAC 0001H
3	FFA4 0100H	FFA4 0000H	FFA4 0001H
4	FF9C 0100H	FF9C 0000H	FF9C 0001H
5	FF94 0100H	FF94 0000H	FF94 0001H
6	FF8C 0100H	FF8C 0000H	FF8C 0001H
7	FF84 0100H	FF84 0000H	FF84 0001H
8	FF3C 0100H	FF3C 0000H	FF3C 0001H
9	FF34 0100H	FF34 0000H	FF34 0001H
10	FF2C 0100H	FF2C 0000H	FF2C 0001H
11	FF24 0100H	FF24 0000H	FF24 0001H
12	FF1C 0100H	FF1C 0000H	FF1C 0001H
13	FF14 0100H	FF14 0000H	FF14 0001H
14	FF0C 0100H	FF0C 0000H	FF0C 0001H
15	FF04 0100H	FF04 0000H	FF04 0001H

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1. The SST49LF030A features are equivalent to the SST49LF040A with 128 KByte less memory. For the SST49LF030A, operations beyond the 3 Mbit boundary (below 20000H) are not valid (see Device Memory Map.

TABLE 12: MEMORY MAP REGISTER ADDRESSES FOR SST49LF080A

Device #	GPI_REG	JEDEC ID	
		Manufacturer	Device
0 (Boot device)	FFBC 0100H	FFBC 0000H	FFBC 0001H
1	FFAC 0100H	FFAC 0000H	FFAC 0001H
2	FF9C 0100H	FF9C 0000H	FF9C 0001H
3	FF8C 0100H	FF8C 0000H	FF8C 0001H
4	FF3C 0100H	FF3C 0000H	FF3C 0001H
5	FF2C 0100H	FF2C 0000H	FF2C 0001H
6	FF1C 0100H	FF1C 0000H	FF1C 0001H
7	FF0C 0100H	FF0C 0000H	FF0C 0001H
8	FEBC 0100H	FEBC 0000H	FEBC 0001H
9	FEAC 0100H	FEAC 0000H	FEAC 0001H
10	FE9C 0100H	FE9C 0000H	FE9C 0001H
11	FE8C 0100H	FE8C 0000H	FE8C 0001H
12	FE3C 0100H	FE3C 0000H	FE3C 0001H
13	FE2C 0100H	FE2C 0000H	FE2C 0001H
14	FE1C 0100H	FE1C 0000H	FE1C 0001H
15	FE0C 0100H	FE0C 0000H	FE0C 0001H

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PARALLEL PROGRAMMING MODE

Device Operation

Commands are used to initiate the memory operation functions of the device. The data portion of the software command sequence is latched on the rising edge of WE#. During the software command sequence the row address is latched on the falling edge of R/C# and the column address is latched on the rising edge of R/C#.

Reset

Driving the RST# low will initiate a hardware reset of the SST49LF0x0A. See Table 26 for Reset timing parameters and Figure 18 for Reset timing diagram.

Read

The Read operation of the SST49LF0x0A device is controlled by OE#. OE# is the output control and is used to gate data from the output pins. Refer to the Read cycle timing diagram, Figure 19, for further details.

Byte-Program Operation

The SST49LF0x0A devices are programmed on a byte-by-byte basis. Before programming, one must ensure that the sector in which the byte is programmed is fully erased. The Byte-Program operation is initiated by executing a four-byte command load sequence for Software Data Protection with address (BA) and data in the last byte sequence. During the Byte-Program operation, the row address (A_{10}-A_0) is latched on the falling edge of R/C# and the column address (A_{21}-A_{11}) is latched on the rising edge of R/C#. The data bus is latched on the rising edge of WE#. The Program operation, once initiated, will be completed, within 20 µs. See Figure 23 for Program operation timing diagram and Figure 35 for its flowchart. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands written during the internal Program operation will be ignored.

Sector-Erase Operation

The Sector-Erase operation allows the system to erase the device on a sector-by-sector basis. The sector architecture is based on uniform sector size of 4 KByte. The Sector-Erase operation is initiated by executing a six-byte command load sequence for Software Data Protection with Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase can be determined using either Data# Polling or Toggle Bit methods. See Figure 24 for Sector-Erase timing waveforms. Any commands written during the Sector-Erase operation will be ignored.

Block-Erase Operation

The Block-Erase Operation allows the system to erase the device in 64 KByte uniform block size. The Block-Erase operation is initiated by executing a six-byte command load sequence for Software Data Protection with Block-Erase command (50H) and block address. The internal Block-Erase operation begins after the sixth WE# pulse. The End-of-Erase can be determined using either Data# Polling or Toggle Bit methods. See Figure 25 for Block-Erase timing waveforms. Any commands written during the Block-Erase operation will be ignored.

Chip-Erase Operation

The SST49LF0x0A devices provide a Chip-Erase operation, which allows the user to erase the entire memory array to the “1s” state. This is useful when the entire device must be quickly erased.

The Chip-Erase operation is initiated by executing a six-byte Software Data Protection command sequence with Chip-Erase command (10H) with address 5555H in the last byte sequence. The internal Erase operation begins with the rising edge of the sixth WE#. During the internal Erase operation, the only valid read is Toggle Bit or Data# Polling. See Table 14 for the command sequence, Figure 26 for Chip-Erase timing diagram, and Figure 38 for the flowchart. Any commands written during the Chip-Erase operation will be ignored.

Write Operation Status Detection

The SST49LF0x0A devices provide two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: Data# Polling D[7] and Toggle Bit D[6]. The End-of-Write detection mode is enabled after the rising edge of WE# which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either D[7] or D[6]. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Data# Polling (DQ_7)

When the SST49LF0x0A devices are in the internal Program operation, any attempt to read DQ_7 will produce the complement of the true data. Once the Program operation is completed, DQ_7 will produce true data. Note that even though DQ_7 may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1 µs. During internal Erase operation, any attempt to read DQ_7 will produce a ‘0’. Once the internal Erase operation is completed, DQ_7 will produce a ‘1’. The Data# Polling is valid after the rising edge of fourth WE# pulse for Program operation. For Sector-, Block-, or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# pulse. See Figure 21 for Data# Polling timing diagram and Figure 36 for a flowchart. Proper status will not be given using Data# Polling if the address is in the invalid range.

Toggle Bit (DQ_6)

During the internal Program or Erase operation, any consecutive attempts to read DQ_6 will produce alternating 0s and 1s, i.e., toggling between 0 and 1. When the internal Program or Erase operation is completed, the toggling will stop. The device is then ready for the next operation. The Toggle Bit is valid after the rising edge of fourth WE# pulse for Program operation. For Sector-, Block-, or Chip-Erase, the Toggle Bit is valid after the rising edge of sixth WE# pulse. See Figure 22 for Toggle Bit timing diagram and Figure 36 for a flowchart.

TABLE 13: OPERATION MODES SELECTION (PP MODE)

Mode	RST#	OE#	WE#	DQ	Address
Read	V_{IH}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Program	V_{IH}	V_{IH}	V_{IL}	D_{IN}	A_{IN}
Erase	V_{IH}	V_{IH}	V_{IL}	X[1]	Sector or Block address, XXH for Chip-Erase
Reset	V_{IL}	X	X	High Z	X
Write Inhibit	V_{IH}	V_{IL}	X	High Z/D_{OUT}	X
	X	X	V_{IH}	High Z/D_{OUT}	X
Product Identification	V_{IH}	V_{IL}	V_{IH}	Manufacturer's ID (BFH) Device ID[2]	See Table 14

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1. X can be V_{IL} or V_{IH}, but no other value.
2. Device ID 1CH for SST49LF030A, 53H for SST49LF040A and 5BH for SST49LF080A

Data Protection (PP Mode)

The SST49LF0x0A devices provide both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# pulse of less than 5 ns will not initiate a Write cycle.

V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The SST49LF0x0A provide the JEDEC approved Software Data Protection scheme for all data alteration operation, i.e., Program and Erase. Any Program operation requires the inclusion of a series of three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of a six-byte load sequence.

Advance Information

SOFTWARE COMMAND SEQUENCE

TABLE 14: SOFTWARE COMMAND SEQUENCE

Command Sequence	1st[1] Cycle		2nd[1] Cycle		3rd[1] Cycle		4th[1] Cycle		5th[1] Cycle		6th[1] Cycle	
	Addr[2]	Data	Addr[2]	Data	Addr[2]	Data	Addr[2]	Data	Addr[2]	Data	Addr[2]	Data
Byte-Program	YYYY 5555H	AAH	YYYY 2AAAH	55H	YYYY 5555H	A0H	PA[3]	Data				
Sector-Erase	YYYY 5555H	AAH	YYYY 2AAAH	55H	YYYY 5555H	80H	YYYY 5555H	AAH	YYYY 2AAAH	55H	SA_X[4]	30H
Block-Erase	YYYY 5555H	AAH	YYYY 2AAAH	55H	YYYY 5555H	80H	YYYY 5555H	AAH	YYYY 2AAAH	55H	BA_X[5]	50H
Chip-Erase[6]	YYYY 5555H	AAH	YYYY 2AAAH	55H	YYYY 5555H	80H	YYYY 5555H	AAH	YYYY 2AAAH	55H	YYYY 5555H	10H
Software ID Entry	YYYY 5555H	AAH	YYYY 2AAAH	55H	YYYY 5555H	90H	Read ID[7]					
Software ID Exit[8]	XXXX XXXXH	F0H										
Software ID Exit[8]	YYYY 5555H	AAH	YYYY 2AAAH	55H	YYYY 5555H	F0H						

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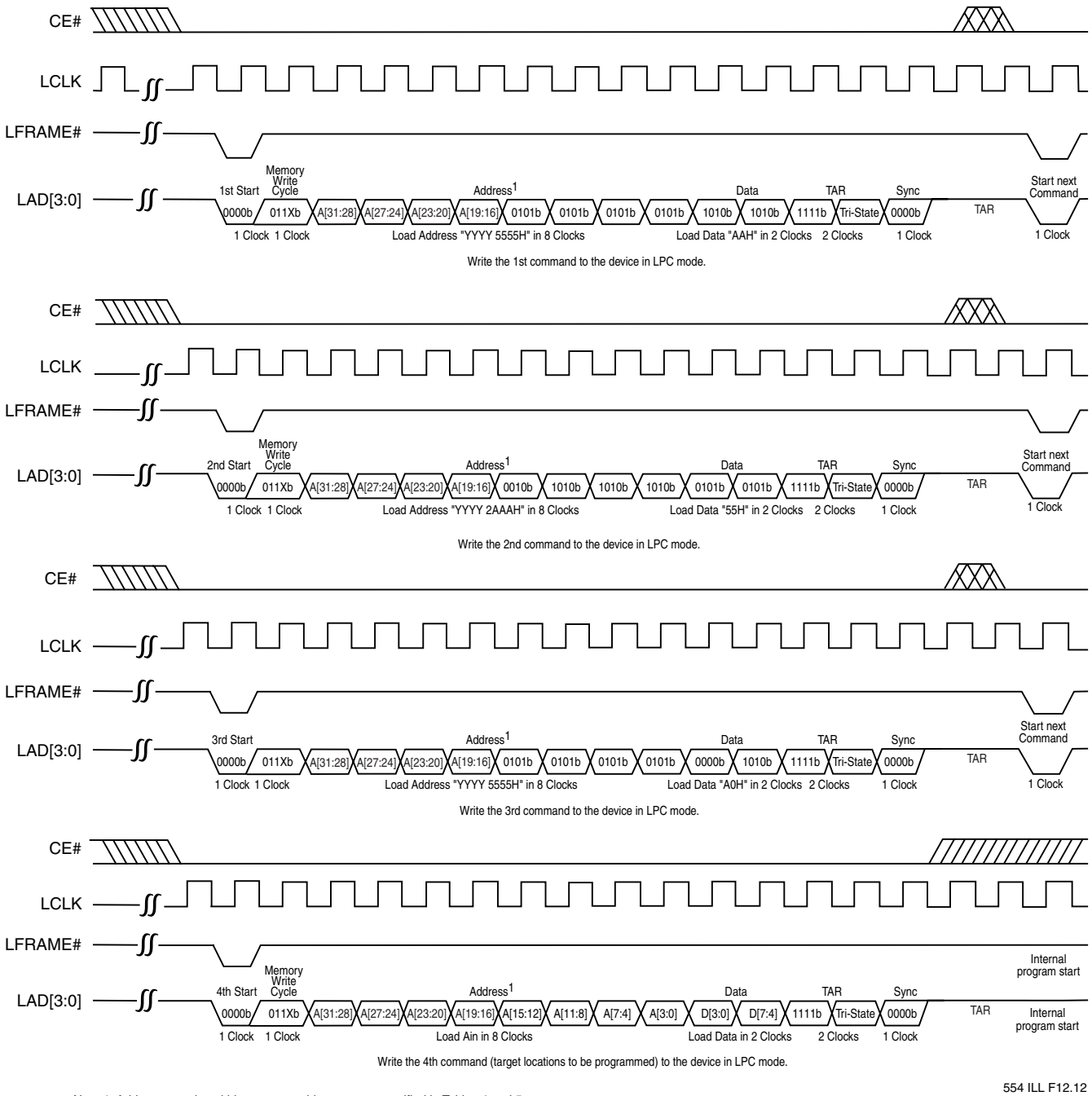
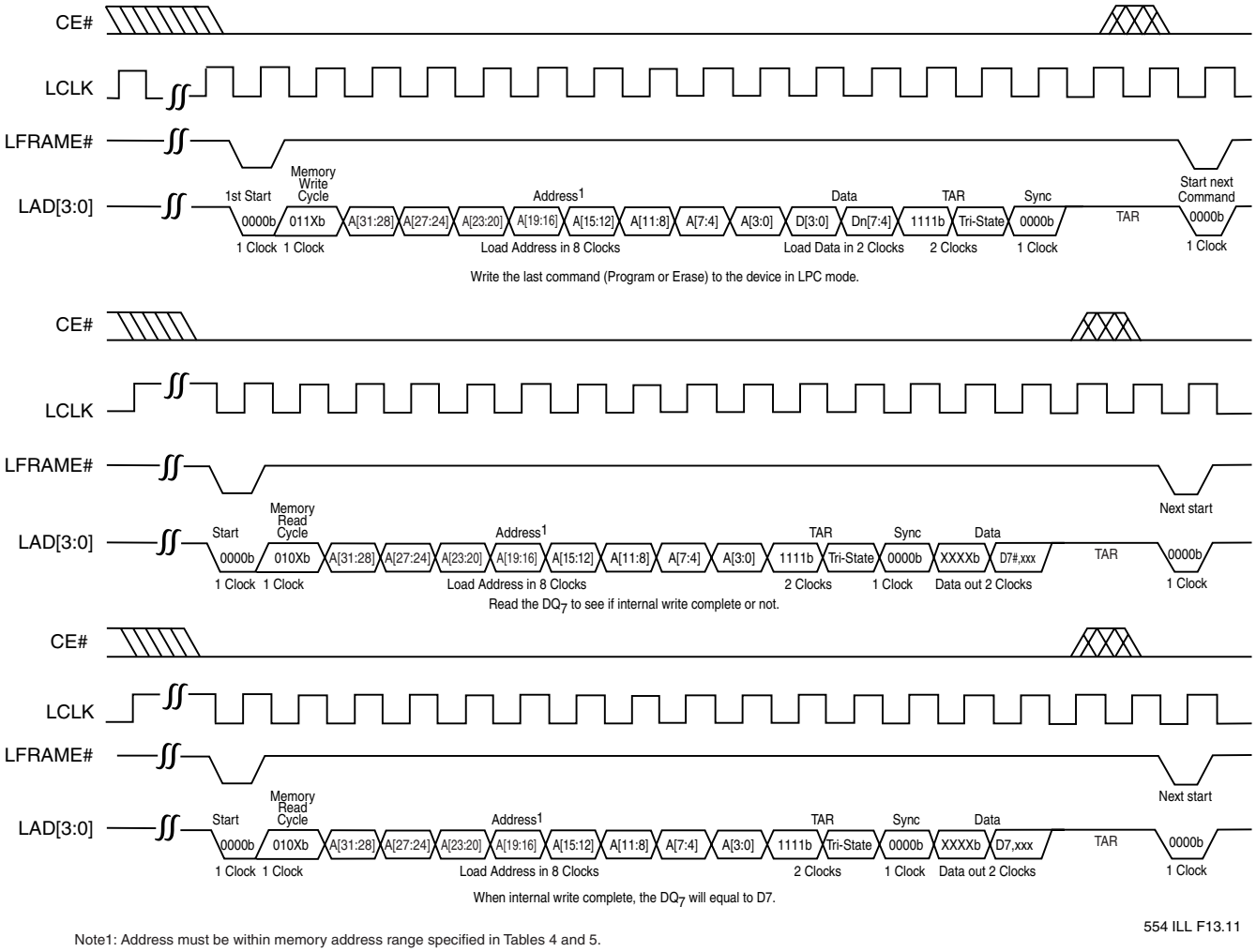
1. LPC mode use consecutive Write cycles to complete a command sequence; PP mode use consecutive bus cycles to complete a command sequence.
2. YYYY = A[31:16]. In LPC mode, during SDP command sequence, YYYY must be within memory address range specified in Tables 5 and 6. In PP mode, YYYY can be V_{IL} or V_{IH}, but no other value.
3. PA = Program Byte address
4. SA_X for Sector-Erase Address
5. BA_X for Block-Erase Address
6. Chip-Erase is supported in PP mode only
7. SST Manufacturer's ID = BFH, is read with A_0 = 0.
   With A_{18}-A_1 = 0; 49LF030A Device ID = 1CH, are read with A_0 = 1.
   With A_{18}-A_1 = 0; 49LF040A Device ID = 53H, are read with A_0 = 1.
   With A_{19}-A_1 = 0; 49LF080A Device ID = 5BH, are read with A_0 = 1.
8. Both Software ID Exit operations are equivalent



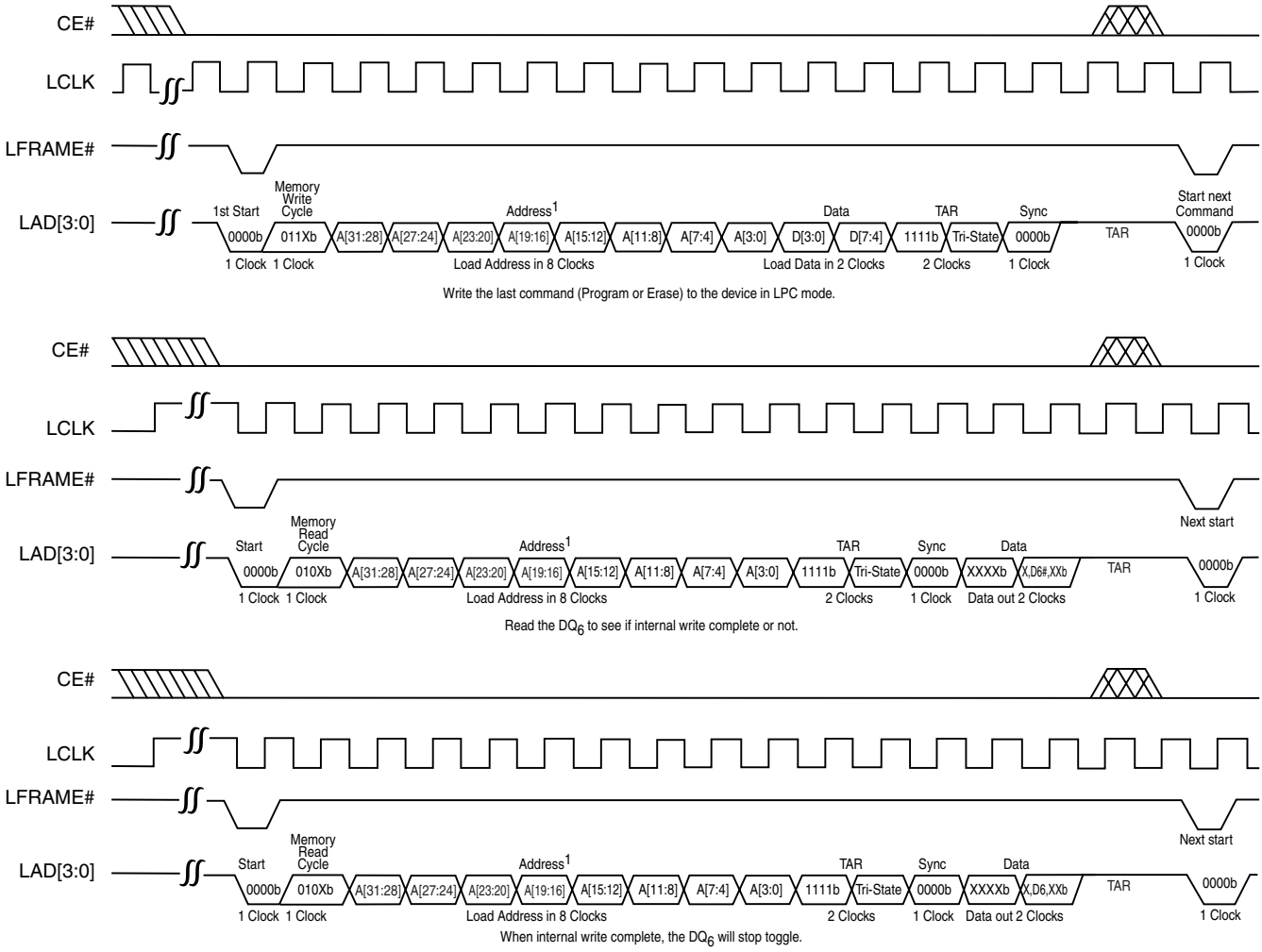
Note 1: Address must be within memory address range specified in Tables 4 and 5.

FIGURE 8: PROGRAM COMMAND SEQUENCE (LPC MODE)



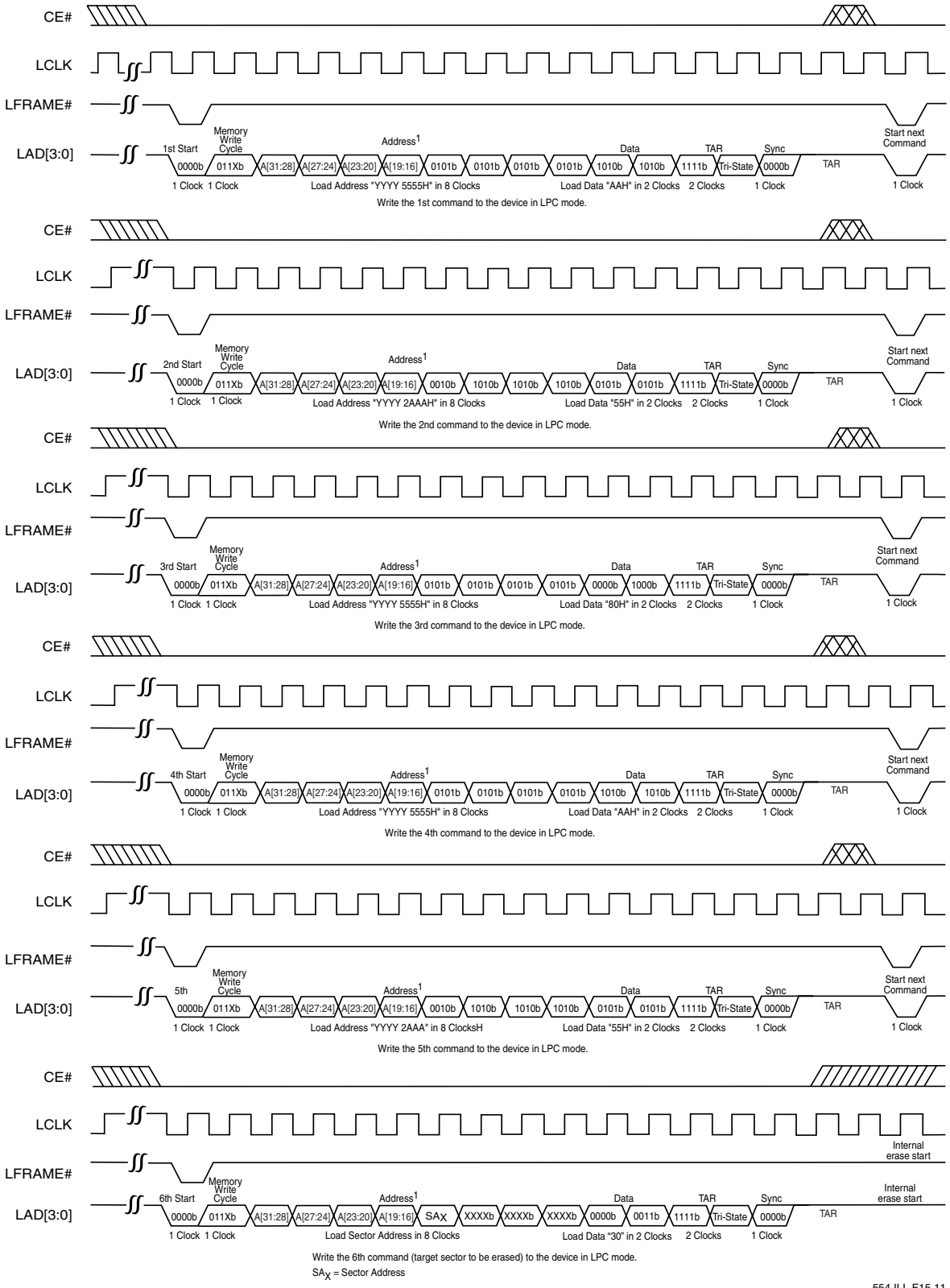
Note1: Address must be within memory address range specified in Tables 4 and 5.

FIGURE 9: DATA# POLLING COMMAND SEQUENCE (LPC MODE)



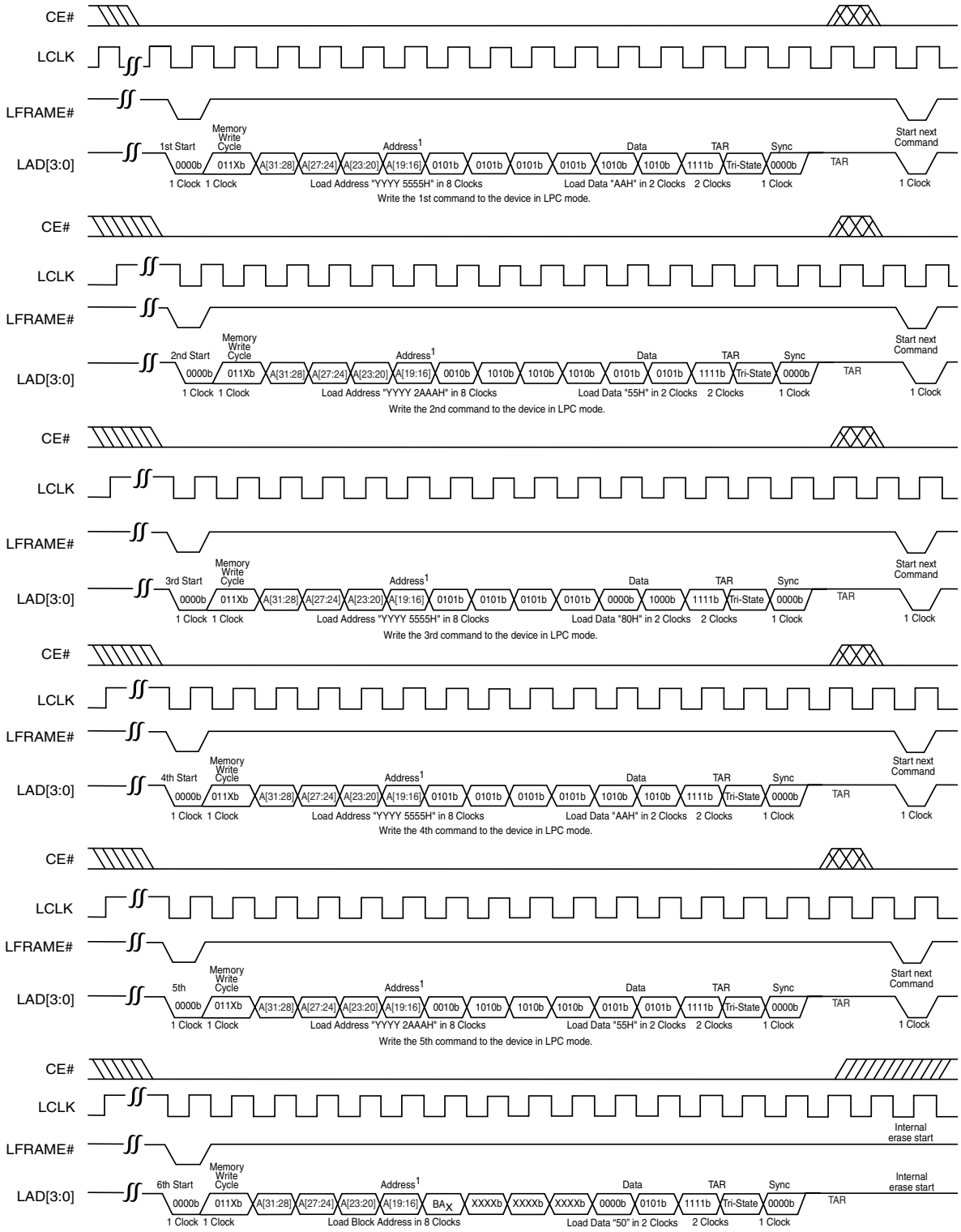
Note 1: Address must be within memory address range specified in Tables 4 and 5.

FIGURE 10: TOGGLE BIT COMMAND SEQUENCE (LPC MODE)



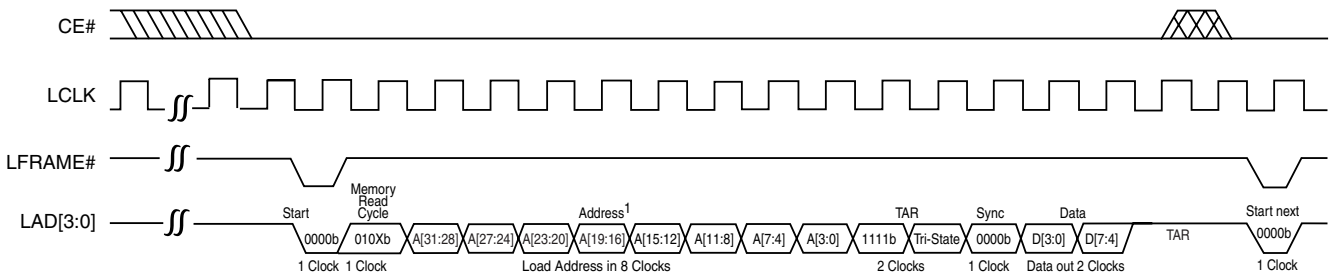
Note 1: Address must be within memory address range specified in Tables 4 and 5.

FIGURE 11: SECTOR-ERASE COMMAND SEQUENCE (LPC MODE)



Note1: Address must be within memory address range specified in Tables 4 and 5.

FIGURE 12: BLOCK-ERASE COMMAND SEQUENCE (LPC MODE)



Note1: See Tables 10 and 11 for Register Addresses

FIGURE 13: REGISTER READOUT COMMAND SEQUENCE (LPC MODE)

ELECTRICAL SPECIFICATIONS

The AC and DC specifications for the LPC interface signals (LA0[3:0], LFRAME, LCLCK and RST#) as defined in Section 4.2.2.4 of the PCI local Bus specification, Rev. 2.1. Refer to Table 15 for the DC voltage and current specifications. Refer to Tables 19 through 22 and Tables 24 through 26 for the AC timing specifications for Clock, Read, Write, and Reset operations.

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this datasheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
D.C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -2.0V to V_{DD}+2.0V
Package Power Dissipation Capability (Ta=25°C) 1.0W
Surface Mount Lead Soldering Temperature (3 Seconds) . . . . . 240°C
Output Short Circuit Current[1] . . . . . 50 mA

1. Outputs shorted for no more than one second. No more than one output shorted at a time.

OPERATING RANGE

Range	Ambient Temp	V_{DD}
Commercial	0°C to +85°C	3.0-3.6V

AC CONDITIONS OF TEST

Input Rise/Fall Time . . . . . 3 ns
Output Load . . . . . C_L = 30 pF
See Figures 29 and 30

DC Characteristics

TABLE 15: DC OPERATING CHARACTERISTICS (ALL INTERFACES)

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}[1]	Active V_{DD} Current				All inputs = V_{IL} or V_{IH}
	Read		12	mA	All outputs = open, V_{DD}=V_{DD} Max
	Write		24	mA	See Note [2]
I_{SB}	Standby V_{DD} Current (LPC Interface)		100	µA	LFRAME#=V_{IH}, f=33 MHz, CE#=V_{IH} V_{DD}=V_{DD} Max, All other inputs ≥ 0.9 V_{DD} or ≤ 0.1 V_{DD}
I_{RY}[3]	Ready Mode V_{DD} Current (LPC Interface)		10	mA	LFRAME#=V_{IL}, f=33 MHz, V_{DD}=V_{DD} Max All other inputs ≥ 0.9 V_{DD} or ≤ 0.1 V_{DD}
I_I	Input Current for Mode and ID[3:0] pins		200	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LI}	Input Leakage Current		1	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LO}	Output Leakage Current		1	µA	V_{OUT}=GND to V_{DD}, V_{DD}=V_{DD} Max
V_{IHI}	INIT# Input High Voltage	1.1	V_{DD}+0.5	V	V_{DD}=V_{DD} Max
V_{ILI}	INIT# Input Low Voltage	-0.5	0.4	V	V_{DD}=V_{DD} Max
V_{IL}	Input Low Voltage	-0.5	0.3 V_{DD}	V	V_{DD}=V_{DD} Min
V_{IH}	Input High Voltage	0.5 V_{DD}	V_{DD}+0.5	V	V_{DD}=V_{DD} Max
V_{OL}	Output Low Voltage		0.1 V_{DD}	V	I_{OL}=1500 µA, V_{DD}=V_{DD} Min
V_{OH}	Output High Voltage	0.9 V_{DD}		V	I_{OH}=-500 µA, V_{DD}=V_{DD} Min

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1. I_{DD} active while a Read or Write (Program or Erase) operation is in progress.
2. For PP Mode: OE# = WE# = V_{IH}; For LPC Mode: f = 1/T_{RC} min, LFRAME# = V_{IH}, CE# = V_{IL}.
3. The device is in Ready mode when no activity is on the LPC bus.

TABLE 16: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Write Operation	100	µs

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter

TABLE 17: PIN CAPACITANCE (V_{DD}=3.3V, Ta=25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$=0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN}=0V	12 pF

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 18: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 19: CLOCK TIMING PARAMETERS (LPC MODE)

Symbol	Parameter	Min	Max	Units
T_{CYC}	LCLK Cycle Time	30		ns
T_{HIGH}	LCLK High Time	11		ns
T_{LOW}	LCLK Low Time	11		ns
-	LCLK Slew Rate (peak-to-peak)	1	4	V/ns
-	RST# or INIT# Slew Rate	50		mV/ns

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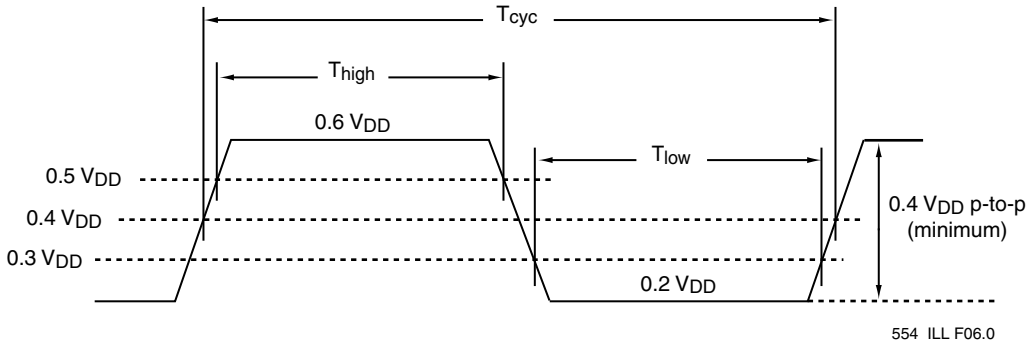


FIGURE 14: LCLK WAVEFORM (LPC MODE)

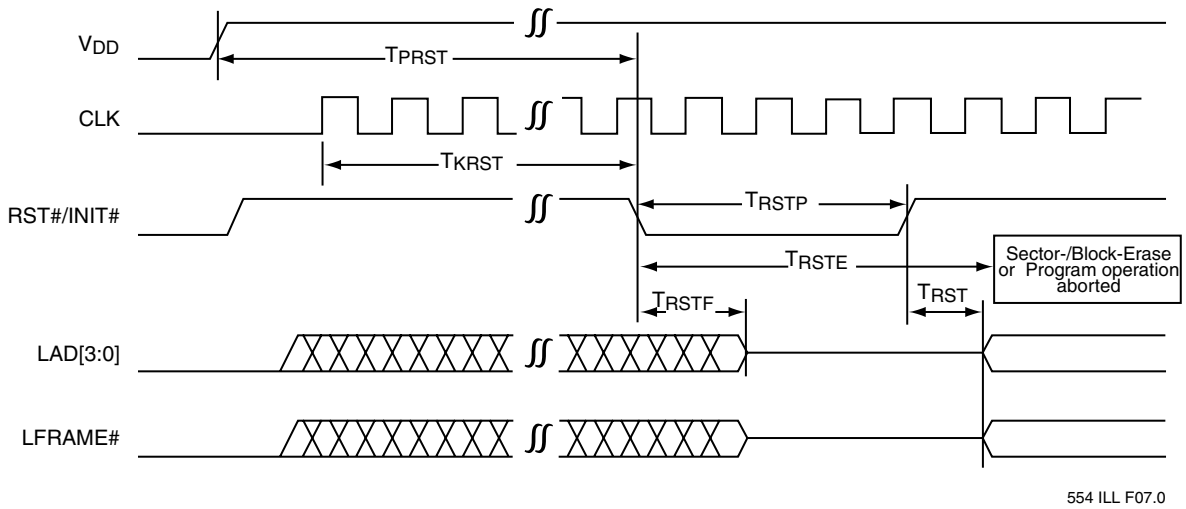
Advance Information

TABLE 20: RESET TIMING PARAMETERS, V_{DD}=3.0-3.6V (LPC MODE)

Symbol	Parameter	Min	Max	Units
T_{PRST}	V_{DD} stable to Reset Low	1		ms
T_{KRST}	Clock Stable to Reset Low	100		µs
T_{RSTP}	RST# Pulse Width	100		ns
T_{RSTF}	RST# Low to Output Float		48	ns
T_{RST}[1]	RST# High to LFRAME# Low	1		µs
T_{RSTE}	RST# Low to reset during Sector-/Block-Erase or Program		10	µs

T20.0 554

1. There may be additional latency due toT_{RSTE} if a reset procedure is performed during a Program or Erase operation.



554 ILL F07.0

FIGURE 15: RESET TIMING DIAGRAM (LPC MODE)

AC Characteristics

TABLE 21: READ/WRITE CYCLE TIMING PARAMETERS, V_{DD}=3.0-3.6V (LPC MODE)

Symbol	Parameter	Min	Max	Units
T_{CYC}	Clock Cycle Time	30		ns
T_{SU}	Data Set Up Time to Clock Rising	7		ns
T_{DH}	Clock Rising to Data Hold Time	0		ns
T_{VAL}[1]	Clock Rising to Data Valid	2	11	ns
T_{BP}	Byte Programming Time		20	µs
T_{SE}	Sector-Erase Time		25	ms
T_{BE}	Block-Erase Time		25	ms
T_{ON}	Clock Rising to Active (Float to Active Delay)	2		ns
T_{OFF}	Clock Rising to Inactive (Active to Float Delay)		28	ns

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1. Minimum and maximum times have different loads. See PCI spec.

TABLE 22: AC INPUT/OUTPUT SPECIFICATIONS (LPC MODE)

Symbol	Parameter	Min	Max	Units	Conditions
I_{OH}(AC)	Switching Current High	-12 V_{DD}		mA	$0 < V_{OUT} \leq 0.3\ V_{DD}$
		-17.1(V_{DD}-V_{OUT})		mA	$0.3\ V_{DD} < V_{OUT} < 0.9\ V_{DD}$
			Equation C[1]		$0.7\ V_{DD} < V_{OUT} < V_{DD}$
	(Test Point)		-32 V_{DD}	mA	$V_{OUT} = 0.7\ V_{DD}$
I_{OL}(AC)	Switching Current Low	16 V_{DD}	Equation D[1]	mA	$V_{DD} > V_{OUT} \geq 0.6\ V_{DD}$
		26.7 V_{OUT}		mA	$0.6\ V_{DD} > V_{OUT} > 0.1\ V_{DD}$
					$0.18\ V_{DD} > V_{OUT} > 0$
	(Test Point)		38 V_{DD}	mA	$V_{OUT} = 0.18\ V_{DD}$
I_{CL}	Low Clamp Current	-25+(V_{IN}+1)/0.015		mA	$-3 < V_{IN} \leq -1$
I_{CH}	High Clamp Current	25+(V_{IN}-V_{DD}-1)/0.015		mA	$V_{DD}+4 > V_{IN} \geq V_{DD}+1$
slewr[2]	Output Rise Slew Rate	1	4	V/ns	0.2 V_{DD}-0.6 V_{DD} load
slewf[2]	Output Fall Slew Rate	1	4	V/ns	0.6 V_{DD}-0.2 V_{DD} load

T22.0 554

1. See PCI spec.
2. PCI specification output load is used.

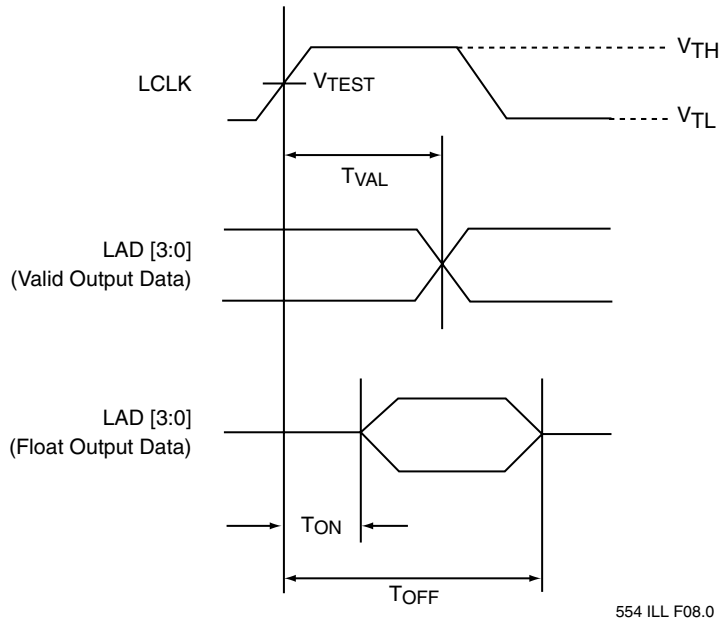


FIGURE 16: OUTPUT TIMING PARAMETERS (LPC MODE)

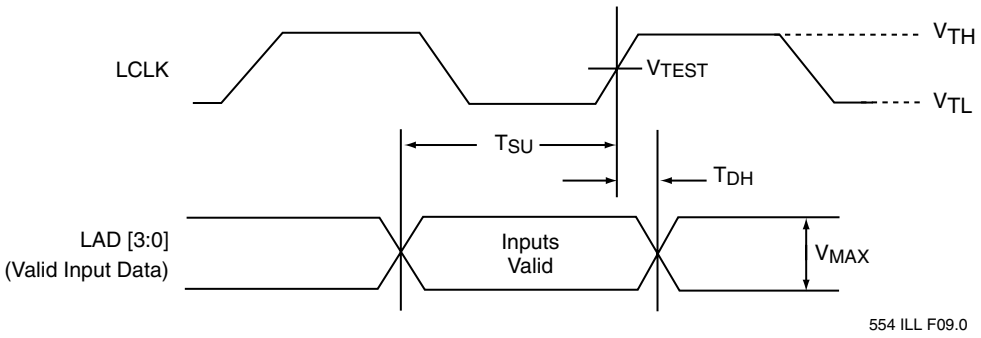


FIGURE 17: INPUT TIMING PARAMETERS (LPC MODE)

TABLE 23: INTERFACE MEASUREMENT CONDITION PARAMETERS (LPC MODE)

Symbol	Value	Units
V_{TH}[1]	0.6 V_{DD}	V
V_{TL}[1]	0.2 V_{DD}	V
V_{TEST}	0.4 V_{DD}	V
V_{MAX}[1]	0.4 V_{DD}	V
Input Signal Edge Rate	1 V/ns	

T23.0 554

1. The input test environment is done with 0.1 V_{DD} of overdrive over V_{IH} and V_{IL}. Timing parameters must be met with no more overdrive than this. V_{MAX} specified the maximum peak-to-peak waveform allowed for measuring input timing. Production testing may use different voltage values, but must correlate results back to these parameters

TABLE 24: READ CYCLE TIMING PARAMETERS, V_{DD}=3.0-3.6V (PP MODE)

Symbol	Parameter	Min	Max	Units
T_{RC}	Read Cycle Time	270		ns
T_{RST}	RST# High to Row Address Setup	1		µs
T_{AS}	R/C# Address Set-up Time	45		ns
T_{AH}	R/C# Address Hold Time	45		ns
T_{AA}	Address Access Time		120	ns
T_{OE}	Output Enable Access Time		60	ns
T_{OLZ}	OE# Low to Active Output	0		ns
T_{OHZ}	OE# High to High-Z Output		35	ns
T_{OH}	Output Hold from Address Change	0		ns

T24.0 554

TABLE 25: PROGRAM/ERASE CYCLE TIMING PARAMETERS, V_{DD}=3.0-3.6V (PP MODE)

Symbol	Parameter	Min	Max	Units
T_{RST}	RST# High to Row Address Setup	1		µs
T_{AS}	R/C# Address Setup Time	50		ns
T_{AH}	R/C# Address Hold Time	50		ns
T_{CWH}	R/C# to Write Enable High Time	50		ns
T_{OES}	OE# High Setup Time	20		ns
T_{OEH}	OE# High Hold Time	20		ns
T_{OEP}	OE# to Data# Polling Delay		40	ns
T_{OET}	OE# to Toggle Bit Delay		40	ns
T_{WP}	WE# Pulse Width	100		ns
T_{WPH}	WE# Pulse Width High	100		ns
T_{DS}	Data Setup Time	50		ns
T_{DH}	Data Hold Time	5		ns
T_{IDA}	Software ID Access and Exit Time		150	ns
T_{BP}	Byte Programming Time		20	µs
T_{SE}	Sector-Erase Time		25	ms
T_{BE}	Block-Erase Time		25	ms
T_{SCE}	Chip-Erase Time		100	ms

T25.0 554

Advance Information

TABLE 26: RESET TIMING PARAMETERS, V_{DD}=3.0-3.6V (PP MODE)

Symbol	Parameter	Min	Max	Units
T_{PRST}	V_{DD} stable to Reset Low	1		ms
T_{RSTP}	RST# Pulse Width	100		ns
T_{RSTF}	RST# Low to Output Float		48	ns
T_{RST}[1]	RST# High to Row Address Setup	1		µs
T_{RSTE}	RST# Low to reset during Sector-/Block-Erase or Program		10	µs
T_{RSTC}	RST# Low to reset during Chip-Erase		50	µs

T26.0 554

1. There may be additional reset latency due to T_{RSTE} or T_{RSTC} if a reset procedure is performed during a Program or Erase operation.

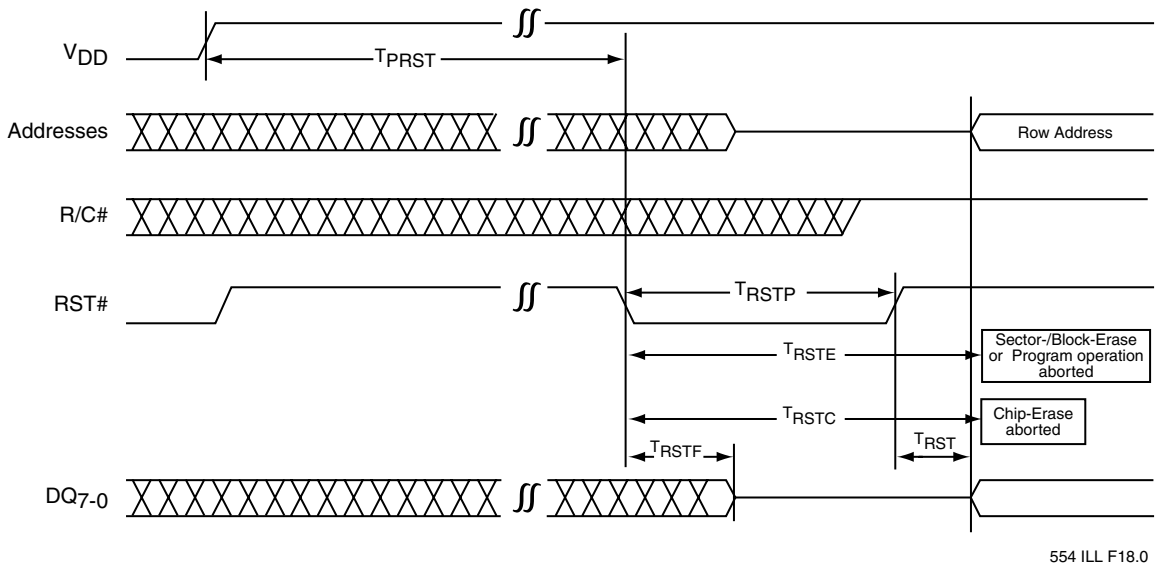


FIGURE 18: RESET TIMING DIAGRAM (PP MODE)

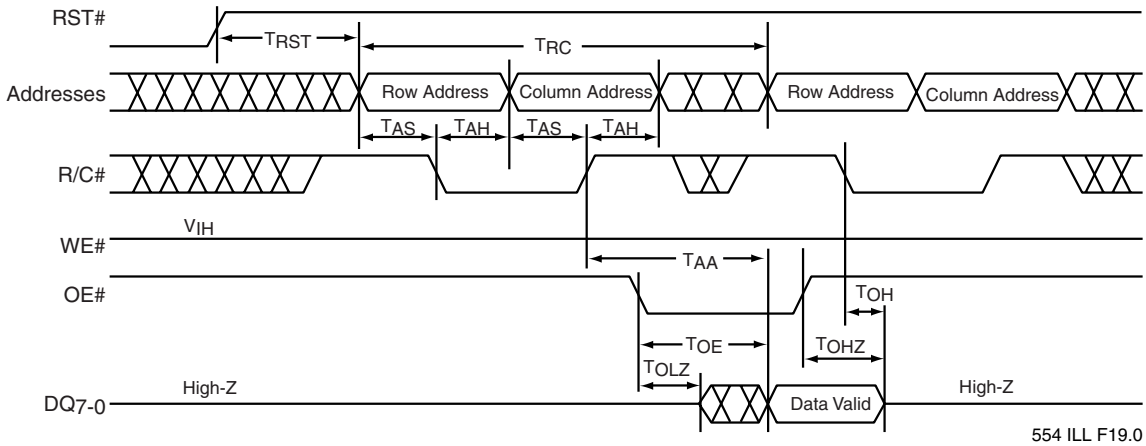


FIGURE 19: READ CYCLE TIMING DIAGRAM (PP MODE)

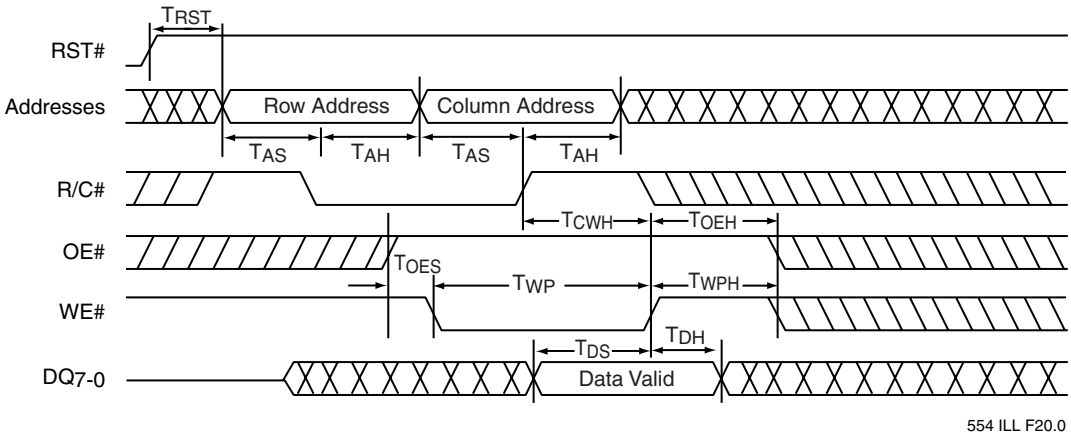


FIGURE 20: WRITE CYCLE TIMING DIAGRAM (PP MODE)

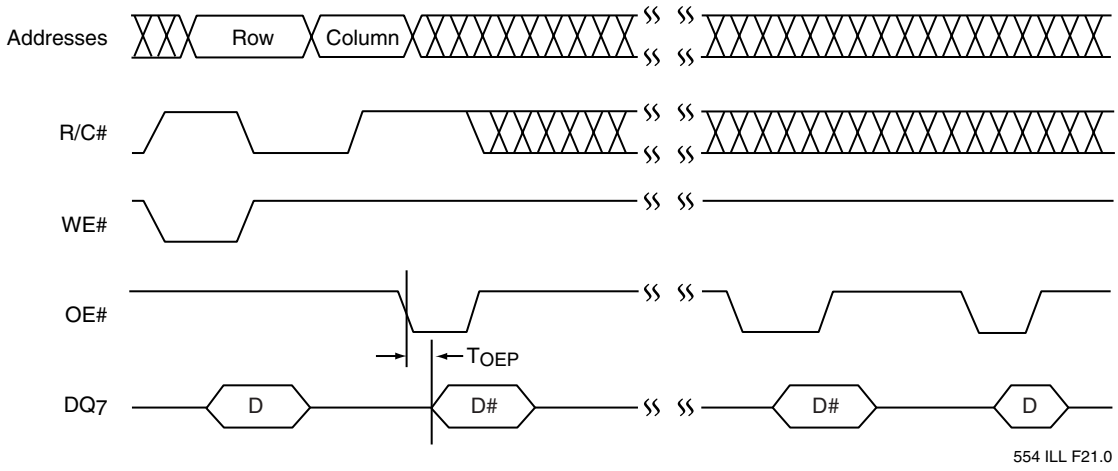


FIGURE 21: DATA# POLLING TIMING DIAGRAM (PP MODE)

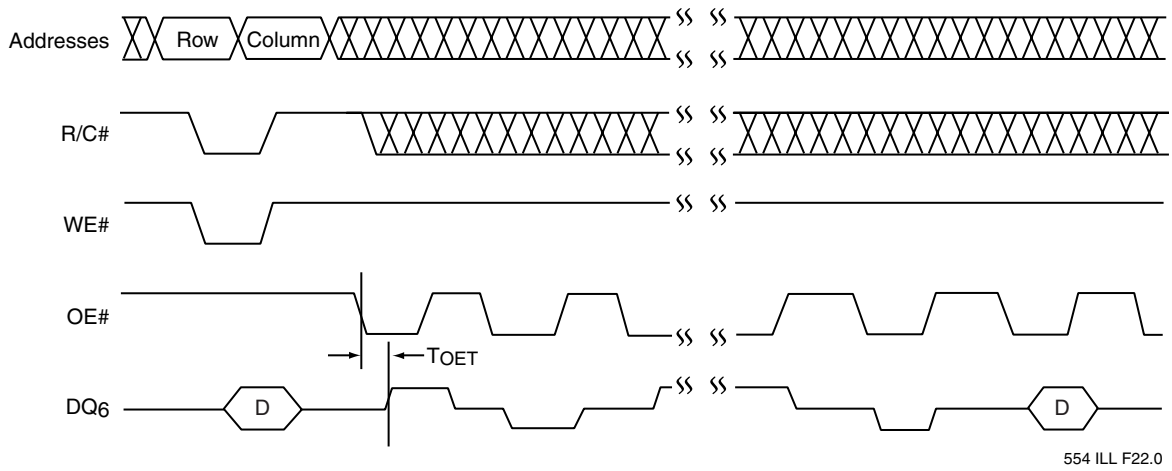


FIGURE 22: TOGGLE BIT TIMING DIAGRAM (PP MODE)

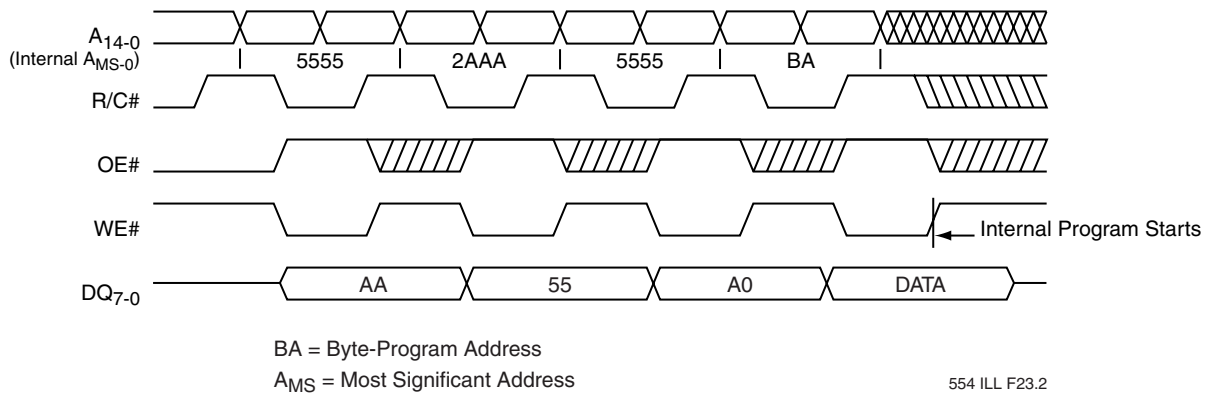


FIGURE 23: BYTE-PROGRAM TIMING DIAGRAM (PP MODE)

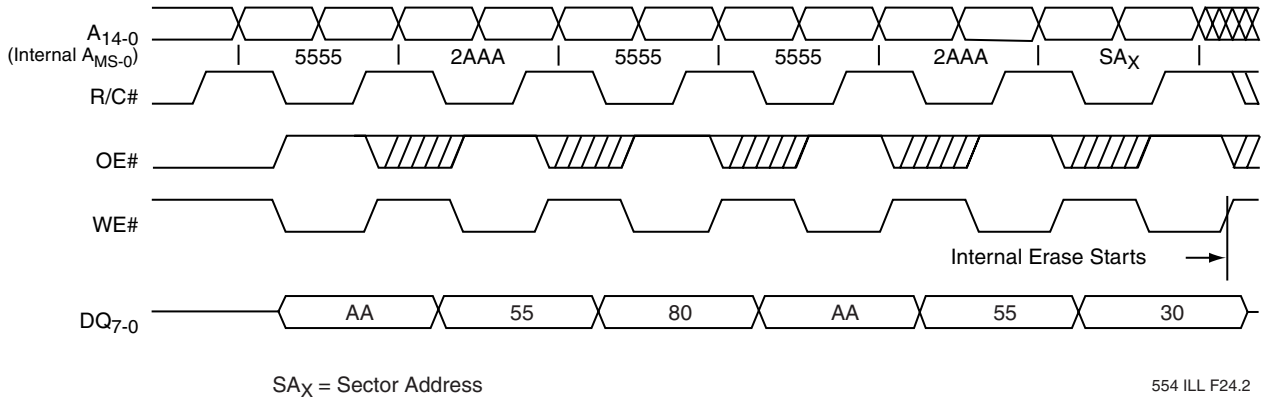


FIGURE 24: SECTOR-ERASE TIMING DIAGRAM (PP MODE)

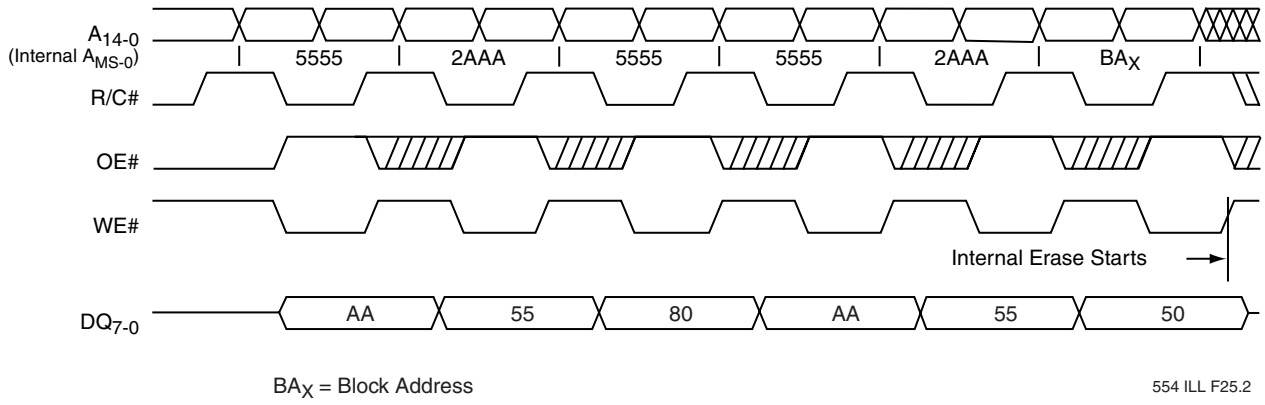


FIGURE 25: BLOCK-ERASE TIMING DIAGRAM (PP MODE)

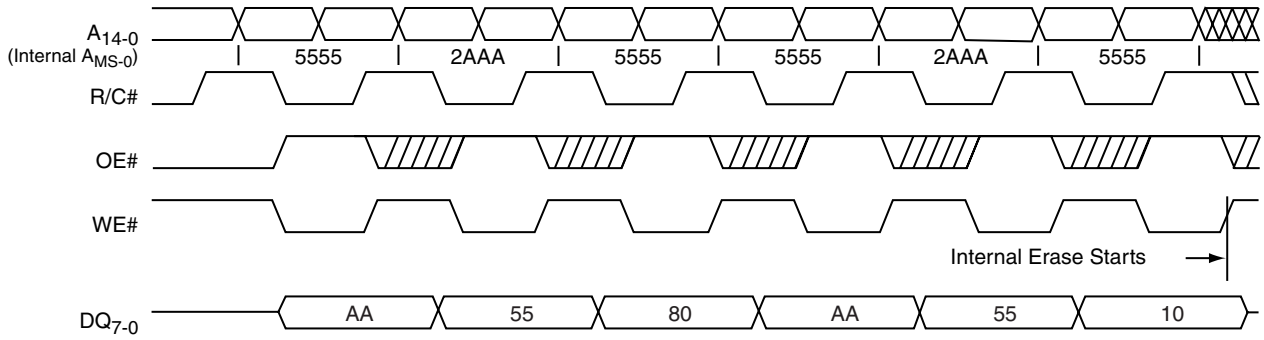


FIGURE 26: CHIP-ERASE TIMING DIAGRAM (PP MODE)

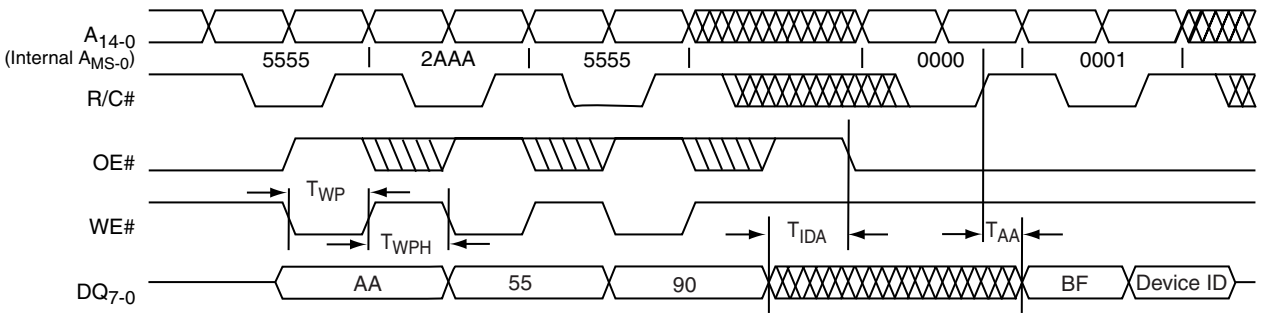


FIGURE 27: SOFTWARE ID ENTRY AND READ (PP MODE)

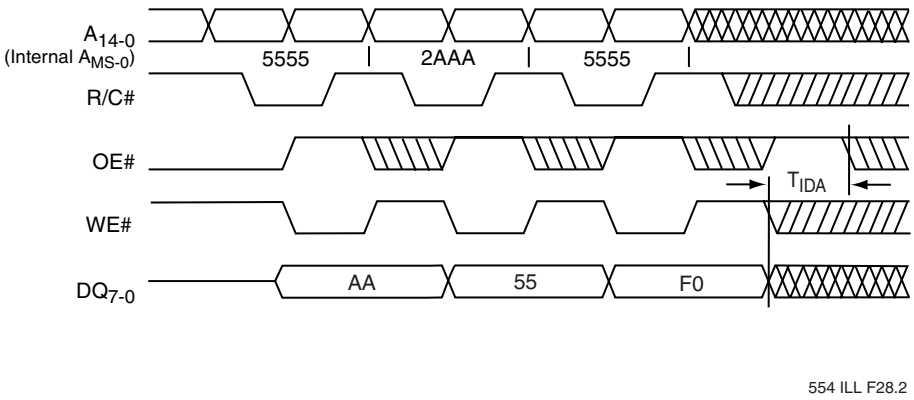
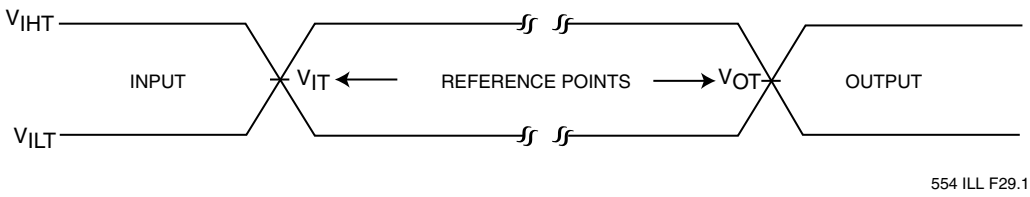


FIGURE 28: SOFTWARE ID EXIT (PP MODE)



AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic "1" and V_{ILT} (0.1 V_{DD}) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} (0.5 V) and V_{OT} (0.5 V_{DD}). Input rise and fall times (10% ↔ 90%) are <5 ns.

Note: V_{IT} - V_{INPUT} Test
V_{OT} - V_{OUTPUT} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

FIGURE 29: AC INPUT/OUTPUT REFERENCE WAVEFORMS

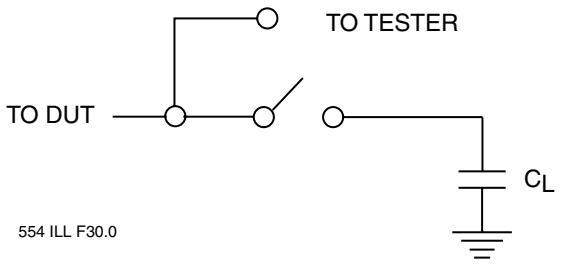


FIGURE 30: A TEST LOAD EXAMPLE

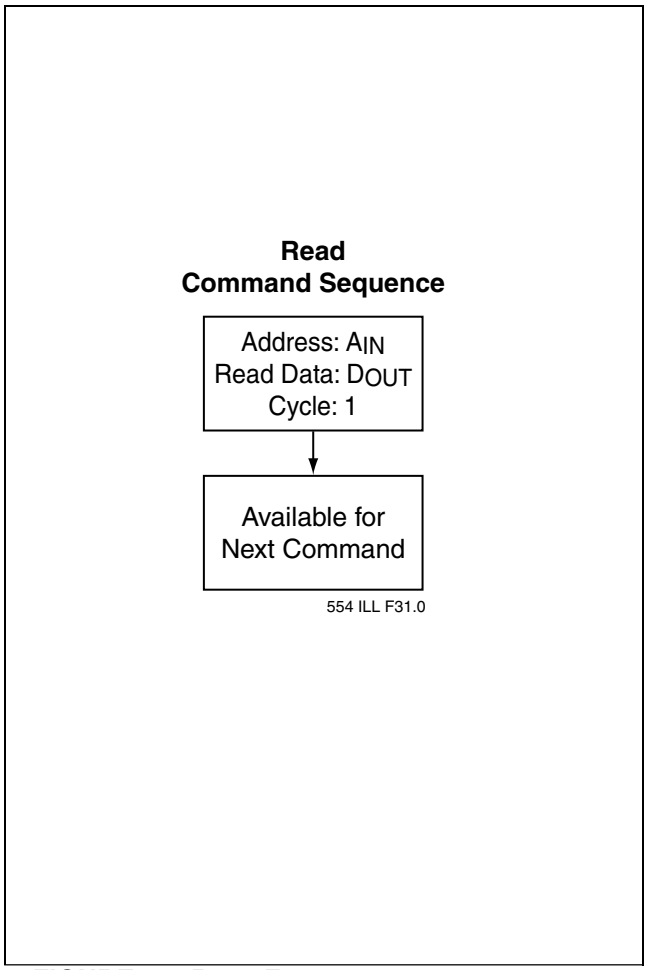


FIGURE 31: READ FLOWCHART (LPC MODE)

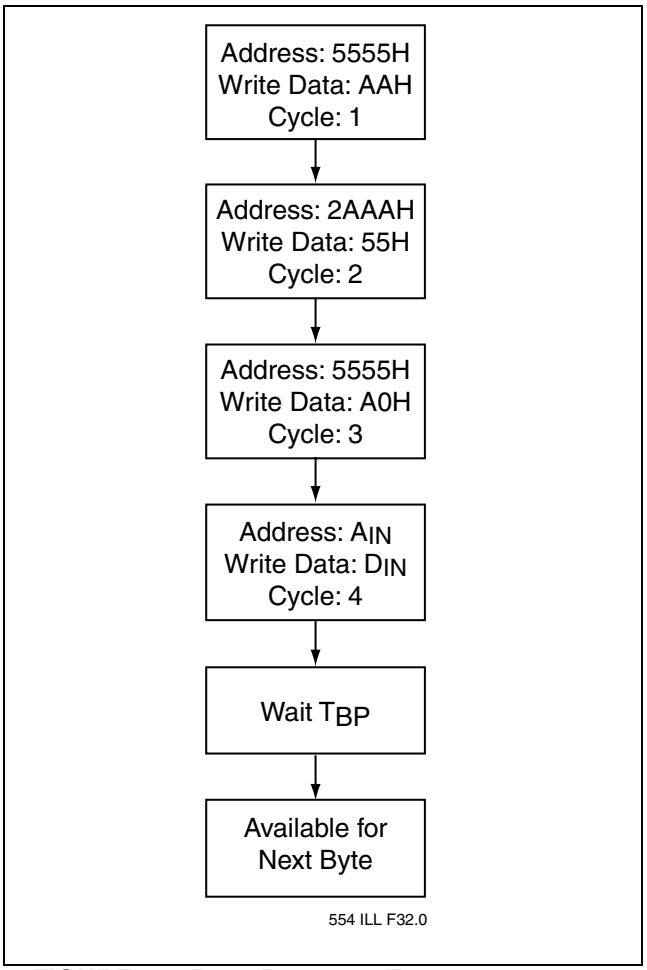


FIGURE 32: BYTE-PROGRAM FLOWCHART (LPC MODE)

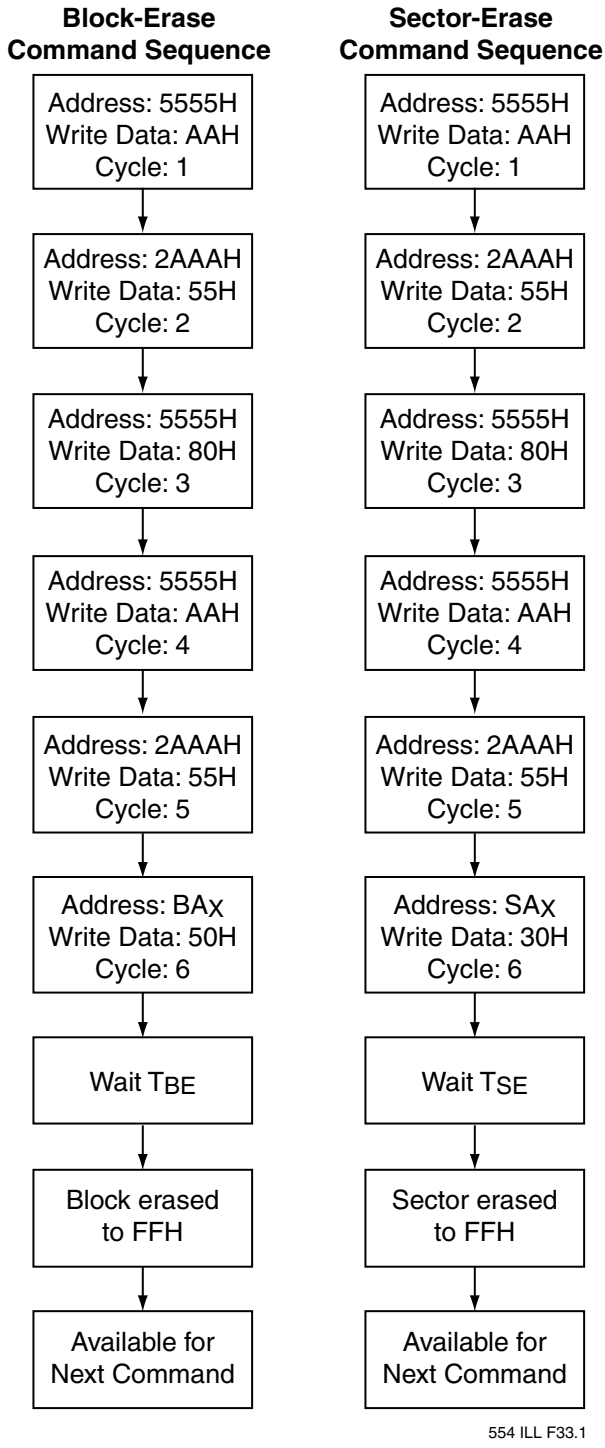


FIGURE 33: ERASE COMMAND SEQUENCES FLOWCHART (LPC MODE)

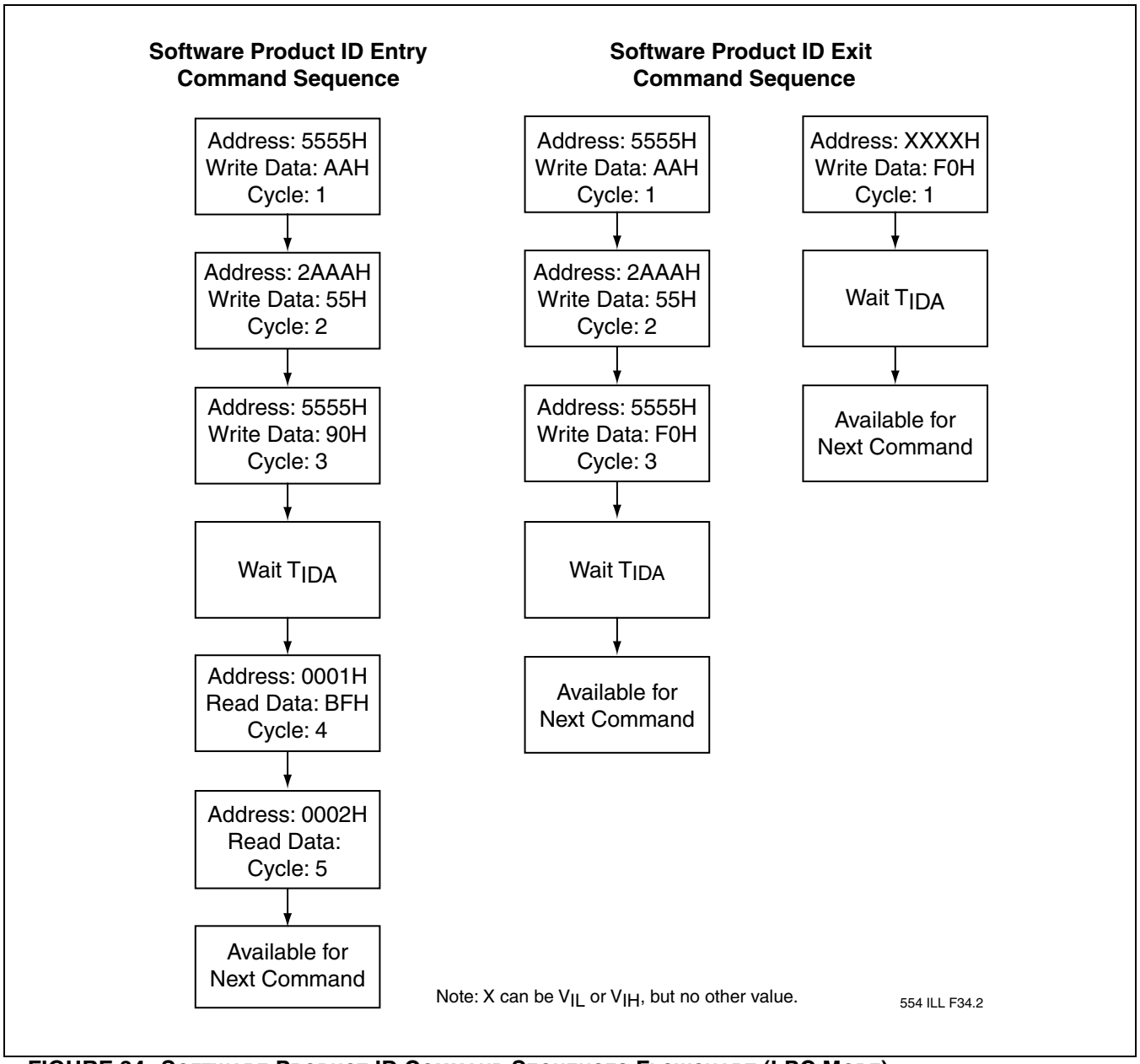


FIGURE 34: SOFTWARE PRODUCT ID COMMAND SEQUENCES FLOWCHART (LPC MODE)

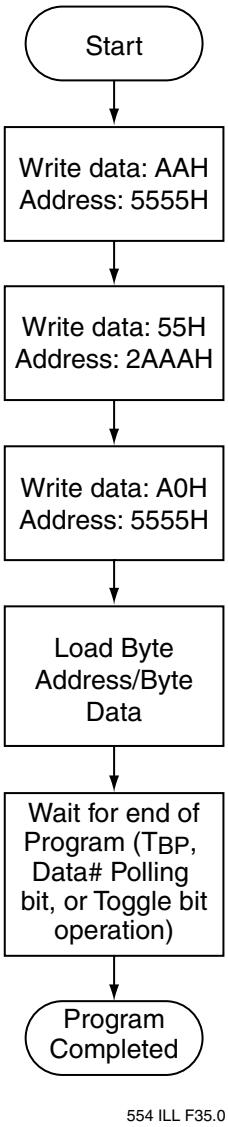


FIGURE 35: BYTE-PROGRAM COMMAND SEQUENCES FLOWCHART (PP MODE)

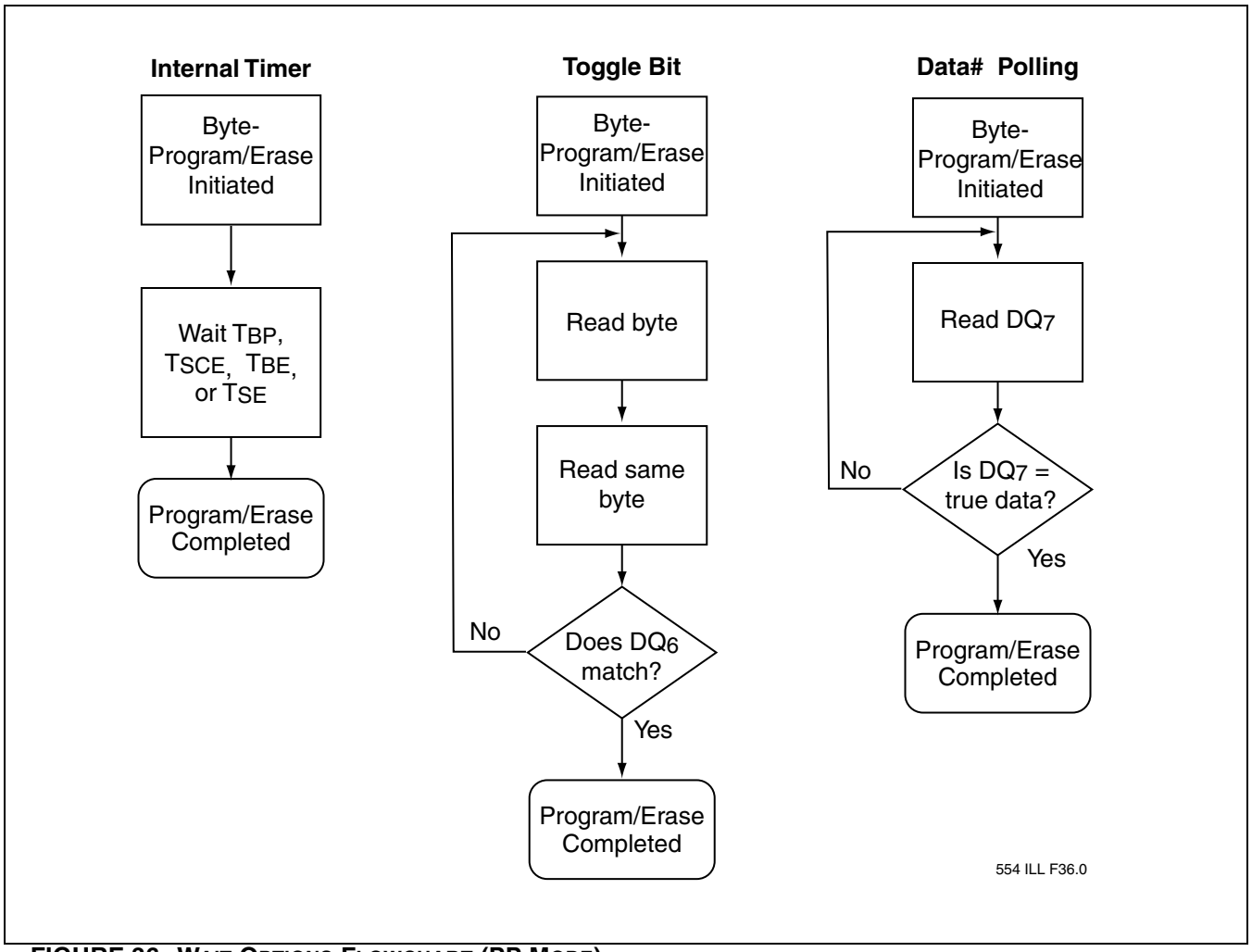


FIGURE 36: WAIT OPTIONS FLOWCHART (PP MODE)

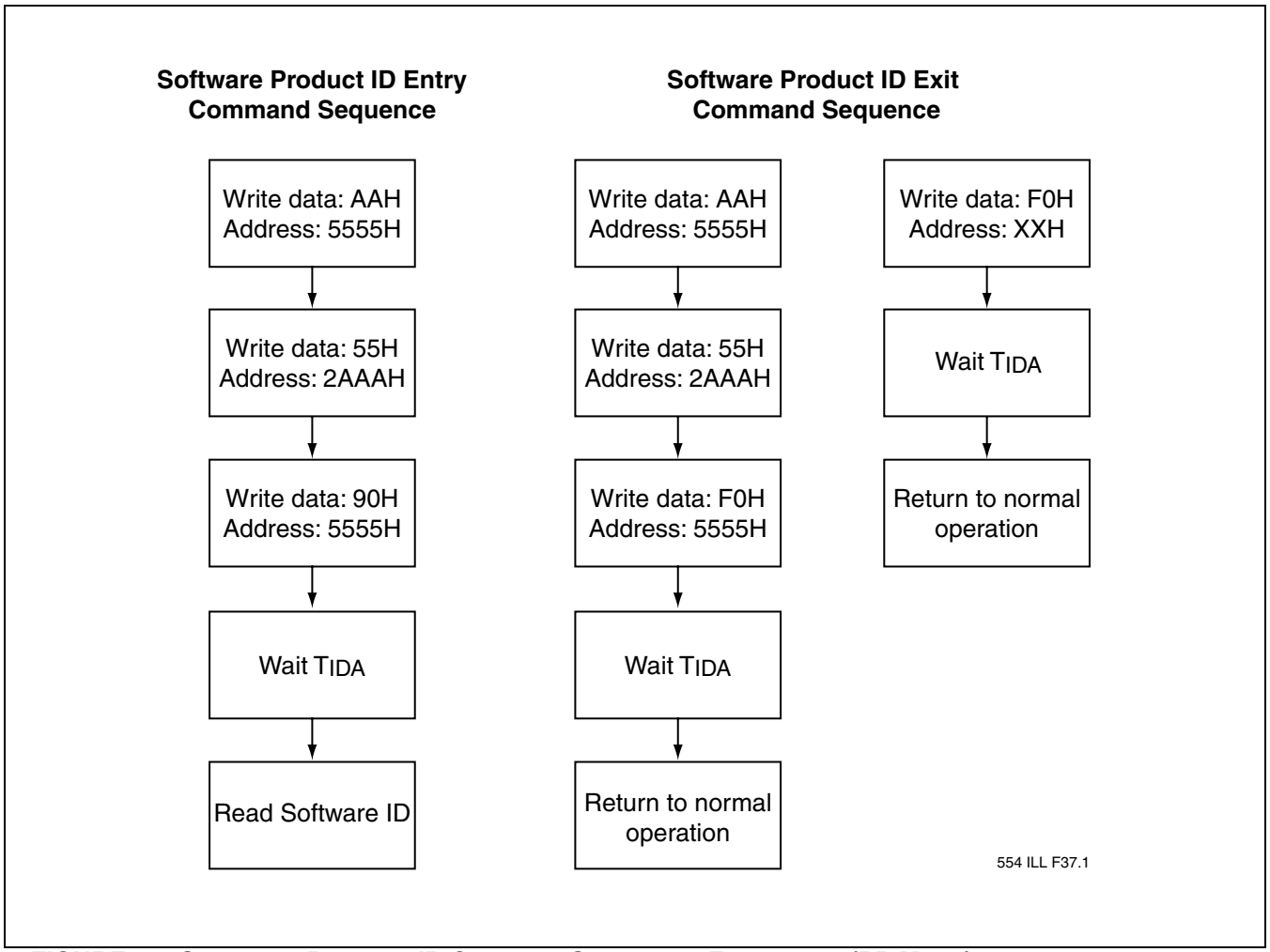


FIGURE 37: SOFTWARE PRODUCT ID COMMAND SEQUENCES FLOWCHART (PP MODE)

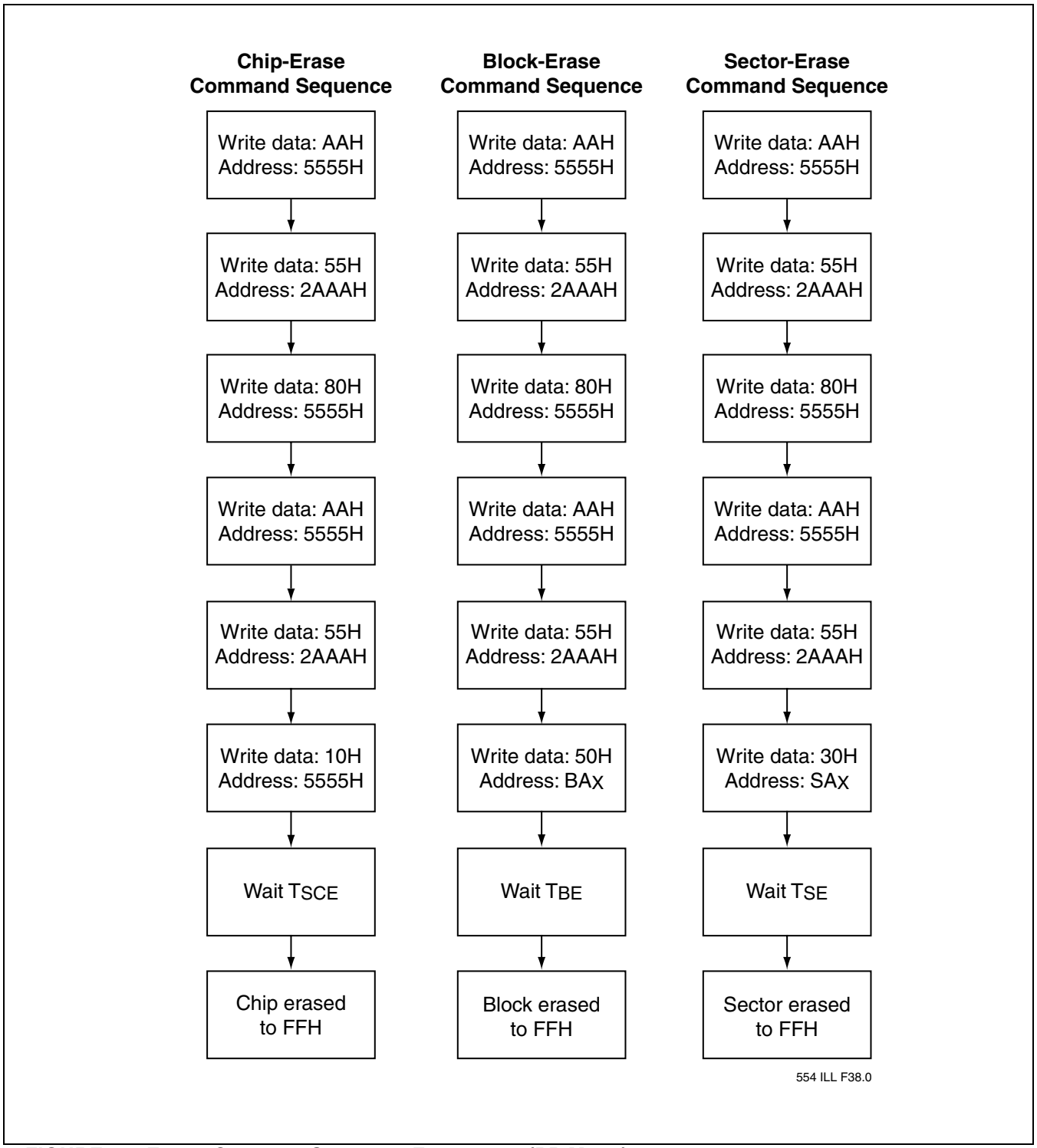
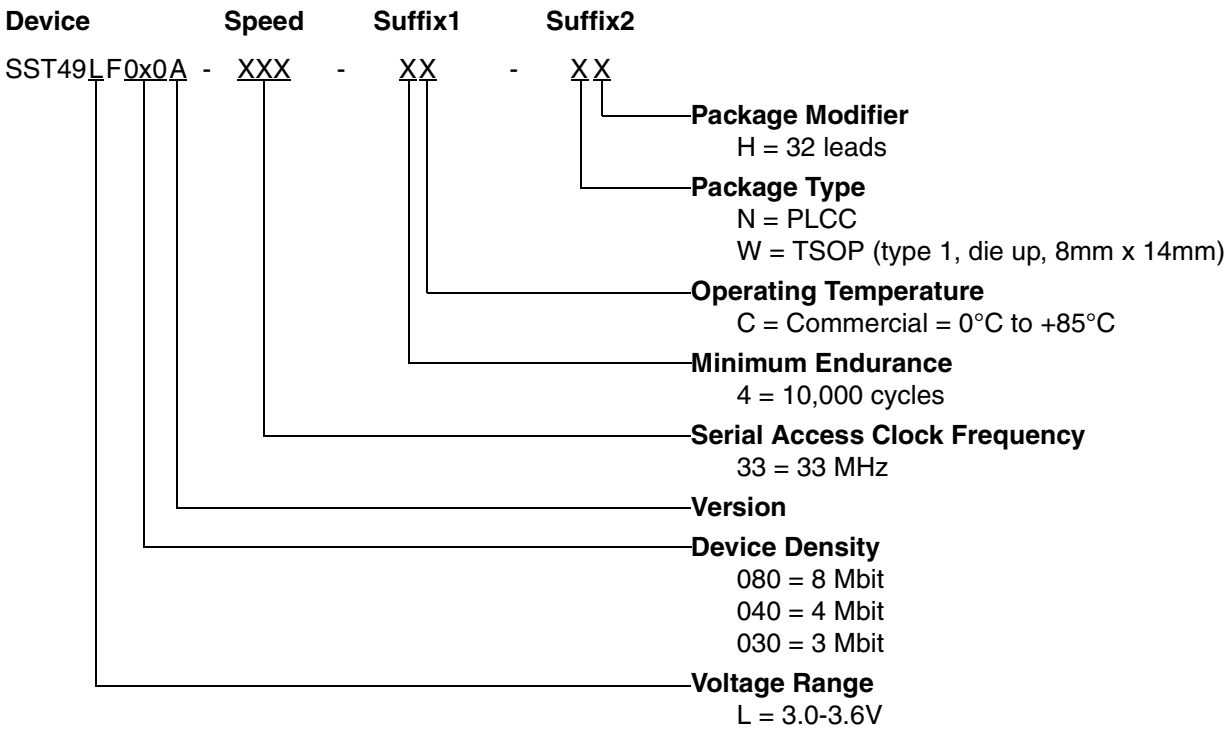


FIGURE 38: ERASE COMMAND SEQUENCE FLOWCHART (PP MODE)

PRODUCT ORDERING INFORMATION



Valid combinations for SST49LF030A

SST49LF030A-33-4C-WH SST49LF030A-33-4C-NH

Valid combinations for SST49LF040A

SST49LF040A-33-4C-WH SST49LF040A-33-4C-NH

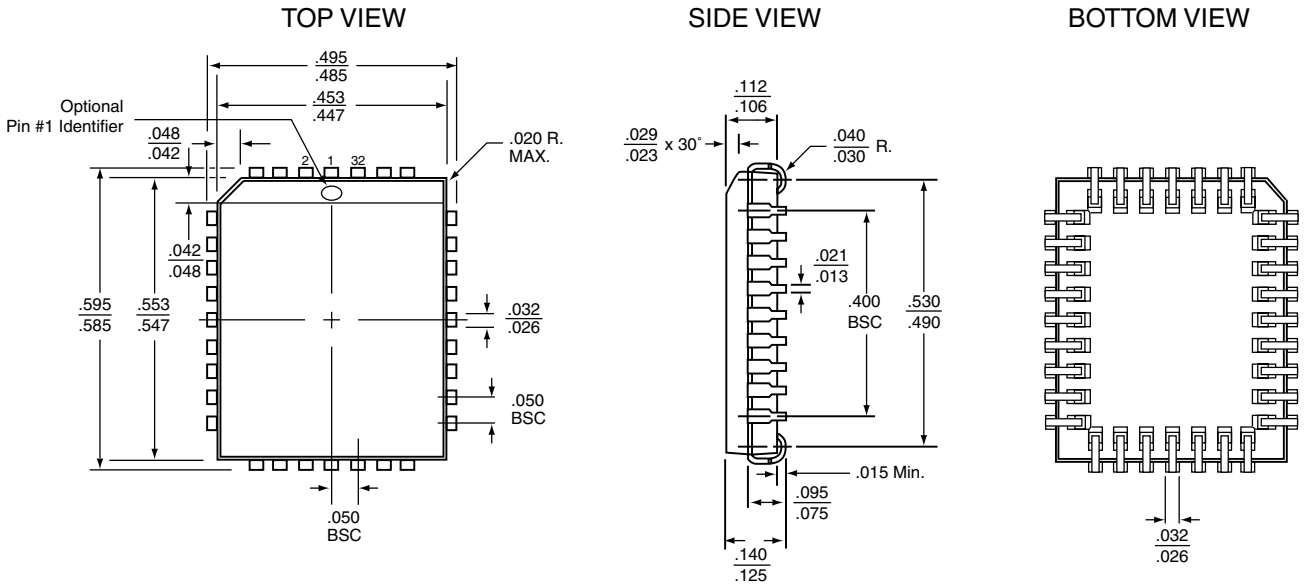
Valid combinations for SST49LF080A

SST49LF080A-33-4C-WH SST49LF080A-33-4C-NH

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Advance Information

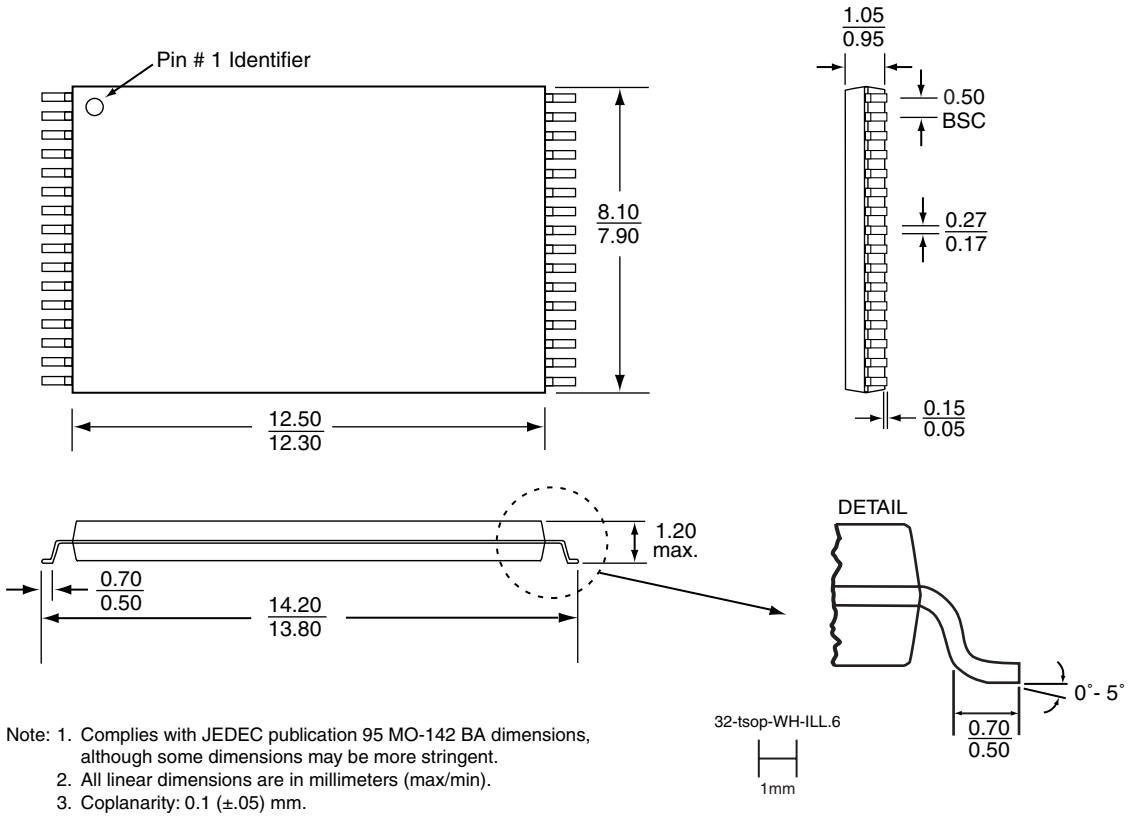
PACKAGING DIAGRAMS



Note: 1. Complies with JEDEC publication 95 MS-016 AE dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (max/min).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.
4. Coplanarity: 4 mils.

32-plcc-NH-ILL.2

32-LEAD PLASTIC LEAD CHIP CARRIER (PLCC)
SST PACKAGE CODE: NH



Note: 1. Complies with JEDEC publication 95 MO-142 BA dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (max/min).
3. Coplanarity: 0.1 (±.05) mm.
4. Maximum allowable mold flash is 0.15 mm at the package ends, and 0.25 mm between leads.

32-LEAD THIN SMALL OUTLINE PACKAGE (TSOP) 8MM X 14MM
SST PACKAGE CODE: WH