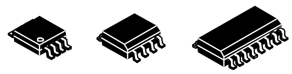


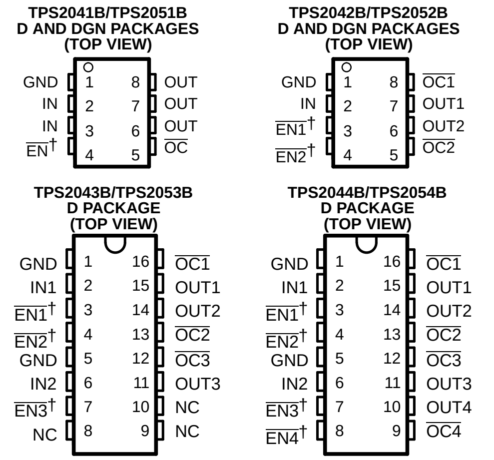
CURRENT-LIMITED, POWER-DISTRIBUTION SWITCHES

FEATURES

- **70-mΩ High-Side MOSFET**
- **500-mA Continuous Current**
- **Thermal and Short-Circuit Protection**
- **Accurate Current Limit (0.7 A min, 1.3 A max)**
- **Operating Range: 2.7 V to 5.5 V**
- **0.6-ms Typical Rise Time**
- **Undervoltage Lockout**
- **Deglitched Fault Report ($\overline{OC}$)**
- **No $\overline{OC}$ Glitch During Power Up**
- **Maximum Standby Supply Current: 1-μA (Single, Dual) or 2-μA (Triple, Quad)**
- **Bidirectional Switch**
- **Ambient Temperature Range: -40°C to 85°C**
- **ESD Protection**
- **UL Pending**

APPLICATIONS

- **Heavy Capacitive Loads**
- **Short-Circuit Protections**



† All enable inputs are active high for the TPS205xB series.
NC − No connect

DESCRIPTION

The TPS204xB/TPS205xB power-distribution switches are intended for applications where heavy capacitive loads and short circuits are likely to be encountered. These devices incorporates 70-mΩ N-channel MOSFET power switches for power-distribution systems that require multiple power switches in a single package. Each switch is controlled by a logic enable input. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the device limits the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ($\overline{OCx}$) logic output low. When continuous heavy overloads and short-circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures that the switch remains off until valid input voltage is present. This power-distribution switch is designed to set current limit at 1 A typically.

GENERAL SWITCH CATALOG

33 mΩ, single TPS201xA 0.2 A − 2 A TPS202x 0.2 A − 2 A TPS203x 0.2 A − 2 A	**80 mΩ, dual** TPS2042B 500 mA TPS2052B 500 mA TPS2046 250 mA TPS2056 250 mA TPS2062 1 A TPS2066 1 A	**80 mΩ, dual** TPS2080 500 mA TPS2081 500 mA TPS2082 500 mA TPS2090 250 mA TPS2091 250 mA TPS2092 250 mA	**80 mΩ, triple** TPS2043B 500 mA TPS2053B 500 mA TPS2047 250 mA TPS2057 250 mA	**80 mΩ, quad** TPS2044B 500 mA TPS2054B 500 mA TPS2048 250 mA TPS2058 250 mA	**80 mΩ, quad** TPS2085 500 mA TPS2086 500 mA TPS2087 500 mA TPS2095 250 mA TPS2096 250 mA TPS2097 250 mA
80 mΩ, single TPS2014 600 mA TPS2015 1 A TPS2041B 500 mA TPS2051B 500 mA TPS2045 250 mA TPS2055 250 mA TPS2061 1 A TPS2065 1 A	**260 mΩ** IN1 IN2 OUT **1.3 Ω** TPS2100/1 IN1 500 mA IN2 10 mA TPS2102/3/4/5 IN1 500 mA IN2 100 mA				

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2004, Texas Instruments Incorporated

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTION AND ORDERING INFORMATION

T_A	ENABLE	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT	TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°c	NUMBER OF SWITCHES	PACKAGED DEVICES(1)	
					MSOP (DGN)	SOIC (D)
-40°C to 85°C	Active low	0.5 A	1 A	Single	TPS2041BDGN	TPS2041BD
	Active high			Single	TPS2051BDGN	TPS2051BD
	Active low			Dual	TPS2042BDGN	TPS2042BD
	Active high			Dual	TPS2052BDGN	TPS2052BD
	Active low			Triple	--	TPS2043BD
	Active high			Triple	--	TPS2053BD
	Active low			Quad	--	TPS2044BD
	Active high			Quad	--	TPS2054BD

(1) The package is available taped and reeled. Add an R suffix to device types (e.g., TPS2042BDR)

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		UNIT
Input voltage range, $V_{I(IN)}$, $V_{I(INx)}$ (2)		-0.3 V to 6 V
Output voltage range, $V_{O(OUT)}$, $V_{O(OUTx)}$ (2)		-0.3 V to 6 V
Input voltage range, $V_{I(/EN)}$, $V_{I(/ENx)}$, $V_{I(EN)}$, $V_{I(ENx)}$		-0.3 V to 6 V
Voltage range, $V_{I(/OC)}$, $V_{I(/OCx)}$		-0.3 V to 6 V
Continuous output current, $I_{O(OUT)}$, $I_{O(OUTx)}$		Internally limited
Continuous total power dissipation		See Dissipation Rating Table
Operating virtual junction temperature range, T_J		-40°C to 125°C
Storage temperature range, T_{stg}		-65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds		260°C
Electrostatic discharge (ESD) protection	Human body model MIL-STD-883C	2 kV
	Charge device model (CDM)	500 V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND.

DISSIPATING RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DGN-8	1712.3 mW	17.123 mW/°C	941.78 mW	684.93 mW
D-8	585.82 mW	5.8582 mW/°C	322.20 mW	234.32 mW
D-16	898.47 mW	8.9847 mW	494.15 mW	359.38 mW

RECOMMENDED OPERATING CONDITIONS

	MIN	MAX	UNIT
Input voltage, $V_{I(IN)}$, $V_{I(INx)}$	2.7	5.5	V
Input voltage, $V_{I(/EN)}$, $V_{I(/ENx)}$, $V_{I(EN)}$, $V_{I(ENx)}$	0	5.5	V
Continuous output current, $I_{O(OUT)}$, $I_{O(OUTx)}$	0	1	A
Operating virtual junction temperature, T_J	-40	125	°C

ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_O = 0.5 A, $V_{I(/ENx)}$ = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)			MIN	TYP	MAX	UNIT
POWER SWITCH								
$r_{DS(on)}$	Static drain-source on-state resistance, 5-V operation and 3.3-V operation	$V_{I(IN)}$ = 5 V or 3.3 V,	I_O = 0.5 A	-40°C ≤ T_J ≤ 125°C		70	135	mΩ
	Static drain-source on-state resistance, 2.7-V operation(2)	$V_{I(IN)}$ = 2.7 V,	I_O = 0.5 A	-40°C ≤ T_J ≤ 125°C		75	150	mΩ
t_r(2)	Rise time, output	$V_{I(IN)}$ = 5.5 V	C_L = 1 µF, R_L = 10 Ω	T_J = 25°C		0.6	1.5	ms
		$V_{I(IN)}$ = 2.7 V				0.4	1	
t_f(2)	Fall time, output	$V_{I(IN)}$ = 5.5 V			0.05		0.5	
		$V_{I(IN)}$ = 2.7 V			0.05		0.5	
ENABLE INPUT $\overline{EN}$ AND $\overline{ENx}$								
V_{IH}	High-level input voltage	2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V			2			V
V_{IL}	Low-level input voltage	2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V					0.8	
I_I	Input current	$V_{I(/ENx)}$ = 0 V or 5.5 V			-0.5		0.5	µA
t_{on}(2)	Turnon time	C_L = 100 µF, R_L = 10 Ω					3	ms
t_{off}(2)	Turnoff time	C_L = 100 µF, R_L = 10 Ω					10	
CURRENT LIMIT								
I_{OS}	Short-circuit output current	$V_{I(IN)}$ = 5 V, OUT connected to GND, device enabled into short-circuit			0.7	1.0	1.3	A
SUPPLY CURRENT (TPS2041B, TPS2051B)								
Supply current, low-level output		No load on OUT, $V_{I(/ENx)}$ = 5.5 V, or $V_{I(ENx)}$ = 0 V		T_J = 25°C		0.5	1	µA
				-40°C ≤ T_J ≤ 125°C		0.5	5	
Supply current, high-level output		No load on OUT, $V_{I(/ENx)}$ = 0 V, or $V_{I(ENx)}$ = 5.5 V		T_J = 25°C		43	60	µA
				-40°C ≤ T_J ≤ 125°C		43	70	
Leakage current		OUT connected to ground, $V_{I(/ENx)}$ = 5.5 V, or $V_{I(ENx)}$ = 0 V		-40°C ≤ T_J ≤ 125°C		1		µA
Reverse leakage current		$V_{I(OUTx)}$ = 5.5 V, IN = ground(2)		T_J = 25°C		0		µA
SUPPLY CURRENT (TPS2042B, TPS2052B)								
Supply current, low-level output		No load on OUT, $V_{I(/ENx)}$ = 5.5 V		T_J = 25°C		0.5	1	µA
				-40°C ≤ T_J ≤ 125°C		0.5	5	
Supply current, high-level output		No load on OUT, $V_{I(/ENx)}$ = 0 V		T_J = 25°C		50	70	µA
				-40°C ≤ T_J ≤ 125°C		50	90	
Leakage current		OUT connected to ground, $V_{I(/ENx)}$ = 5.5 V		-40°C ≤ T_J ≤ 125°C		1		µA
Reverse leakage current		$V_{I(OUTx)}$ = 5.5 V, IN = ground(2)		T_J = 25°C		0.2		µA

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
(2) Not tested in production, specified by design.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_O = 0.5 A, $V_{I(/ENx)}$ = 0 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
SUPPLY CURRENT (TPS2043B, TPS2053B)						
Supply current, low-level output	No load on OUT, $V_{I(ENx)}$ = 0 V	T_J = 25°C		0.5	2	μA
		-40°C ≤ T_J ≤ 125°C		0.5	10	
Supply current, high-level output	No load on OUT, $V_{I(ENx)}$ = 5.5 V	T_J = 25°C		65	90	μA
		-40°C ≤ T_J ≤ 125°C		65	110	
Leakage current	OUT connected to ground, $V_{I(ENx)}$ = 0 V	-40°C≤ T_J ≤ 125°C		1		μA
Reverse leakage current	$V_{I(OUTx)}$ = 5.5 V, INx = ground[3]	T_J = 25°C		0.2		μA
SUPPLY CURRENT (TPS2044B, TPS2054B)						
Supply current, low-level output	No load on OUT, $V_{I(/ENx)}$ = 5.5 V, or $V_{I(ENx)}$ = 0 V	T_J = 25°C		0.5	2	μA
		-40°C ≤ T_J ≤ 125°C		0.5	10	
Supply current, high-level output	No load on OUT, $V_{I(/ENx)}$ = 0 V, or $V_{I(ENx)}$ = 5.5 V	T_J = 25°C		75	110	μA
		-40°C ≤ T_J ≤ 125°C		75	140	
Leakage current	OUT connected to ground, $V_{I(/ENx)}$ = 5.5 V, or $V_{I(ENx)}$ = 0 V	-40°C≤ T_J ≤ 125°C		1		μA
Reverse leakage current	$V_{I(OUTx)}$ = 5.5 V, INx = ground[3]	T_J = 25°C		0.2		μA
UNDERVOLTAGE LOCKOUT						
Low-level input voltage, IN, INx			2		2.5	V
Hysteresis, IN, INx	T_J = 25°C			75		mV
OVERCURRENT $\overline{OC}$ and $\overline{OCx}$						
Output low voltage, $V_{OL(/OCx)}$	$I_{O(/OCx)}$ = 5 mA				0.4	V
Off-state current[3]	$V_{O(/OCx)}$ = 5 V or 3.3 V				1	μA
$\overline{OC}$ deglitch[3]	$\overline{OCx}$ assertion or deassertion		4	8	15	ms
THERMAL SHUTDOWN[4]						
Thermal shutdown threshold[3]			135			°C
Recovery from thermal shutdown[3]			125			°C
Hysteresis[3]				10		°C

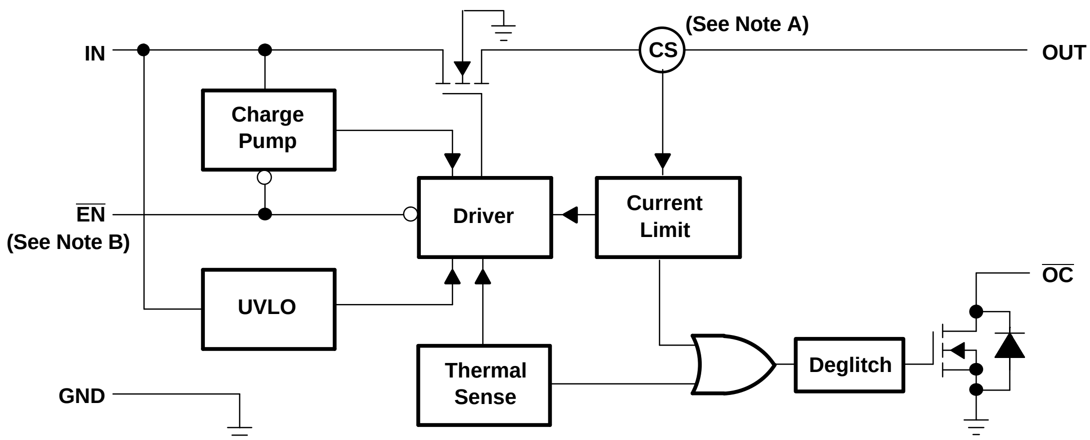
(3) Not tested in production, specified by design.
(4) The thermal shutdown only reacts under overcurrent conditions.

DEVICE INFORMATION

Terminal Functions (TPS2041B and TPS2051B)

TERMINAL			I/O	DESCRIPTION
NAME	TPS2041B	TPS2051B		
$\overline{EN}$	4	-	I	Enable input, logic low turns on power switch
EN	-	4	I	Enable input, logic high turns on power switch
GND	1	1		Ground
IN	2, 3	2, 3	I	Input voltage
$\overline{OC}$	5	5	O	Overcurrent open-drain output, active-low
OUT	6, 7, 8	6, 7, 8	O	Power-switch output

Functional Block Diagram (TPS2041B and TPS2051B)

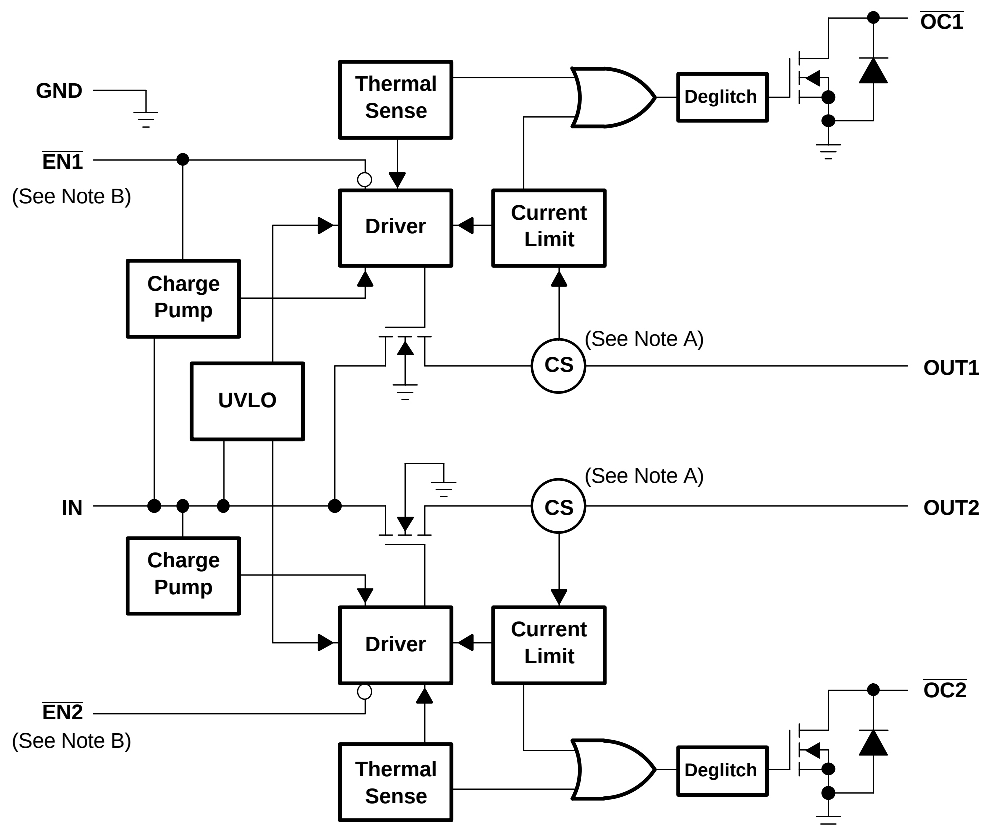


Note A: Current sense
Note B: Active low ($\overline{EN}$) for TPS2041B; Active high (EN) for TPS2051B

Terminal Functions (TPS2042B and TPS2052B)

TERMINAL			I/O	DESCRIPTION
NAME	TPS2042B	TPS2052B		
$\overline{EN1}$	3	-	I	Enable input, logic low turns on power switch IN-OUT1
$\overline{EN2}$	4	-	I	Enable input, logic low turns on power switch IN-OUT2
EN1	-	3	I	Enable input, logic high turns on power switch IN-OUT1
EN2	-	4	I	Enable input, logic high turns on power switch IN-OUT2
GND	1	1		Ground
IN	2	2	I	Input voltage
$\overline{OC1}$	8	8	O	Overcurrent, open-drain output, active low, IN-OUT1
$\overline{OC2}$	5	5	O	Overcurrent, open-drain output, active low, IN-OUT2
OUT1	7	7	O	Power-switch output, IN-OUT1
OUT2	6	6	O	Power-switch output, IN-OUT2

Functional Block Diagram (TPS2042B and TPS2052B)



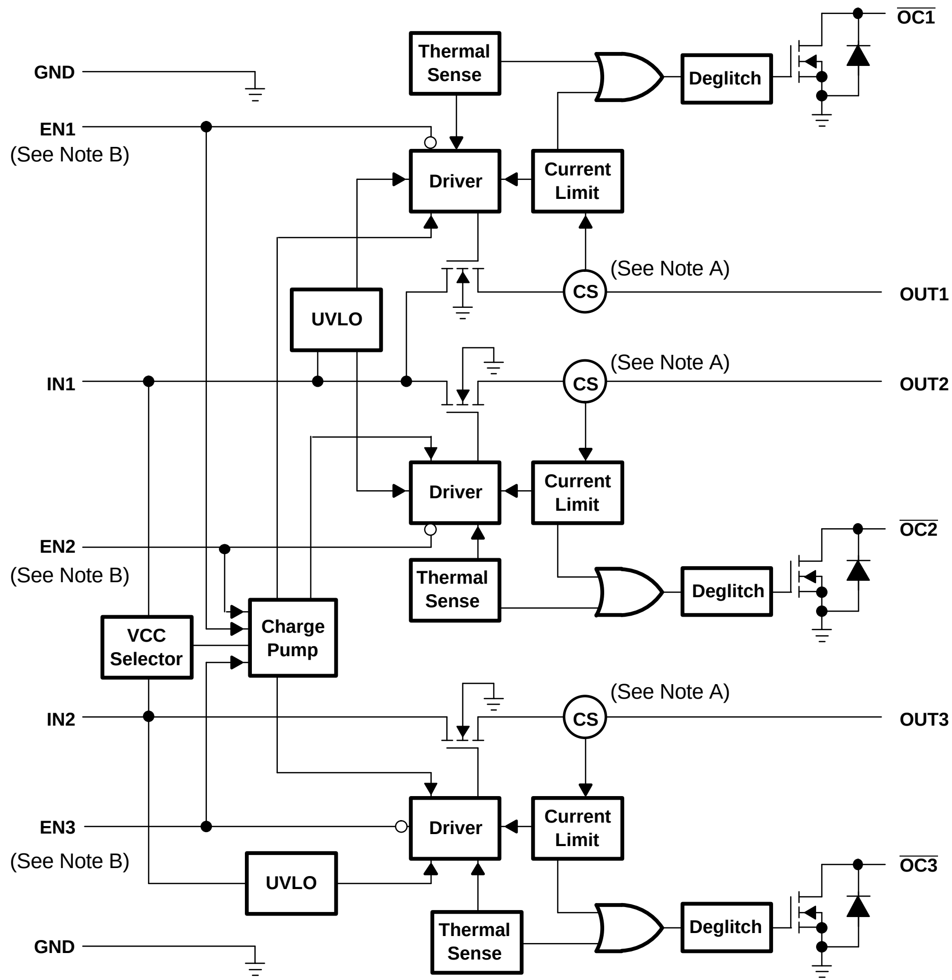
Note A: Current sense

Note B: Active low ($\overline{ENx}$) for TPS2042B; Active high (ENx) for TPS2052B

Terminal Functions (TPS2043B and TPS2053B)

TERMINAL			I/O	DESCRIPTION
NAME	TPS2043B	TPS2053B		
$\overline{EN1}$	3	--	I	Enable input, logic low turns on power switch IN1-OUT1
$\overline{EN2}$	4	--	I	Enable input, logic low turns on power switch IN1-OUT2
$\overline{EN3}$	7	--	I	Enable input, logic low turns on power switch IN2-OUT3
EN1	--	3	I	Enable input, logic high turns on power switch IN1-OUT1
EN2	--	4	I	Enable input, logic high turns on power switch IN1-OUT2
EN3	--	7	I	Enable input, logic high turns on power switch IN2-OUT3
GND	1, 5	1, 5		Ground
IN1	2	2	I	Input voltage for OUT1 and OUT2
IN2	6	6	I	Input voltage for OUT3
NC	8, 9, 10	8, 9, 10		No connection
$\overline{OC1}$	16	16	O	Overcurrent, open-drain output, active low, IN1-OUT1
$\overline{OC2}$	13	13	O	Overcurrent, open-drain output, active low, IN1-OUT2
$\overline{OC3}$	12	12	O	Overcurrent, open-drain output, active low, IN2-OUT3
OUT1	15	15	O	Power-switch output, IN1-OUT1
OUT2	14	14	O	Power-switch output, IN1-OUT2
OUT3	11	11	O	Power-switch output, IN2-OUT3

Functional Block Diagram (TPS2043B and TPS2053B)



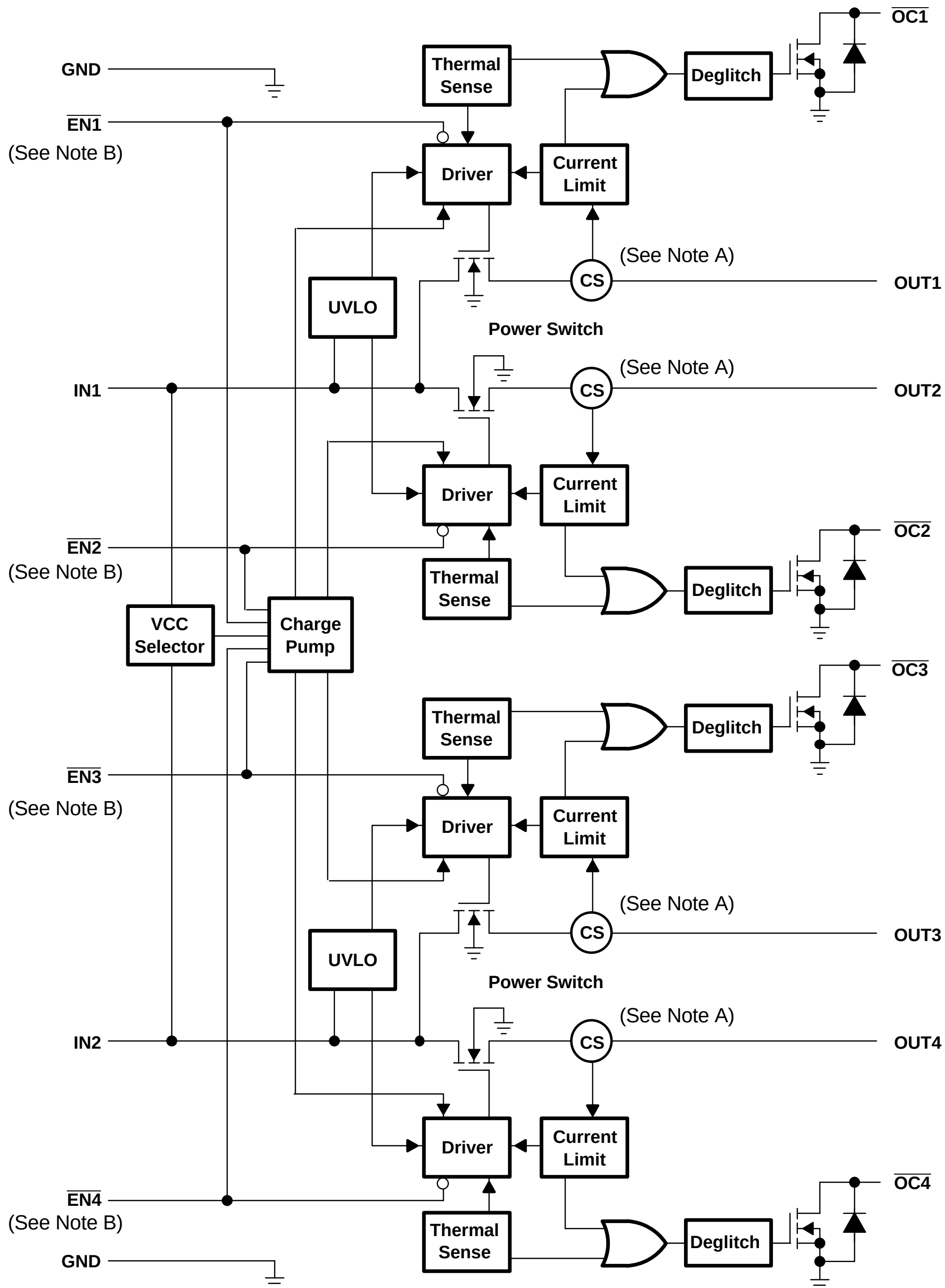
Note A: Current sense

Note B: Active low ($\overline{\text{ENx}}$) for TPS2043B; Active high (ENx) for TPS2053B

Terminal Functions (TPS2044B and TPS2054B)

TERMINAL			I/O	DESCRIPTION
NAME	TPS2044B	TPS2054B		
$\overline{EN1}$	3	-	I	Enable input, logic low turns on power switch IN1-OUT1
$\overline{EN2}$	4	-	I	Enable input, logic low turns on power switch IN1-OUT2
$\overline{EN3}$	7	-	I	Enable input, logic low turns on power switch IN2-OUT3
$\overline{EN4}$	8	-	I	Enable input, logic low turns on power switch IN2-OUT4
EN1	-	3	I	Enable input, logic high turns on power switch IN1-OUT1
EN2	-	4	I	Enable input, logic high turns on power switch IN1-OUT2
EN3	-	7	I	Enable input, logic high turns on power switch IN2-OUT3
EN4	-	8	I	Enable input, logic high turns on power switch IN2-OUT4
GND	1, 5	1, 5		Ground
IN1	2	2	I	Input voltage for OUT1 and OUT2
IN2	6	6	I	Input voltage for OUT3 and OUT4
$\overline{OC1}$	16	16	O	Overcurrent, open-drain output, active low, IN1-OUT1
$\overline{OC2}$	13	13	O	Overcurrent, open-drain output, active low, IN1-OUT2
$\overline{OC3}$	12	12	O	Overcurrent, open-drain output, active low, IN2-OUT3
$\overline{OC4}$	9	9	O	Overcurrent, open-drain output, active low, IN2-OUT4
OUT1	15	15	O	Power-switch output, IN1-OUT1
OUT2	14	14	O	Power-switch output, IN1-OUT2
OUT3	11	11	O	Power-switch output, IN2-OUT3
OUT4	10	10	O	Power-switch output, IN2-OUT4

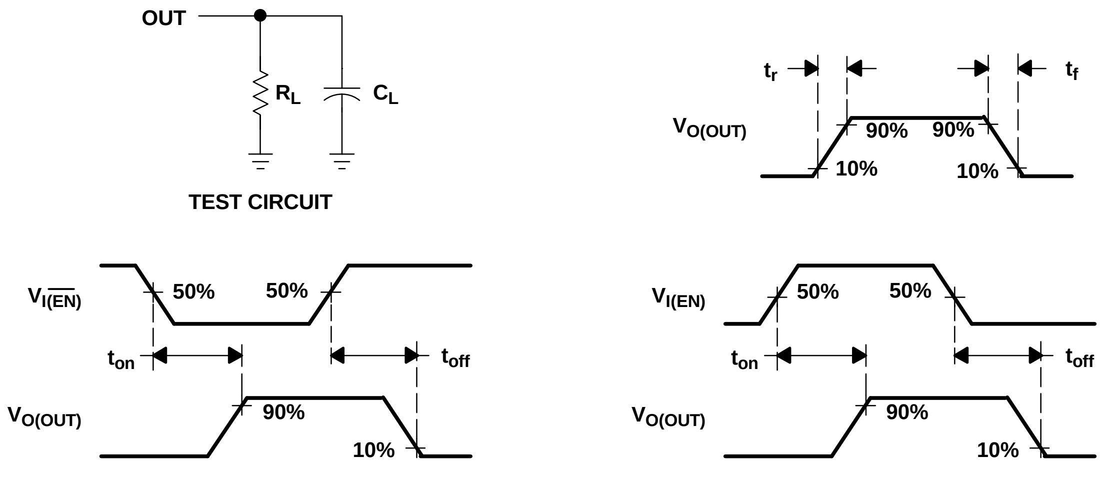
Functional Block Diagram (TPS2044B and TPS2054B)



Note A: Current sense

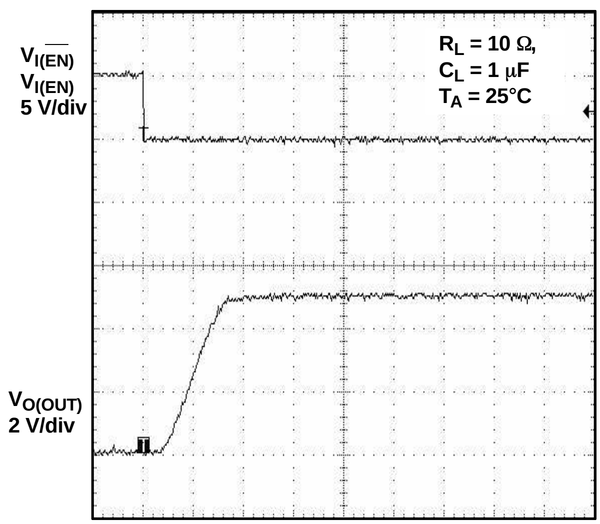
Note B: Active low ($\overline{ENx}$) for TPS2044B; Active high (ENx) for TPS2054B

PARAMETER MEASUREMENT INFORMATION



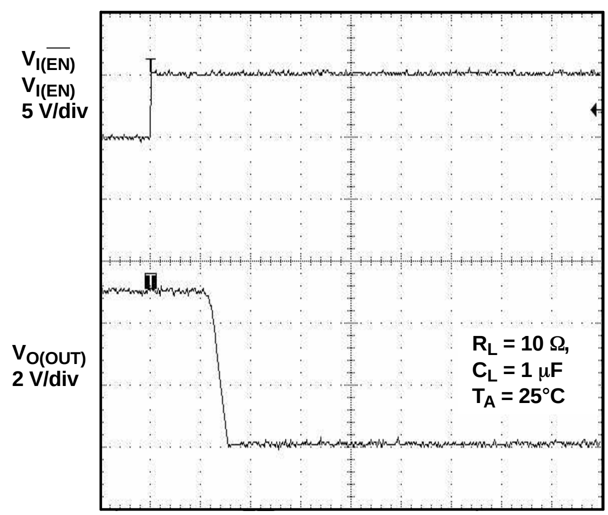
VOLTAGE WAVEFORMS

Figure 1. Test Circuit and Voltage Waveforms



t − Time − 500 μs/div

Figure 2. Turnon Delay and Rise Time With 1-μF Load



t − Time − 500 μs/div

Figure 3. Turnoff Delay and Fall Time With 1-μF Load

PARAMETER MEASUREMENT INFORMATION (continued)

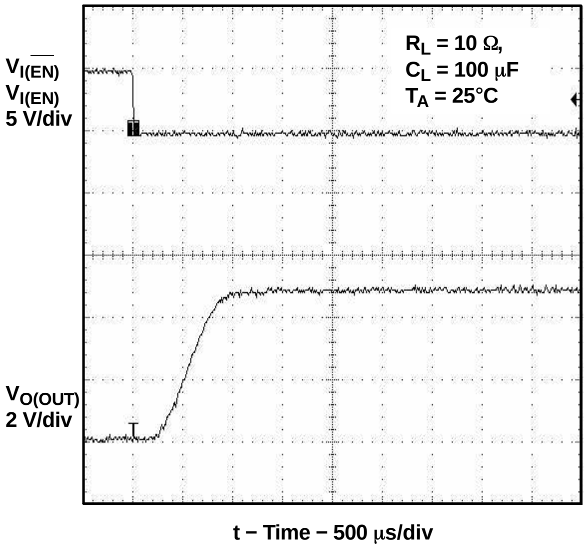


Figure 4. Turnon Delay and Rise Time With 100-µF Load

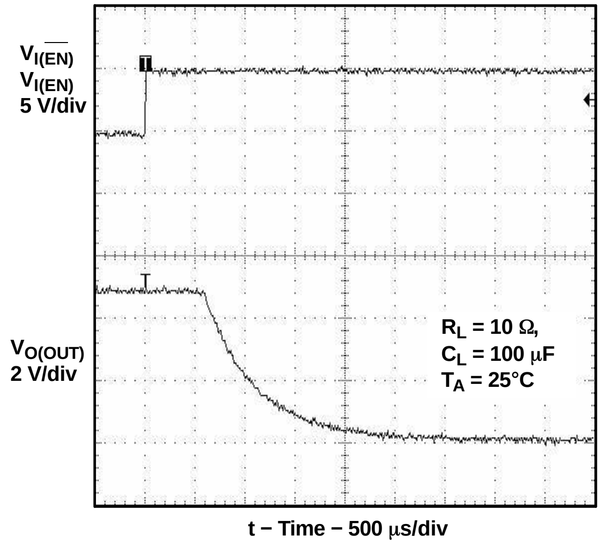


Figure 5. Turnoff Delay and Fall Time With 100-µF Load

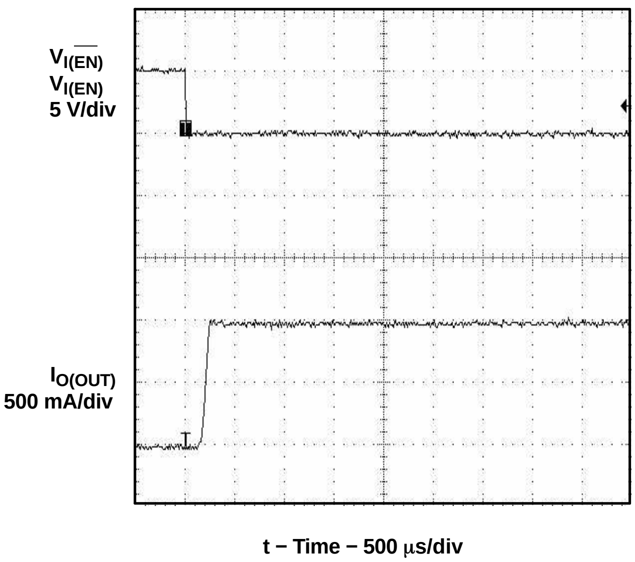


Figure 6. Short-Circuit Current, Device Enabled Into Short

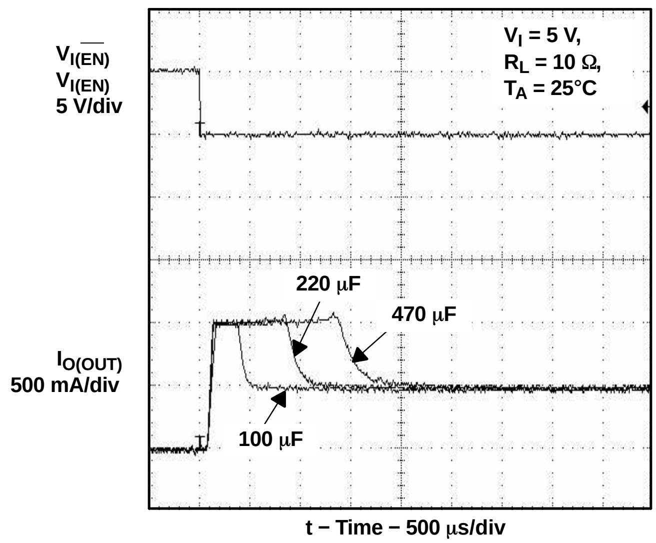


Figure 7. Inrush Current With Different Load Capacitance

PARAMETER MEASUREMENT INFORMATION (continued)

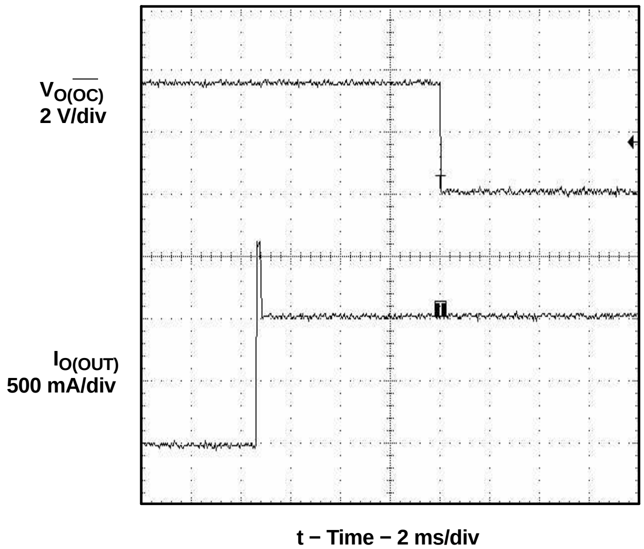


Figure 8. 3-Ω Load Connected to Enabled Device

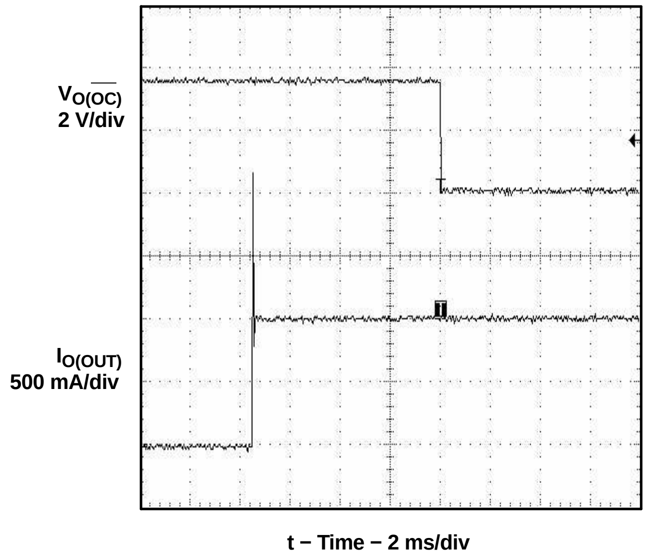


Figure 9. 2-Ω Load Connected to Enabled Device

TYPICAL CHARACTERISTICS

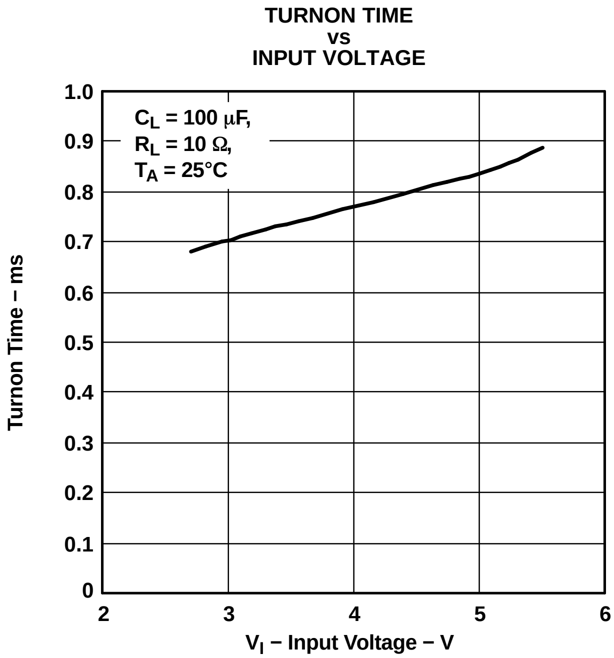


Figure 10.

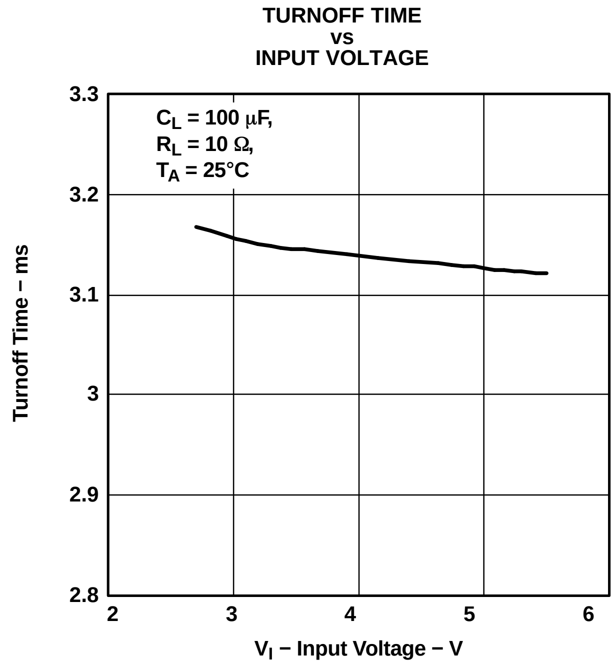


Figure 11.

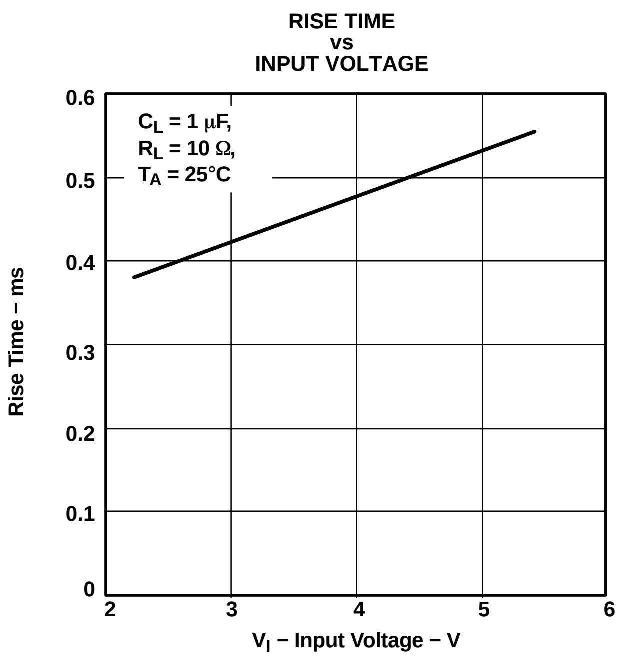


Figure 12.

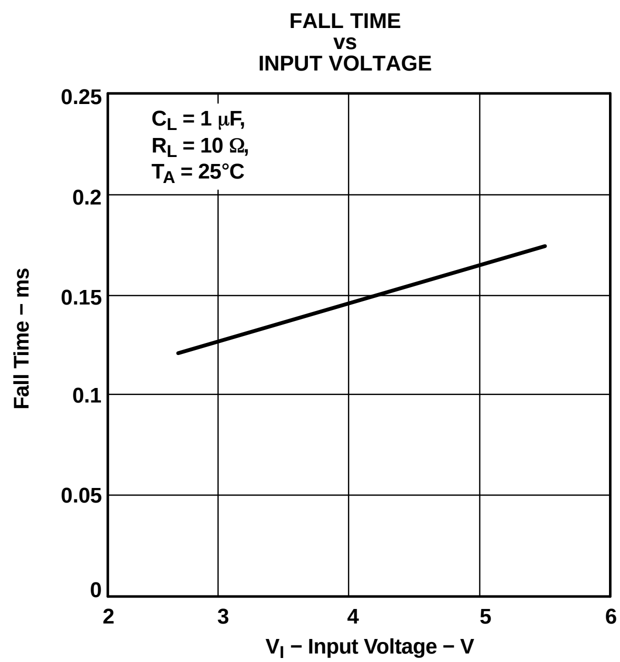


Figure 13.

TYPICAL CHARACTERISTICS (continued)

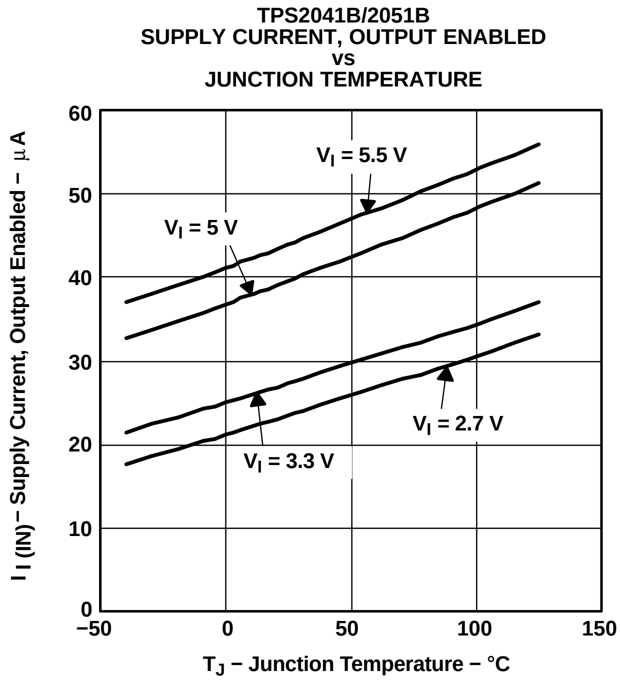


Figure 14.

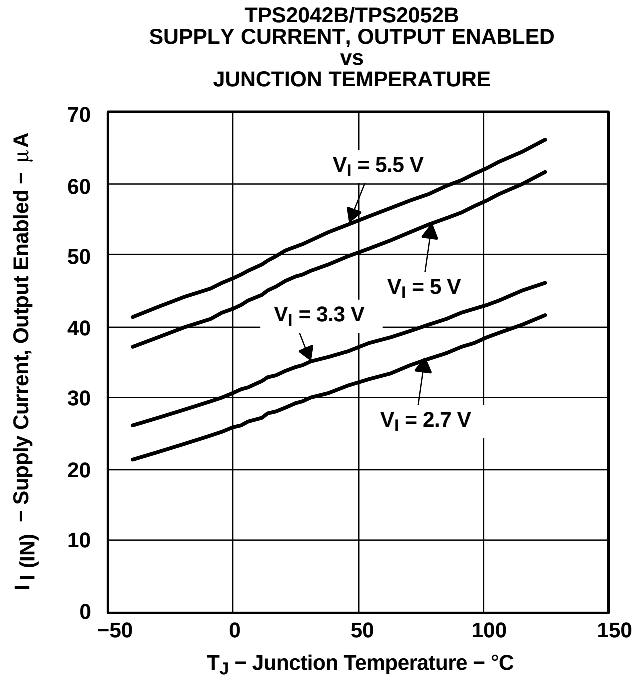


Figure 15.

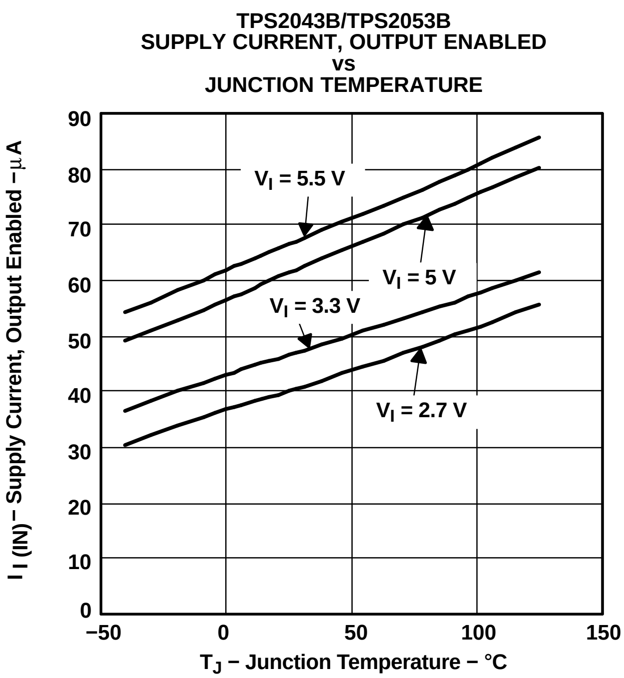


Figure 16.

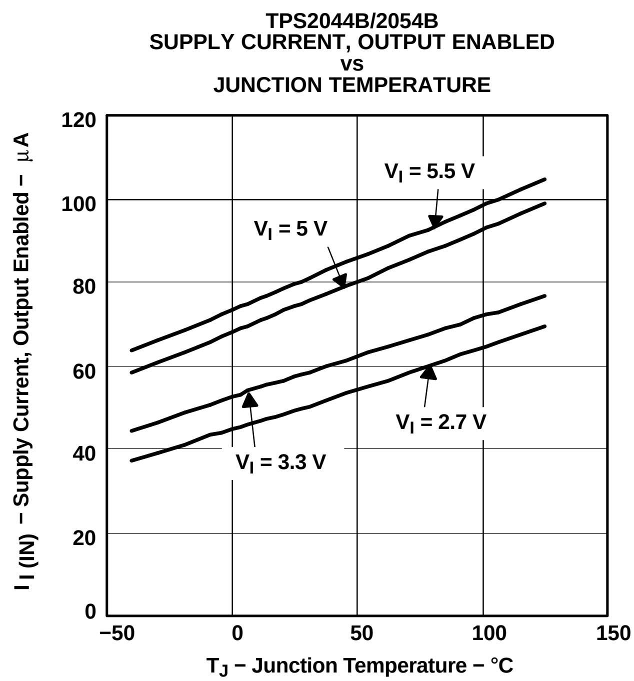


Figure 17.

TYPICAL CHARACTERISTICS (continued)

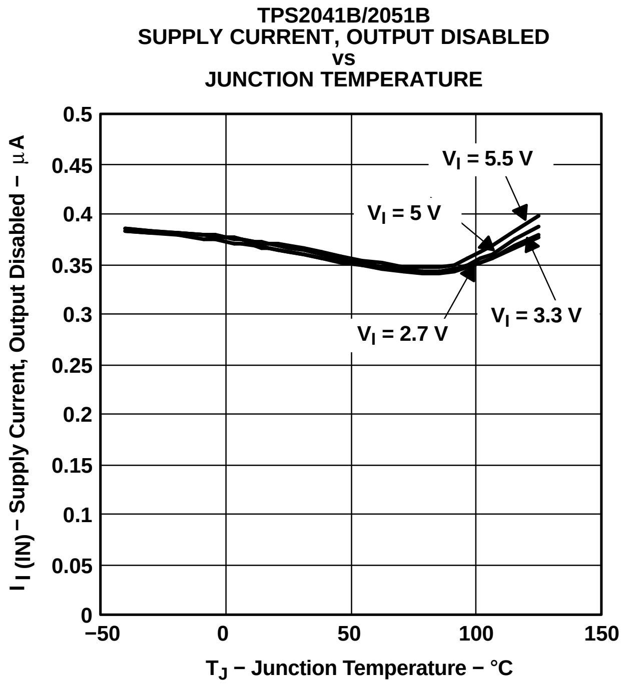


Figure 18.

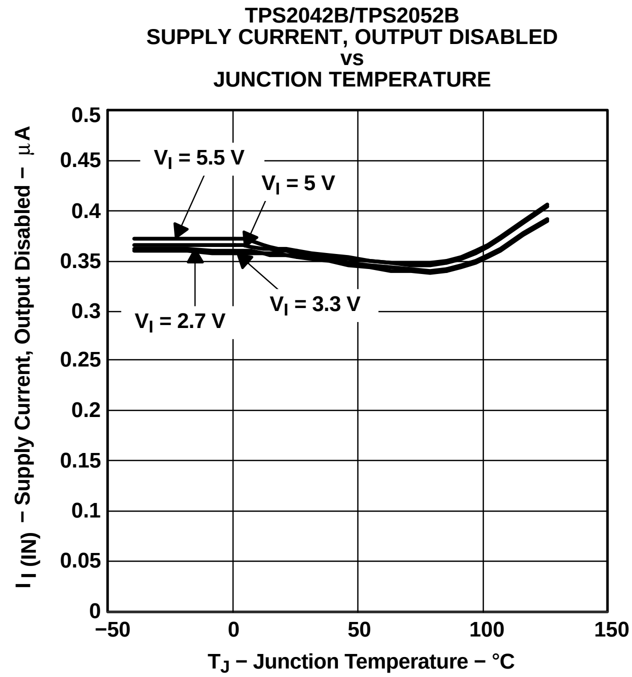


Figure 19.

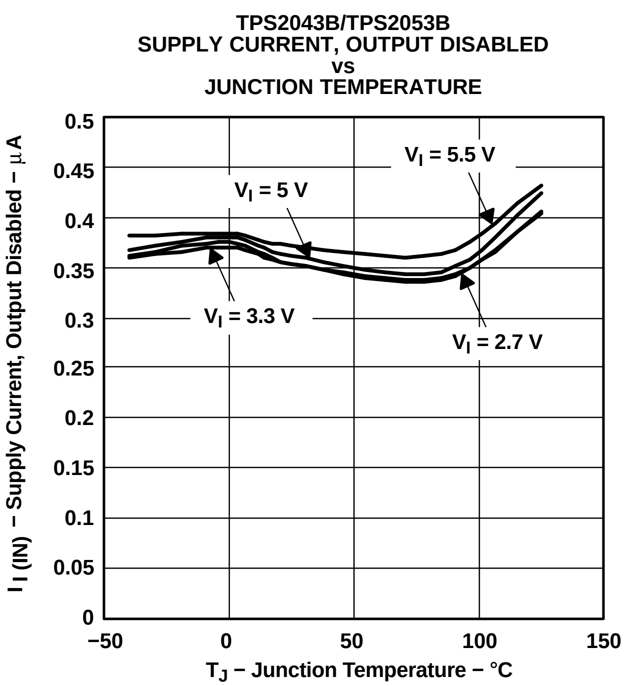


Figure 20.

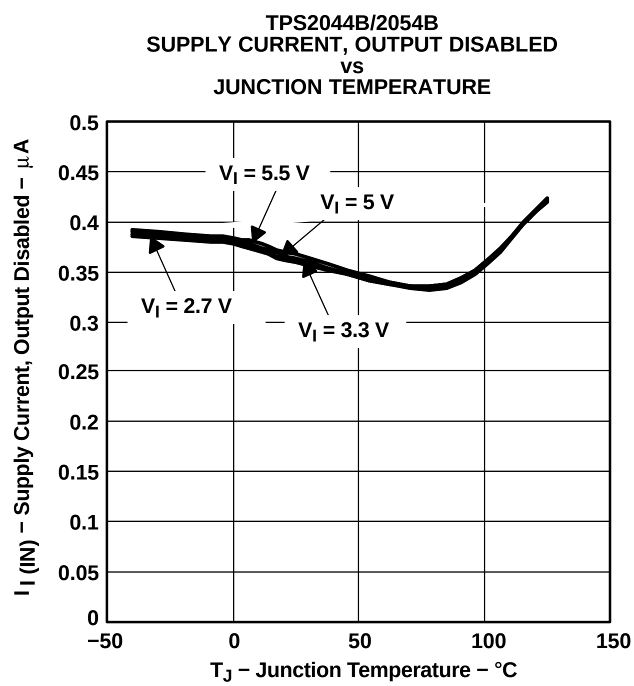


Figure 21.

TYPICAL CHARACTERISTICS (continued)

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

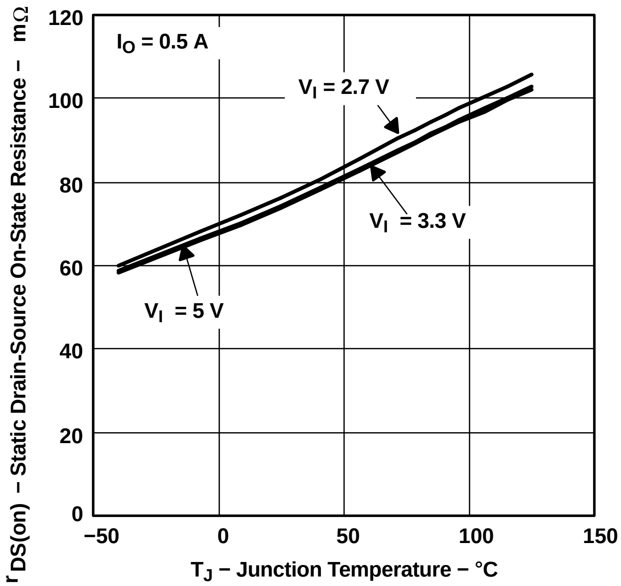


Figure 22.

SHORT-CIRCUIT OUTPUT CURRENT vs JUNCTION TEMPERATURE

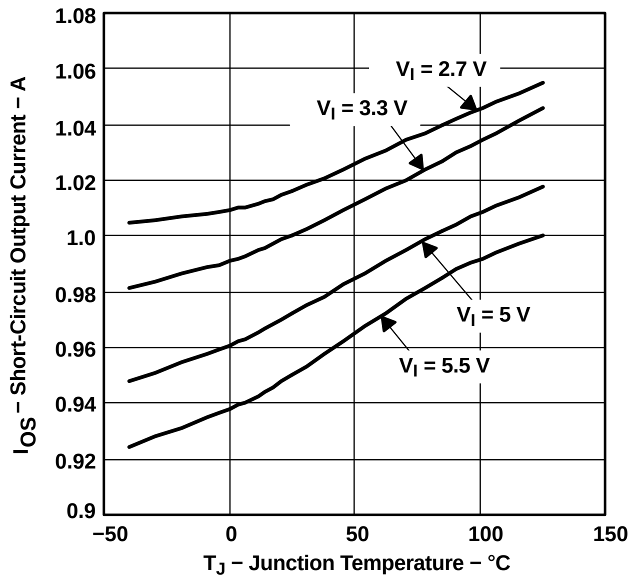


Figure 23.

THRESHOLD TRIP CURRENT vs INPUT VOLTAGE

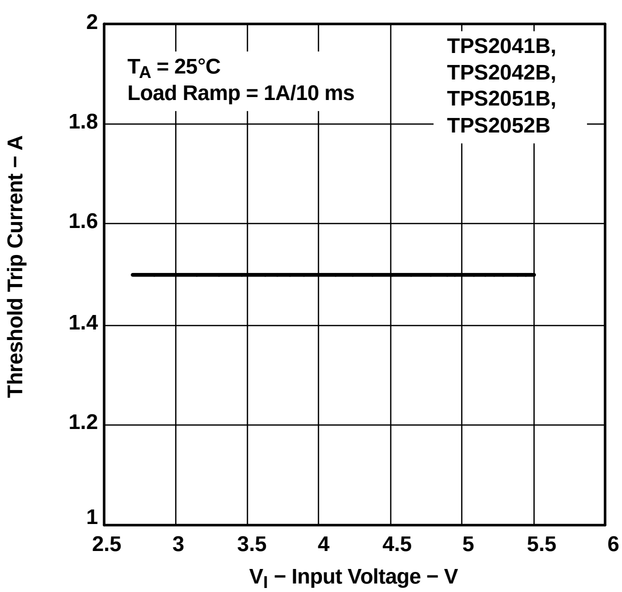


Figure 24.

THRESHOLD TRIP CURRENT vs INPUT VOLTAGE

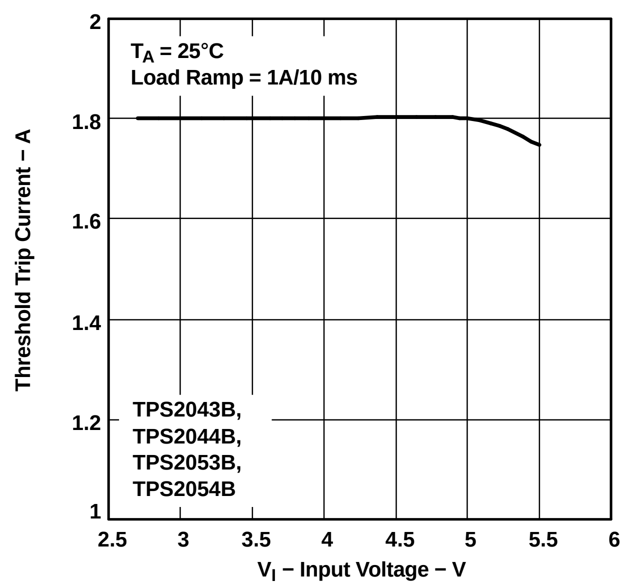


Figure 25.

TEXAS INSTRUMENTS
www.ti.com

TYPICAL CHARACTERISTICS (continued)

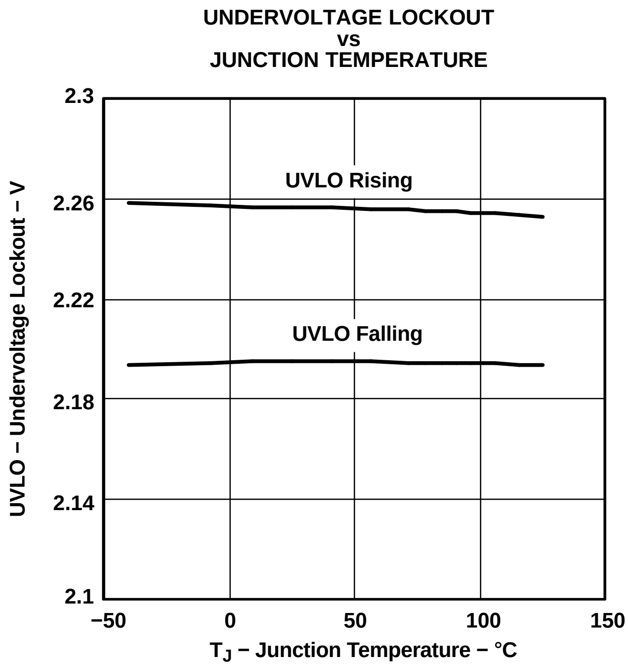


Figure 26.

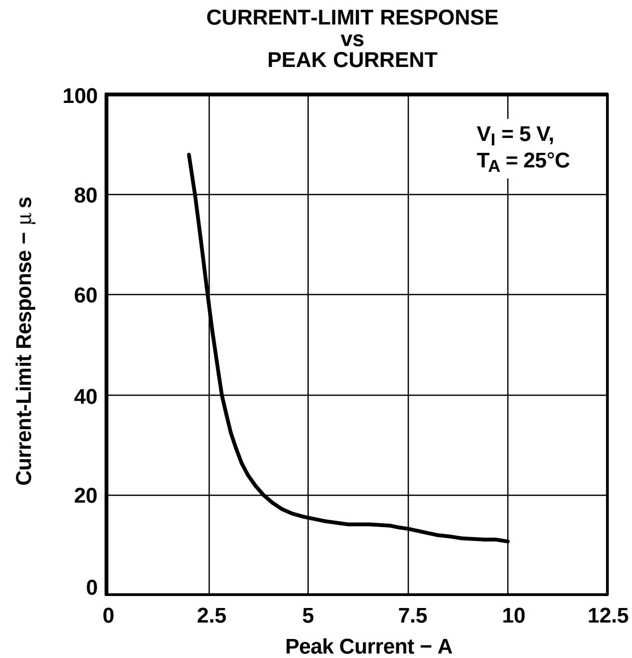


Figure 27.

APPLICATION INFORMATION

POWER-SUPPLY CONSIDERATIONS

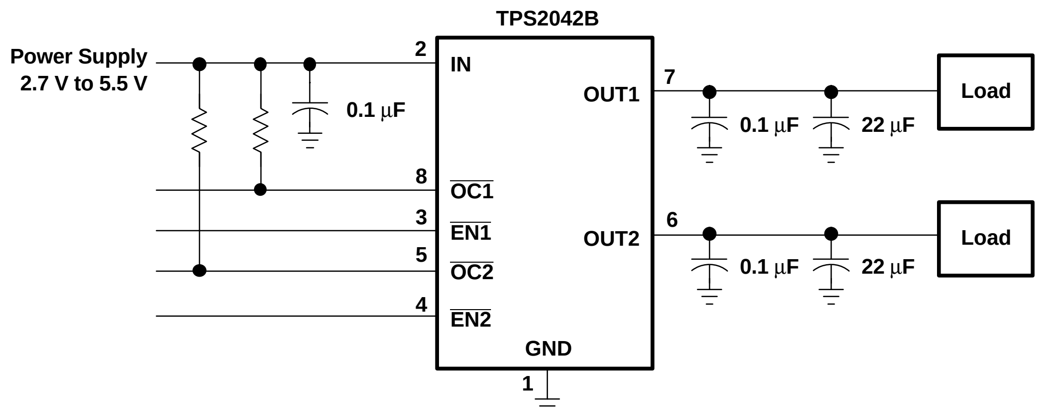


Figure 28. Typical Application (Example, TPS2042B)

A 0.01-µF to 0.1-µF ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-µF to 0.1-µF ceramic capacitor improves the immunity of the device to short-circuit transients.

OVERCURRENT

A sense FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 14 through Figure 17). The TPS204xB/TPS205xB senses the short and immediately switches into a constant-current output.

In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for a short period of time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshold), the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see Figure 18 through Figure 21). The TPS204xB/TPS205xB is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

$\overline{\text{OC}}$ RESPONSE

The $\overline{\text{OCx}}$ open-drain output is asserted (active low) when an overcurrent or overtemperature shutdown condition is encountered after a 10-ms deglitch timeout. The output remains asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause a momentary overcurrent condition; however, no false reporting on $\overline{\text{OCx}}$ occurs due to the 10-ms deglitch circuit. The TPS204xB/TPS205xB is designed to eliminate false overcurrent reporting. The internal overcurrent deglitch eliminates the need for external components to remove unwanted pulses. $\overline{\text{OCx}}$ is not deglitched when the switch is turned off due to an overtemperature shutdown.

APPLICATION INFORMATION (continued)

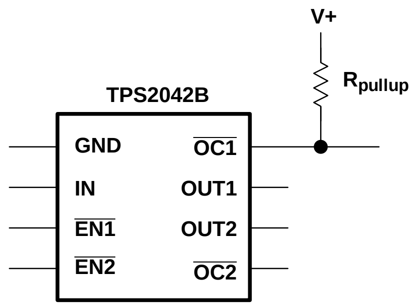


Figure 29. Typical Circuit for the $\overline{OC}$ Pin (Example, TPS2042B)

POWER DISSIPATION AND JUNCTION TEMPERATURE

The low on-resistance on the N-channel MOSFET allows the small surface-mount packages to pass large currents. The thermal resistances of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from Figure 22. Using this value, the power dissipation per switch can be calculated by:

- $P_D = r_{DS(on)} \times I^2$

Multiply this number by the number of switches being used. This step renders the total power dissipation from the N-channel MOSFETs.

Finally, calculate the junction temperature:

- $T_J = P_D \times R_{\Theta JA} + T_A$

Where:

- T_A= Ambient temperature °C
- $R_{\Theta JA}$ = Thermal resistance
- P_D = Total power dissipation based on number of switches being used.

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

THERMAL PROTECTION

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The TPS204xB/TPS205xB implements a thermal sensing to monitor the operating junction temperature of the power distribution switch. In an overcurrent or short-circuit condition, the junction temperature rises due to excessive power dissipation. Once the die temperature rises to approximately 140°C due to overcurrent conditions, the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 10°C, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed. The $\overline{OCx}$ open-drain output is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

UNDERVOLTAGE LOCKOUT (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch is quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO also keeps the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. On reinsertion, the power switch is turned on, with a controlled rise time to reduce EMI and voltage overshoots.

APPLICATION INFORMATION (continued)

UNIVERSAL SERIAL BUS (USB) APPLICATIONS

The universal serial bus (USB) interface is a 12-Mb/s, or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts/self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

Self-powered and bus-powered hubs distribute data and power to downstream functions. The TPS204xB/TPS205xB can provide-power distribution solutions to many of these classes of devices.

HOST/SELF-POWERED AND BUS-POWERED HUBS

Hosts and self-powered hubs have a local power supply that powers the embedded functions and the downstream ports (see Figure 30 and Figure 31). This power supply must provide from 5.25 V to 4.75 V to the board side of the downstream connection under full-load and no-load conditions. Hosts and SPHs are required to have current-limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

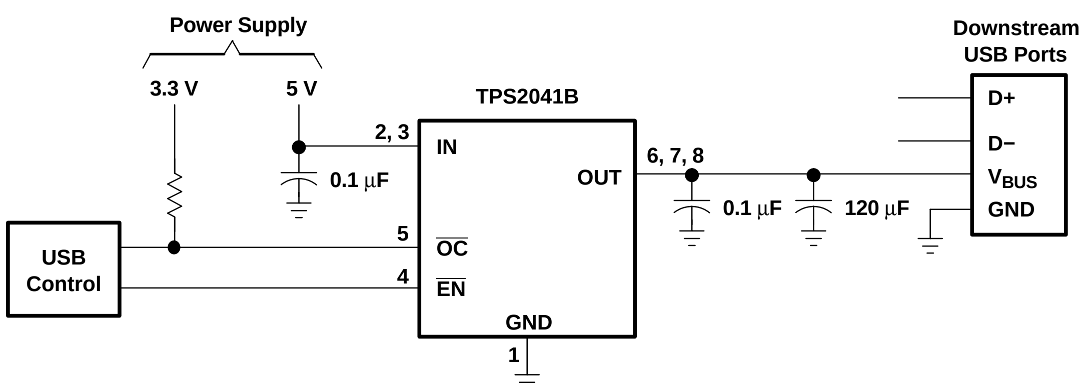


Figure 30. Typical One-Port USB Host / Self-Powered Hub

APPLICATION INFORMATION (continued)

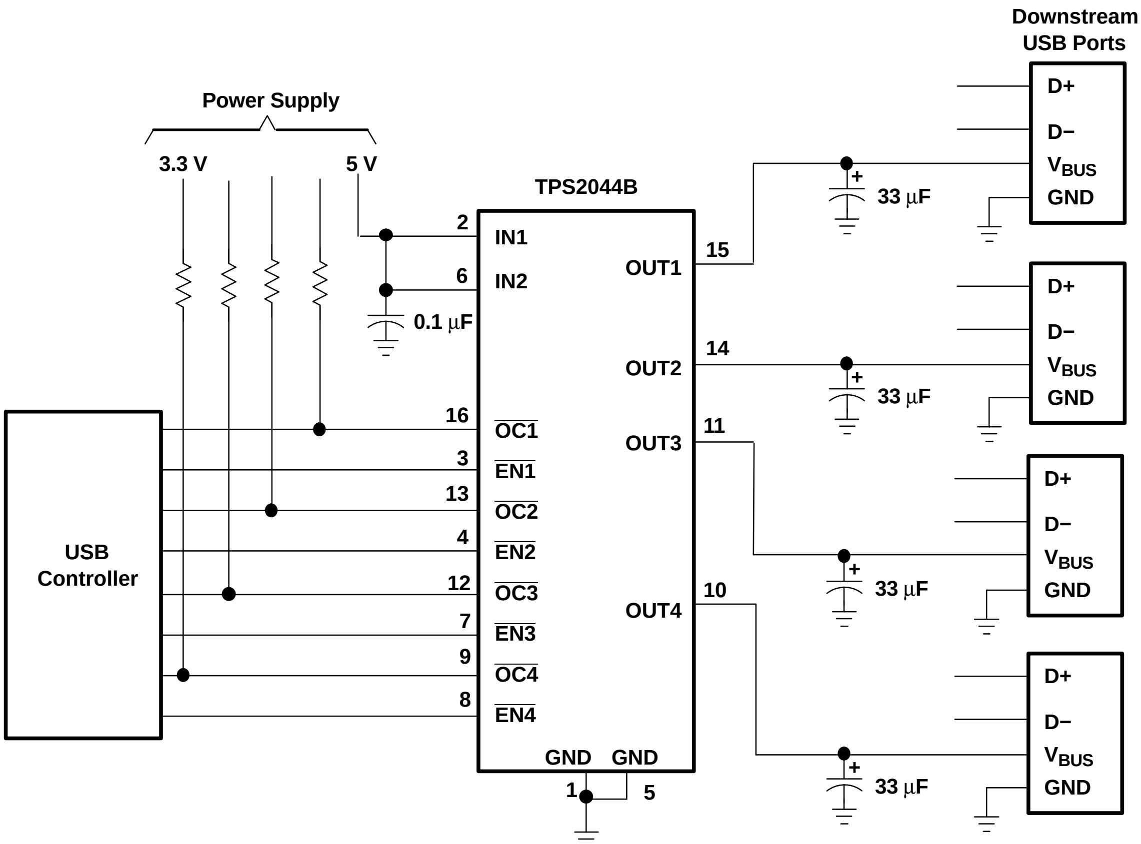


Figure 31. Typical Four-Port USB Host / Self-Powered Hub

Bus-powered hubs obtain all power from upstream ports and often contain an embedded function. The hubs are required to power up with less than one unit load. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This can be accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than one unit load. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

LOW-POWER BUS-POWERED AND HIGH-POWER BUS-POWERED FUNCTIONS

Both low-power and high-power bus-powered functions obtain all power from upstream ports; low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 µF at power up, the device must implement inrush current limiting (see Figure 32).

APPLICATION INFORMATION (continued)

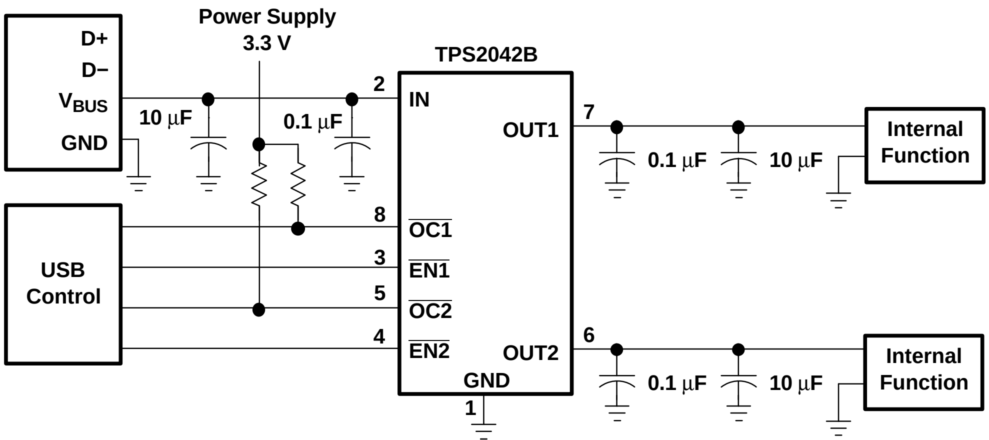


Figure 32. High-Power Bus-Powered Function (Example, TPS2042B)

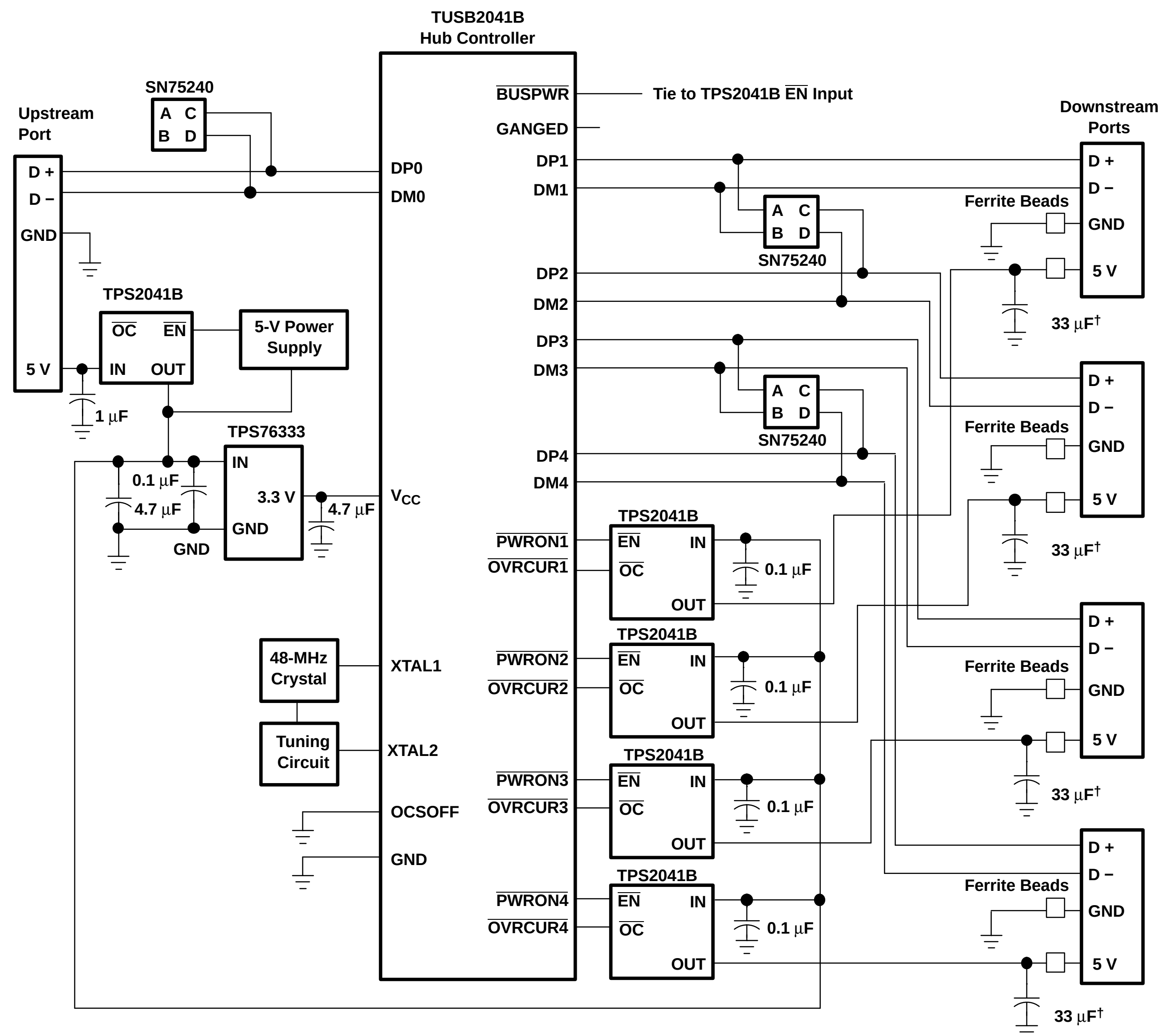
USB POWER-DISTRIBUTION REQUIREMENTS

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power-distribution features must be implemented.

- Hosts/self-powered hubs must:
  – Current-limit downstream ports
  – Report overcurrent conditions on USB V_{BUS}
- Bus-powered hubs must:
  – Enable/disable power to downstream ports
  – Power up at <100 mA
  – Limit inrush current (<44 Ω and 10 µF)
- Functions must:
  – Limit inrush currents
  – Power up at <100 mA

The feature set of the TPS204xB/TPS205xB allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-powered hubs, as well as the input ports for bus-powered functions (see Figure 33 through Figure 36).

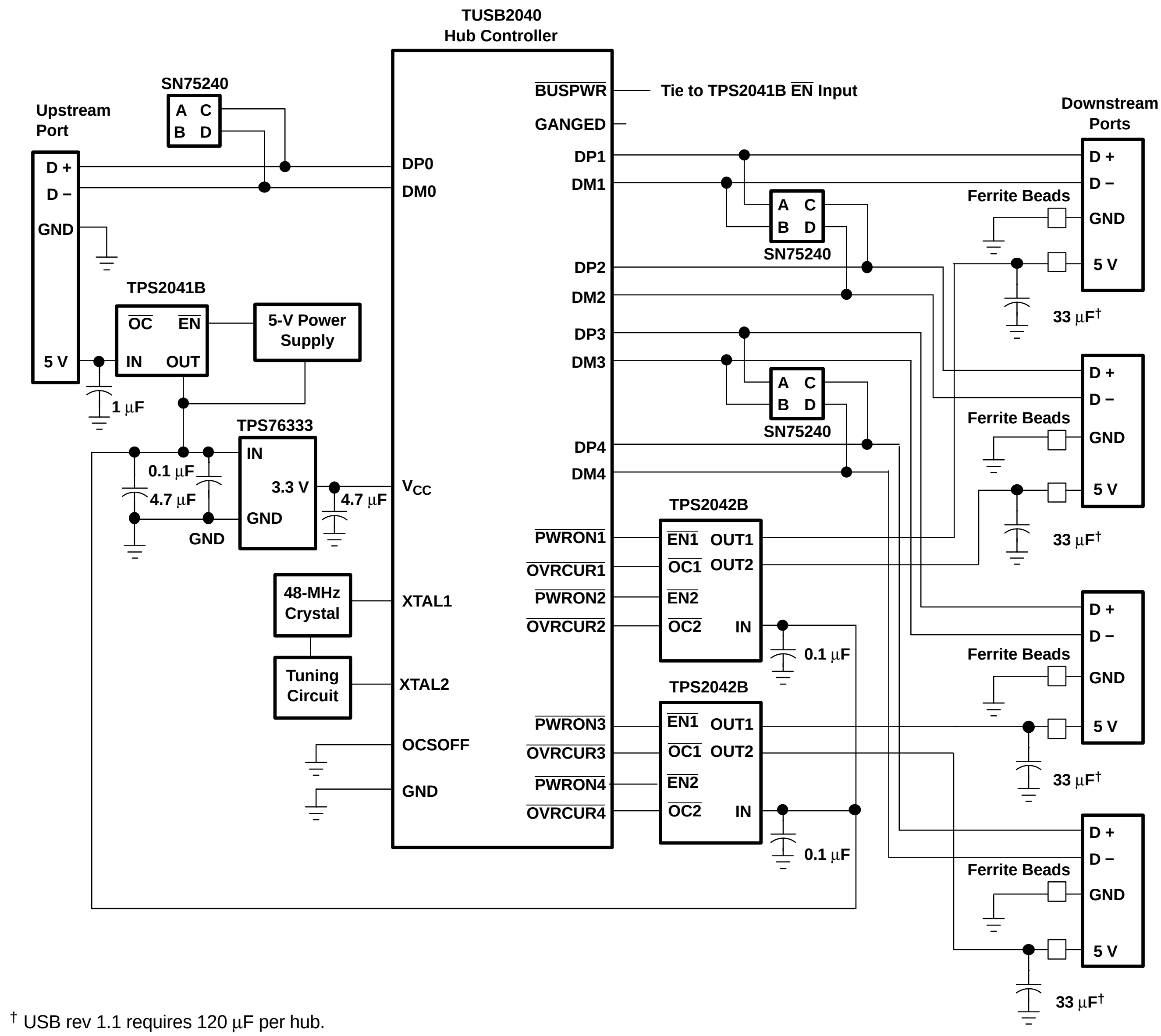
APPLICATION INFORMATION (continued)



† USB rev 1.1 requires 120 µF per hub.

Figure 33. Hybrid Self / Bus-Powered Hub Implementation, TPS2041B/TPS2051B

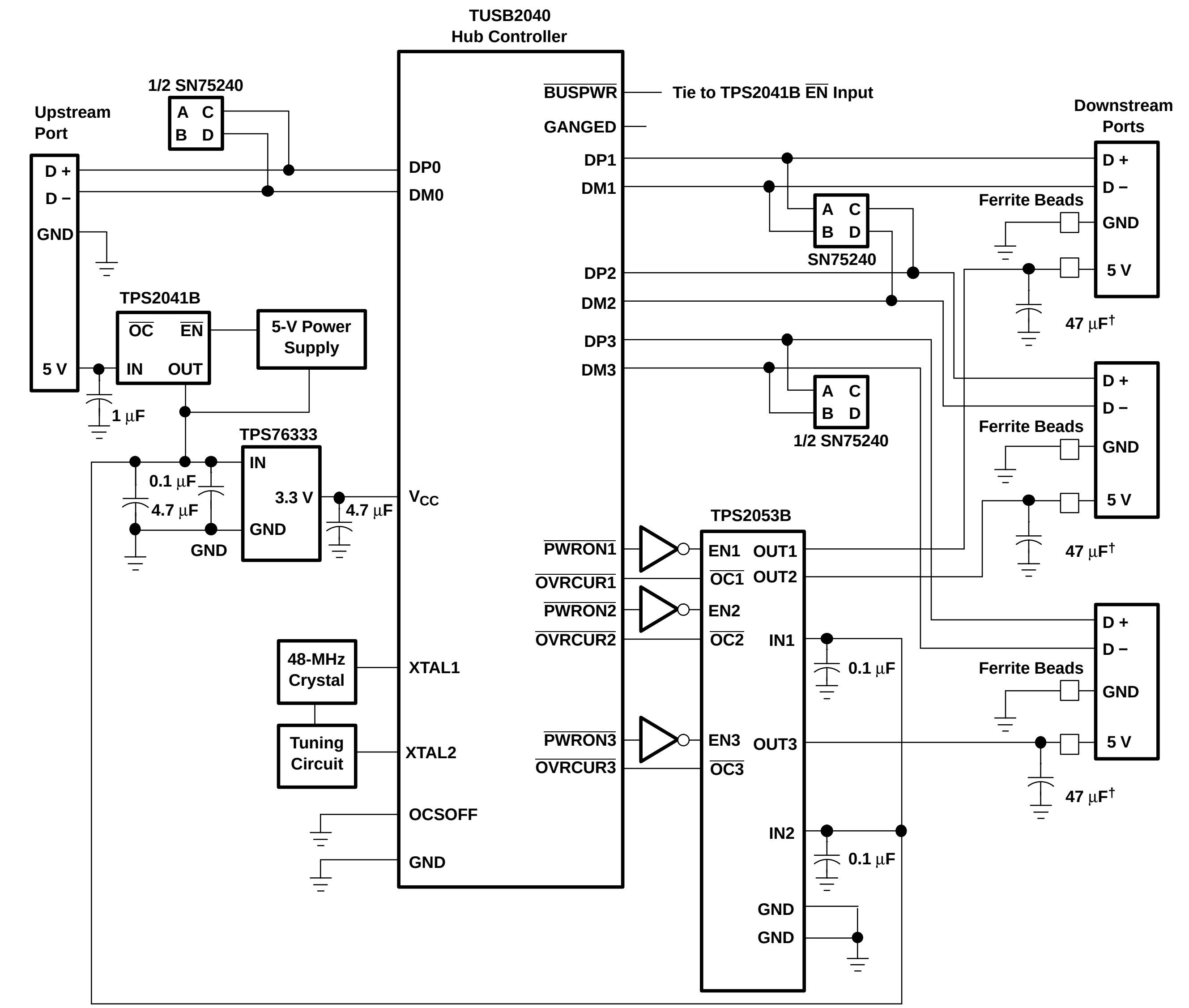
APPLICATION INFORMATION (continued)



† USB rev 1.1 requires 120 µF per hub.

Figure 34. Hybrid Self / Bus-Powered Hub Implementation, TPS2042B/TPS2052B

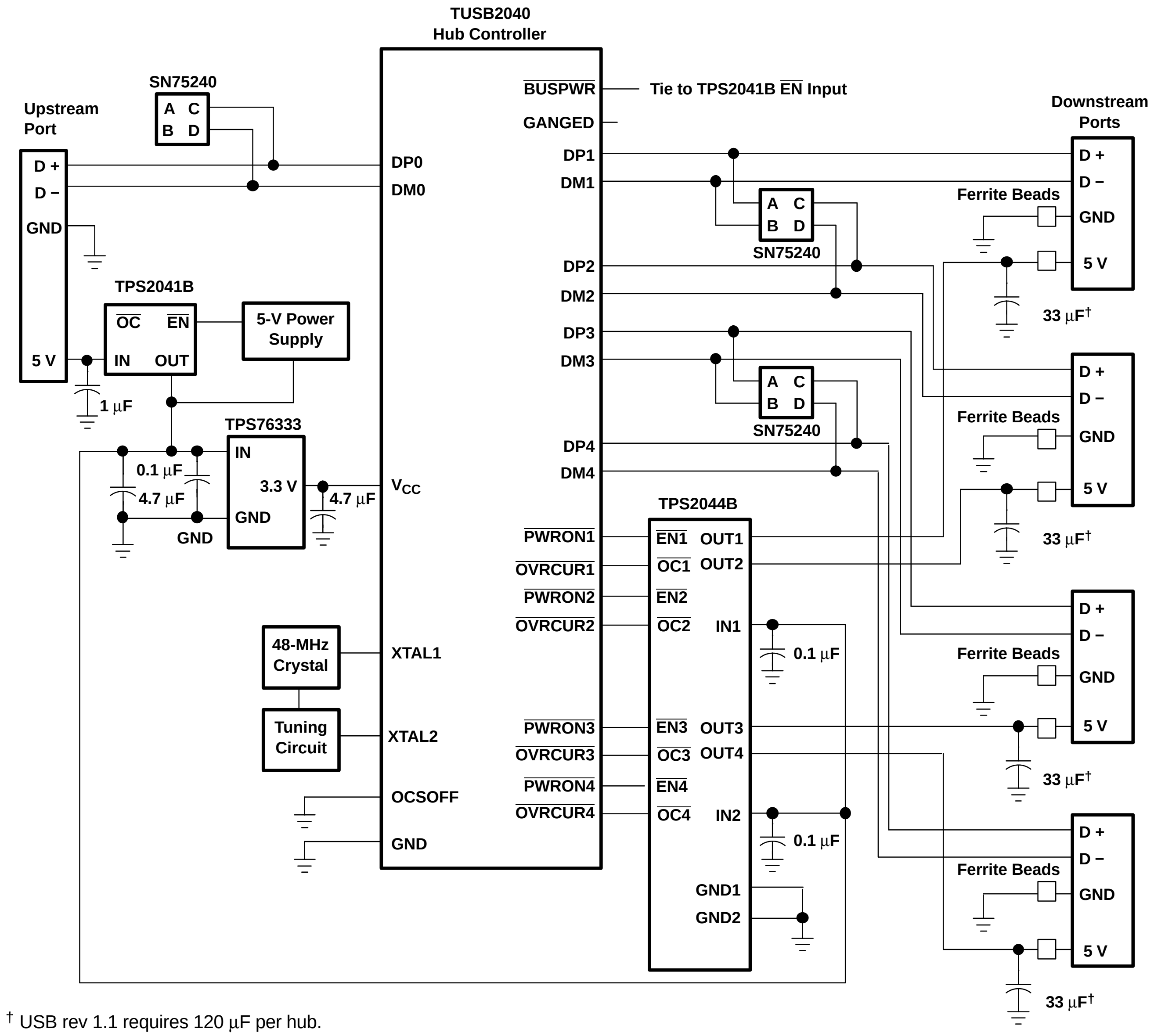
APPLICATION INFORMATION (continued)



† USB rev 1.1 requires 120 µF per hub.

Figure 35. Hybrid Self / Bus-Powered Hub Implementation, TPS2043B/TPS2053B

APPLICATION INFORMATION (continued)



† USB rev 1.1 requires 120 µF per hub.

Figure 36. Hybrid Self / Bus-Powered Hub Implementation, TPS2044B/TPS2054B

APPLICATION INFORMATION (continued)

GENERIC HOT-PLUG APPLICATIONS

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS204xB/TPS205xB, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS204xB/TPS205xB also ensures that the switch is off after the card has been removed, and that the switch is off during the next insertion. The UVLO feature insures a soft start with a controlled rise time for every insertion of the card or module.

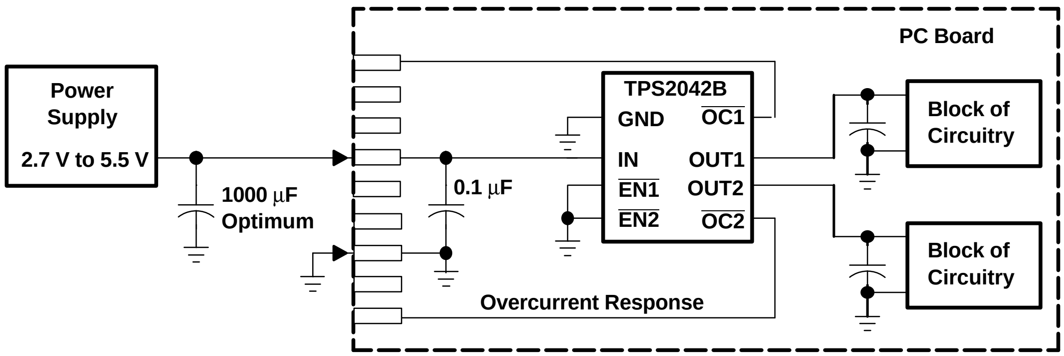


Figure 37. Typical Hot-Plug Implementation (Example, TPS2042B)

By placing the TPS204xB/TPS205xB between the V_{CC} input and the rest of the circuitry, the input power reaches these devices first after insertion. The typical rise time of the switch is approximately 1 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

DETAILED DESCRIPTION

Power Switch

The power switch is an N-channel MOSFET with a low on-state resistance. Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled. The power switch supplies a minimum current of 500 mA.

Charge Pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires little supply current.

Driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage.

Enable ($\overline{\text{ENx}}$)

The logic enable pin disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current. The supply current is reduced to less than 1 µA or 2 µA when a logic high is present on $\overline{\text{EN}}$. A logic zero input on $\overline{\text{EN}}$ restores bias to the drive and control circuits and turns the switch on. The enable input is compatible with both TTL and CMOS logic levels.

DETAILED DESCRIPTION (continued)

Enable (ENx)

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current. The supply current is reduced to less than 1 µA or 2 µA when a logic low is present on ENx. A logic high input on ENx restores bias to the drive and control circuits and turns the switch on. The enable input is compatible with both TTL and CMOS logic levels.

Overcurrent ($\overline{OCx}$)

The $\overline{OCx}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output remains asserted until the overcurrent or overtemperature condition is removed. A 10-ms deglitch circuit prevents the $\overline{OCx}$ signal from oscillation or false triggering. If an overtemperature shutdown occurs, the $\overline{OCx}$ is asserted instantaneously.

Current Sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant-current mode and holds the current constant while varying the voltage on the load.

Thermal Sense

The TPS204xB/TPS205xB implements a thermal sensing to monitor the operating temperature of the power distribution switch. In an overcurrent or short-circuit condition, the junction temperature rises. When the die temperature rises to approximately 140°C due to overcurrent conditions, the internal thermal sense circuitry turns off the switch, thus preventing the device from damage. Hysteresis is built into the thermal sense, and after the device has cooled approximately 10 degrees, the switch turns back on. The switch continues to cycle off and on until the fault is removed. The open-drain false reporting output ($\overline{OCx}$) is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

Undervoltage Lockout

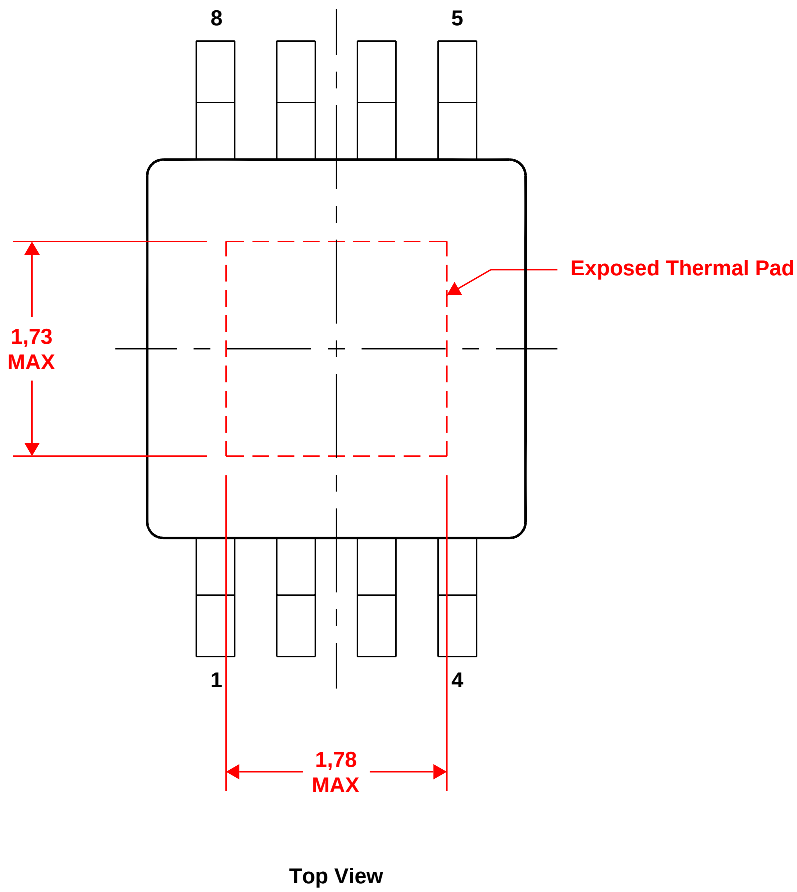
A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. When the thermal pad is soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, *PowerPAD Thermally Enhanced Package*, Texas Instruments Literature No. SLMA002 and Application Brief, *PowerPAD Made Easy*, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



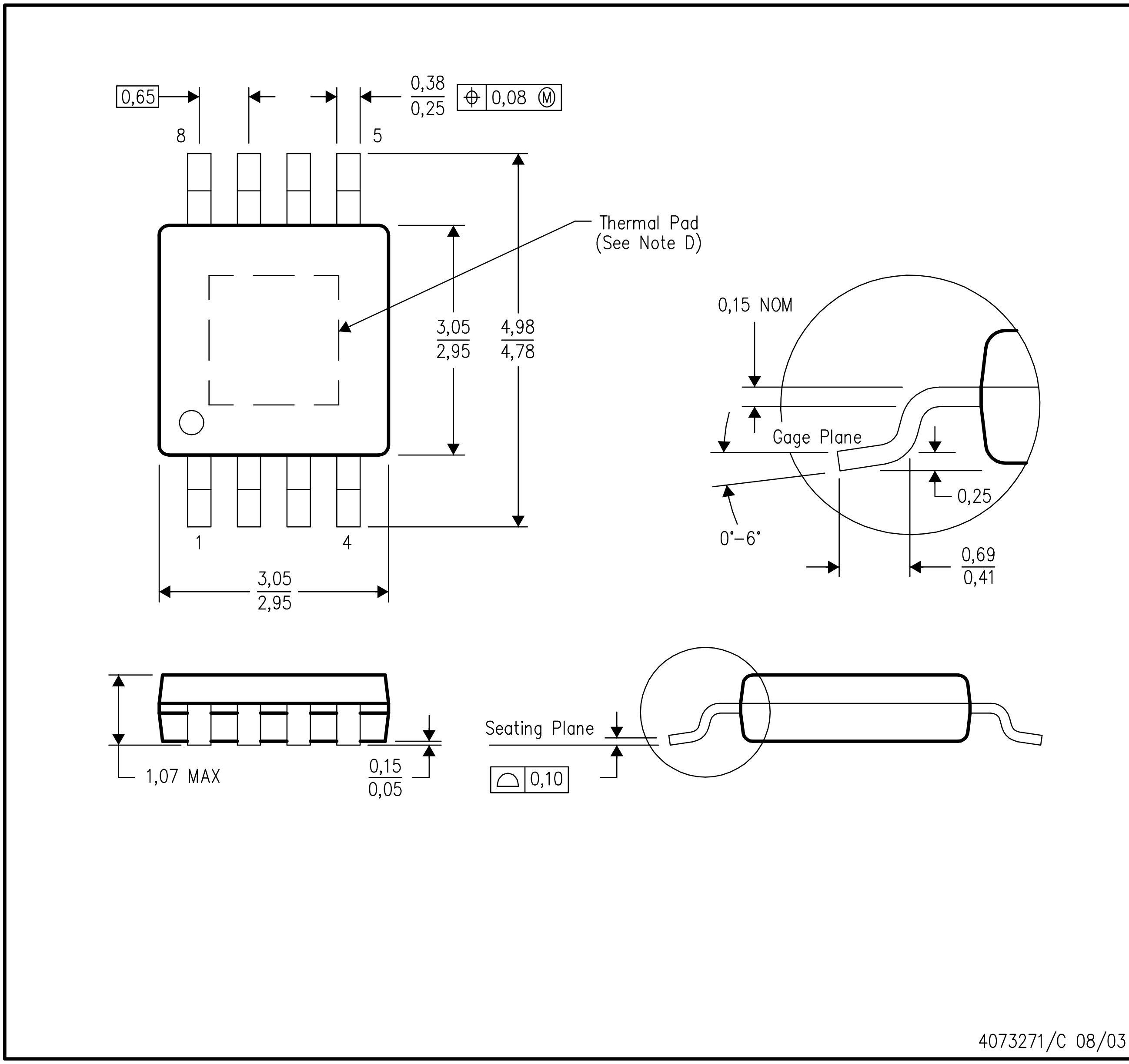
NOTE: All linear dimensions are in millimeters

PPTD041

Exposed Thermal Pad Dimensions

PowerPAD is a trademark of Texas Instruments

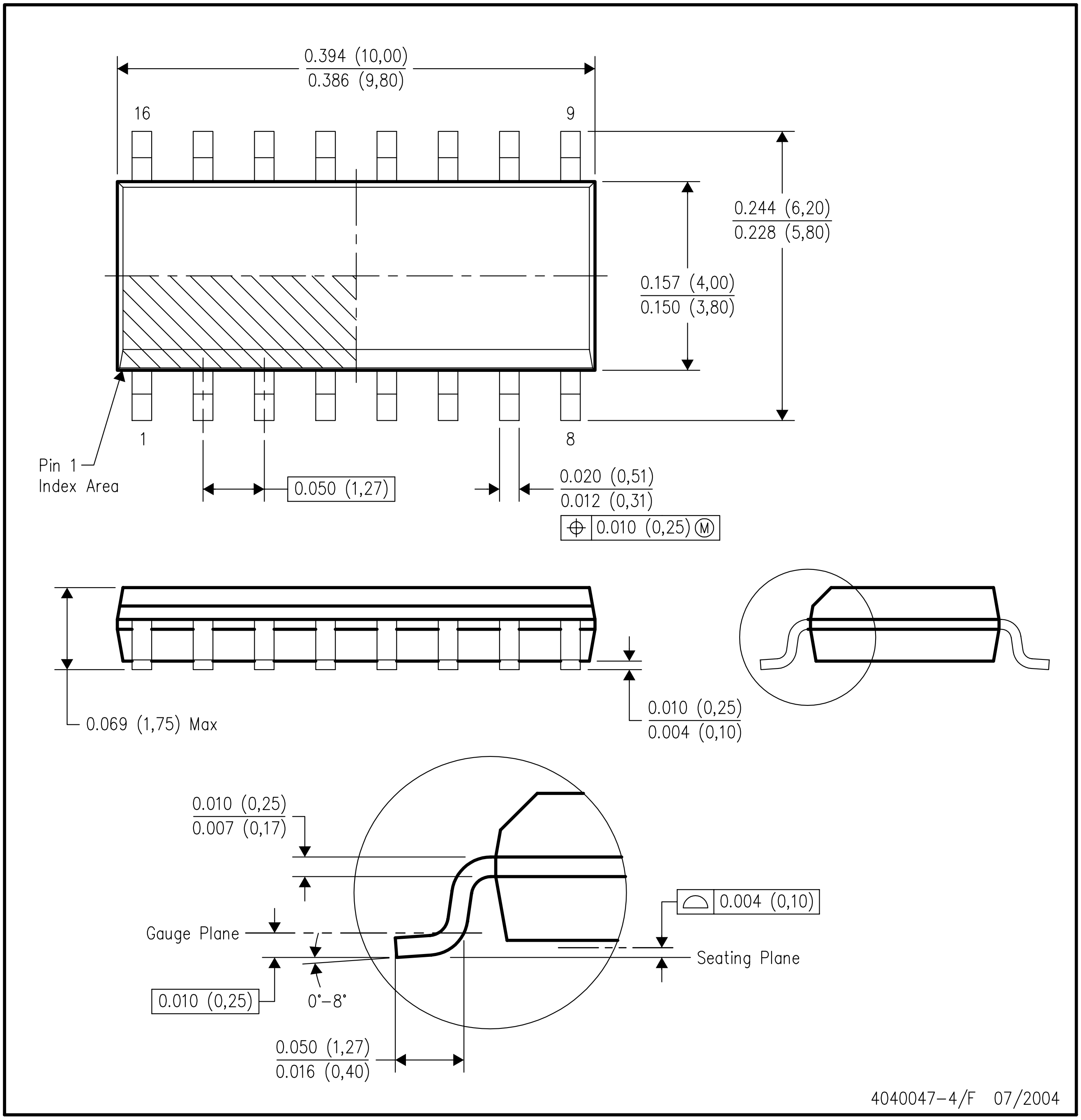
DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
E. Falls within JEDEC MO-187

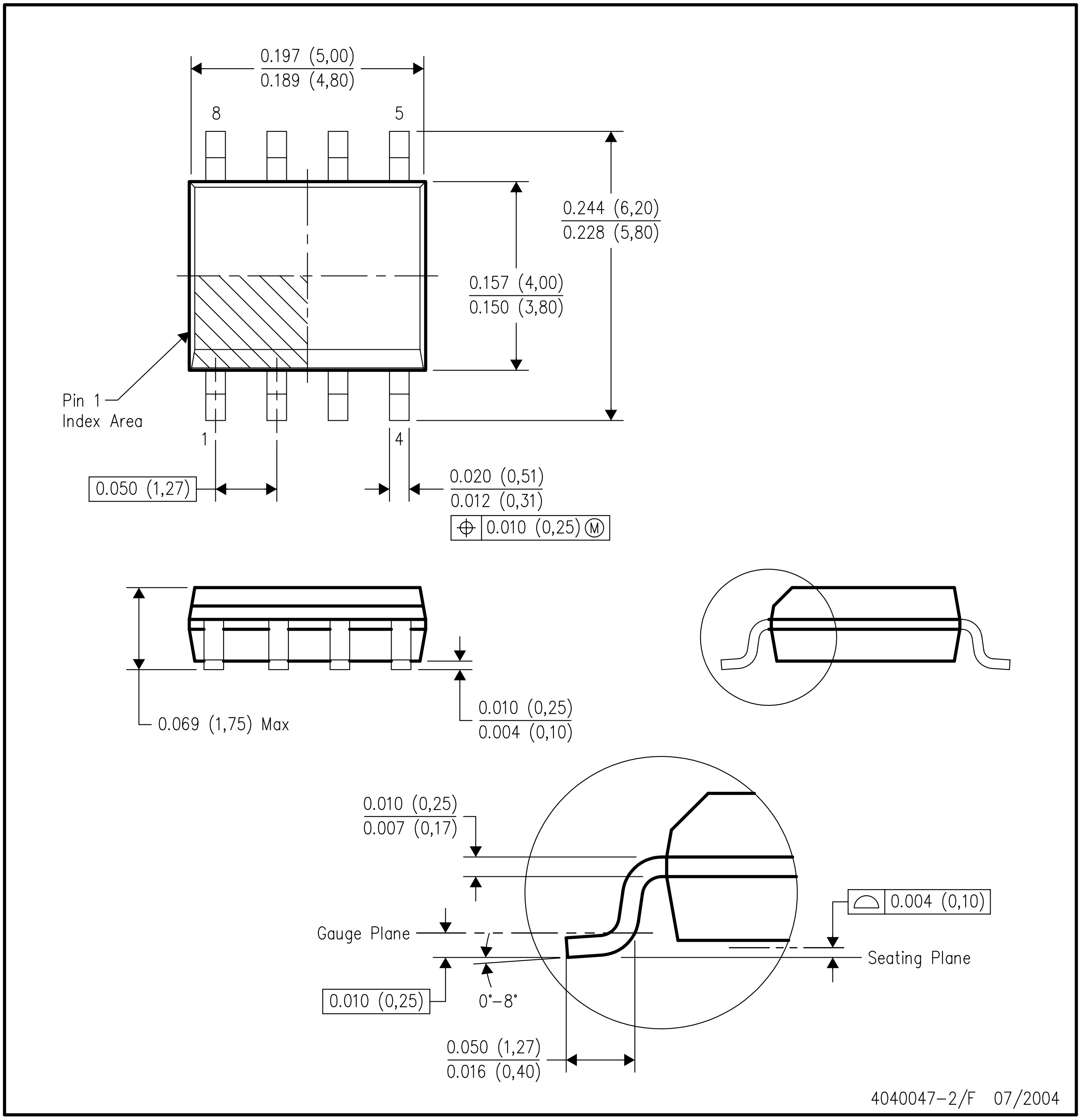
PowerPAD is a trademark of Texas Instruments.

D (R-PDSO-G16) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012 variation AC.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS–012 variation AA.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2004, Texas Instruments Incorporated