

# Hex-Half-Bridge / Double Six-Driver

TLE 6208-6 G

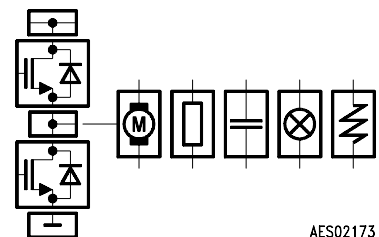
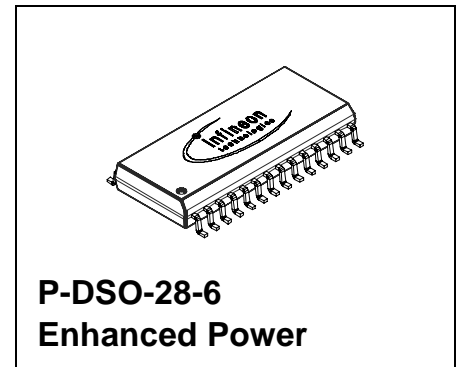
## Data Sheet

SPT 4

### 1 Overview

#### 1.1 Features

- Six High-Side and six Low-Side-Drivers
- Free configurable as switch, halfbridge or H-bridge
- Optimized for DC motor management applications
- 0.6 A continuous (1 A peak) current per switch
- $R_{DS\ ON}$ ; typ. 0.8  $\Omega$ , @ 25 °C per switch
- Outputs fully short circuit protected with diagnosis
- Overtemperature-Protection with hysteresis and diagnosis
- Temperature prewarning
- Standard SPI-Interface
- Very low current consumption (typ. 10  $\mu$ A, @ 25 °C) in stand-by (Inhibit) mode
- Over- and Undervoltage-Lockout
- CMOS/TTL compatible inputs with hysteresis
- Internal clamp diodes
- Enhanced power P-DSO-Package



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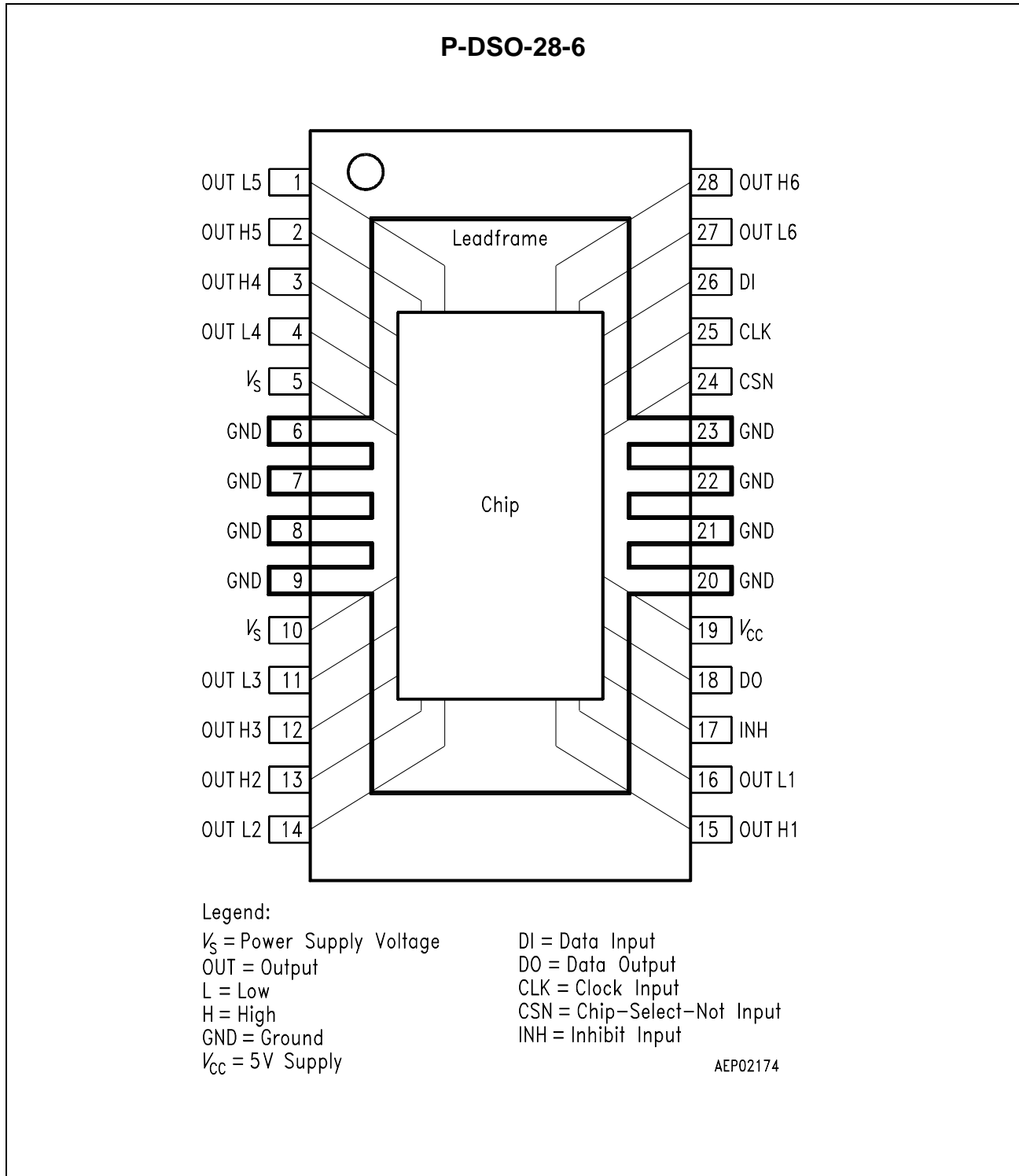
Type	Ordering Code	Package
TLE 6208-6 G	Q67007-A9462	P-DSO-28-6

### Functional Description

The TLE 6208-6 G is a fully protected **Hex-Half-Bridge-Driver** designed specifically for automotive and industrial motion control applications. The part is based on Infineons Smart Power Technology SPT® which allows bipolar and CMOS control circuitry in accordance with DMOS power devices existing on the same monolithic circuitry. The six low and high side drivers are freely configurable and can be controlled separately. Therefore all kind of loads can be combined. In motion control up to 5 actuators (DC-Motors) can be connected to the 6 halfbridge-outputs (cascade configuration). Operation modes forward (cw), reverse (ccw), brake and high impedance are controlled from a standard SPI-Interface. The possibility to control the outputs via software from a central logic, allows limiting the power dissipation. So the standard P-DSO-28-6-package meets the application requirements and saves PCB-Board-space and cost.

Furthermore the build-in features like Over- and Undervoltage-Lockout, Over-Temperature-Protection and the very low quiescent current in stand-by mode opens a wide range of automotive- and industrial-applications.

## 1.2 Pin Configuration (top view)



**Figure 1**

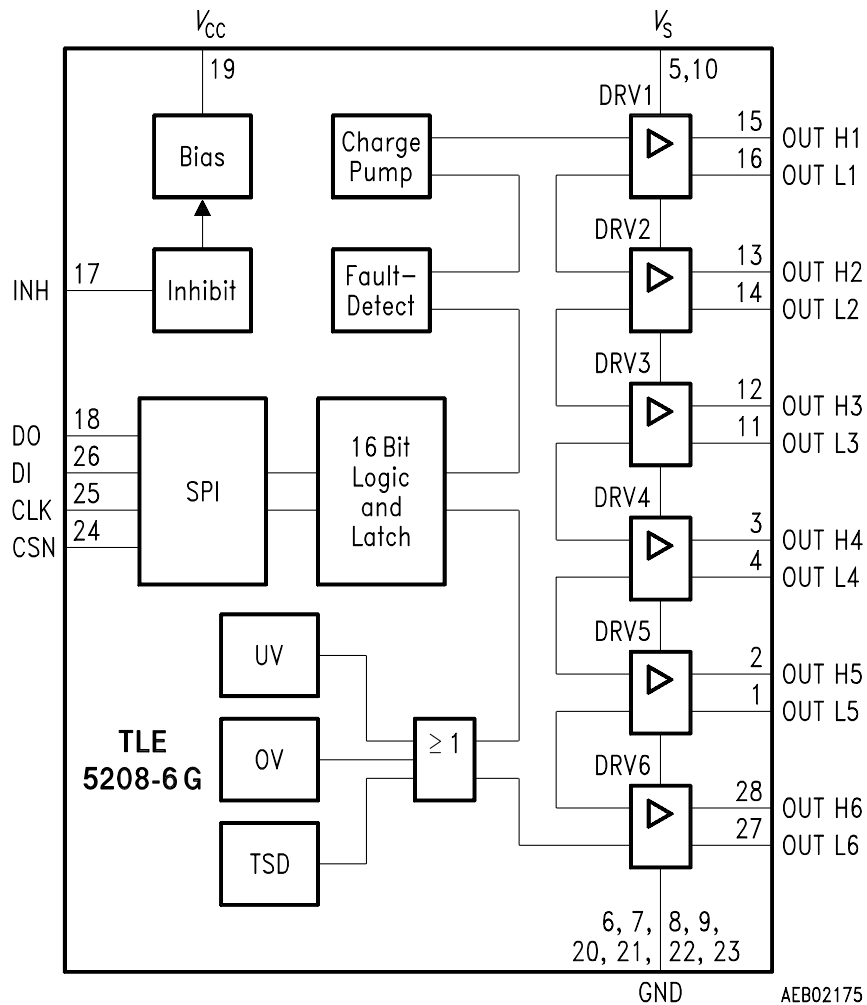
### 1.3 Pin Definitions and Functions

Pin No.	Symbol	Function
1	OUTL5	<b>Low-Side-Output 5</b> ; Power-MOS open drain with internal reverse diode; no internal clamp diode or active zenering; short circuit protected and open load controlled.
2	OUTH5	<b>High-Side-Output 5</b> ; Power-MOS open source with internal reverse diode; no internal clamp diode or active zenering; short circuit protected and open load controlled.
3	OUTH4	<b>High-Side-Output 4</b> ; see pin2.
4	OUTL4	<b>Low-Side-Output 4</b> ; see pin1.
5	$V_S$	<b>Power supply</b> ; external connection to pin 10 necessary; needs a blocking capacitor as close as possible to GND Value: 22 $\mu$ F electrolytic in parallel to 220 nF ceramic.
6, 7, 8, 9	GND	<b>Ground</b> ; Reference potential; internal connection to pin 20, 21, 22 and 23; cooling tab; to reduce thermal resistance; place cooling areas on PCB close to this pins.
10	$V_S$	<b>Power Supply</b> ; see pin 5.
11	OUTL3	<b>Low-Side-Output 3</b> ; see pin1.
12	OUTH3	<b>High-Side-Output 3</b> ; see pin2.
13	OUTH2	<b>High-Side-Output 2</b> ; see pin2.
14	OUTL2	<b>Low-Side-Output 2</b> ; see pin1.
15	OUTH1	<b>High-Side-Output 1</b> ; see pin2.
16	OUTL1	<b>Low-Side-Output 1</b> ; see pin1.
17	INH	<b>Inhibit input</b> ; has an internal pull down; device is switched in standby condition by pulling the INH terminal low.
18	DO	<b>Serial-Data-Output</b> ; this 3-state output transfers diagnosis data to the control device; the output will remain 3-stated unless the device is selected by a low on Chip-Select-Not (CSN); see <b>Table 2</b> for Diagnosis protocol.
19	$V_{CC}$	<b>Logic supply voltage</b> ; needs a blocking capacitor as close as possible to GND; Value: 10 $\mu$ F electrolytic in parallel to 220 nF ceramic.

### 1.3 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Function
20, 21, 22, 23	GND	<b>Ground</b>
24	CSN	<b>Chip-Select-Not input</b> ; CSN is an active low input; serial communication is enabled by pulling the CSN terminal low; CSN input should only be transitioned when CLK is low; CSN has an internal active pull up and requires CMOS logic level inputs.
25	CLK	<b>Serial clock input</b> ; clocks the shiftregister; CLK has an internal active pull down and requires CMOS logic level inputs.
26	DI	<b>Serial data input</b> ; receives serial data from the control device; serial data transmitted to DI is an 16bit control word with the Least Significant Bit (LSB) being transferred first: the input has an active pull down and requires CMOS logic level inputs; DI will accept data on the falling edge of CLK-signal; see <b>Table 1</b> for input data protocol.
27	OUTL6	<b>Low-Side-Output 6</b> ; see pin1.
28	OUTH6	<b>High-Side-Output 6</b> ; see pin2.

## 1.4 Functional Block Diagram



**Figure 2**  
**Block Diagram**

## 1.5 Circuit Description

**Figure 2** shows a block schematic diagram of the module.

There are 6 halfbridge drivers on the right-hand side. An HS driver and an LS driver are combined to form a halfbridge driver in each case.

The drivers communicate via the internal data bus with the logic and the other control and monitoring functions: undervoltage (UV), overvoltage (OV), overtemperature (TSD), charge pump and fault detect.

Two connection interfaces are provided for supply to the module: All power drivers are connected to the supply voltage  $V_S$ . These are monitored by overvoltage and undervoltage comparators with hysteresis, so that the correct function can be checked in the application at any time.

The logic is supplied by the  $V_{CC}$  voltage, typ. with 5 V. The  $V_{CC}$  voltage uses an internally generated Power-On Reset (POR) to initialize the module at power-on. The advantage of this system is that information stored in the logic remains intact in the event of short-term failures in the supply voltage  $V_S$ . The system can therefore continue to operate following  $V_S$  undervoltage, without having to be reprogrammed. The “undervoltage” information is stored, and can be read out via the interface. The same logically applies for overvoltage. “Interference spikes” on  $V_S$  are therefore effectively suppressed.

The situation is different in the case of undervoltage on the  $V_{CC}$  connection pin. If this occurs, then the internally stored data is deleted, and the output levels are switched to high-impedance status (tristate). The module is initialized by  $V_{CC}$  following restart (Power-On Reset = POR).

The 16-bit wide programming word or control word (see **Table 1**) is read in via the DI data input, and this is synchronized with the clock input CLK. The status word appears synchronously at the DO data output (see **Table 2**).

The transmission cycle begins when the chip is selected with the CSN input (H to L). If the CSN input changes from L to H then the word which has been read in becomes the control word. The DO output switches to tristate status at this point, thereby releasing the DO bus circuit for other uses.

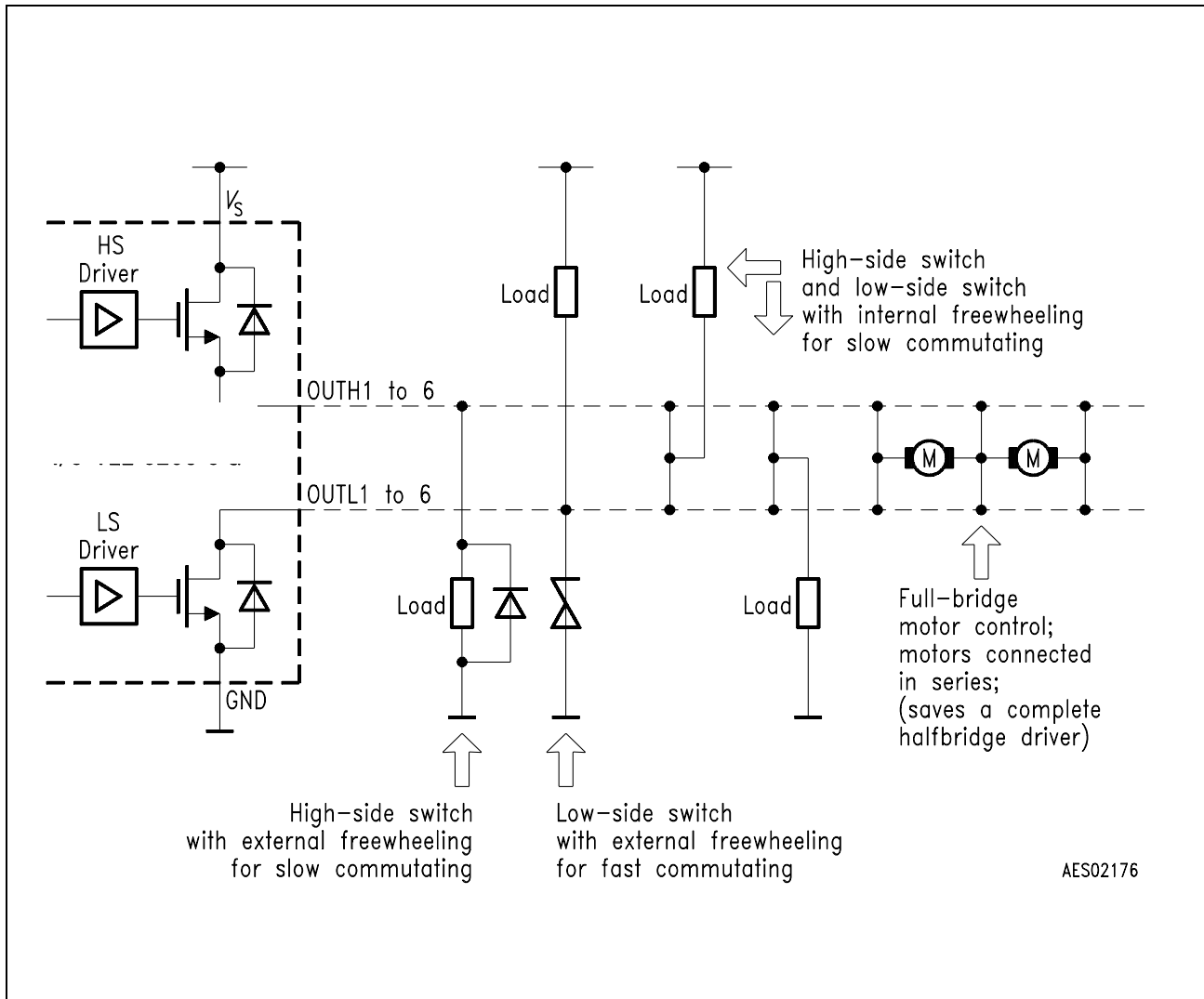
The INH inhibit input can be used to cut off the complete module. This reduces the current consumption to just a few  $\mu\text{A}$ , and results in the loss of any data stored. The output levels are switched to tristate status. The module is reinitialized with the internally generated POR (Power-On Reset) at restart.

This feature allows the use of this module in battery-operated applications (vehicle body control applications).

Every driver block from DRV 1 to 6 contains a low-side driver and a high-side driver. The output connections have been selected so that each HS driver and LS driver pair can be combined to form a halfbridge by short-circuiting adjacent connections. The full flexibility of the configuration can be achieved by dissecting the halfbridges into “quarter-bridges”.

**Table 3** shows examples of possible applications.

When commutating inductive loads, the dissipated power peak can be significantly reduced by activating the transistor located parallel to the internal freewheeling diode. A special, integrated “timer” for power ON/OFF times ensures there is no crossover current at the halfbridge.



**Figure 3**  
**Configuration Examples for “Quarter Bridges” on the TLE 6208-6 G**

**Table 1**  
**Input Data Protocol**

<b>BIT</b>	
15	OVLO on/off
14	Underload SD on/off
13	Overcurrent SD on/off
12	HS-Switch 6
11	LS-Switch 6
10	HS-Switch 5
9	LS-Switch 5
8	HS-Switch 4
7	LS-Switch 4
6	HS-Switch 3
5	LS-Switch 3
4	HS-Switch 2
3	LS-Switch 2
2	HS-Switch 1
1	LS-Switch 1
0	Status Register Reset

H = ON  
L = OFF

**Table 2**  
**Diagnosis Data Protocol**

<b>BIT</b>	
15	Power supply fail
14	Underload
13	Overload
12	Status HS-Switch 6
11	Status LS-Switch 6
10	Status HS-Switch 5
9	Status LS-Switch 5
8	Status HS-Switch 4
7	Status LS-Switch 4
6	Status HS-Switch 3
5	Status LS-Switch 3
4	Status HS-Switch 2
3	Status LS-Switch 2
2	Status HS-Switch 1
1	Status LS-Switch 1
0	Temp. Prewarning

H = ON  
L = OFF

**Table 3**  
**Fault Result Table**

<b>Fault</b>	<b>Diag.-Bit</b>	<b>Result</b>
Overcurrent (load)	13	Only the failed output is switched OFF. Function and protection can be deactivated by bit No. 13.
Short circuit to GND (high-side-switch)	13	Only the failed output is switched OFF. Function and protection can be deactivated by bit No. 13.
Short circuit to $V_S$ (low-side-switch)	13	Only the failed output is switched OFF. Function and protection can be deactivated by bit No. 13.
Temperature warning	0	Reaction of control device needed.
Temperature shut down (SD)	–	All outputs OFF.
Openload	14	Only the failed output is switched OFF. Function can be deactivated by bit No. 14.
Underload	14	Only the failed output is switched OFF. Function can be deactivated by bit No. 14.
Undervoltage lockout (UVLO)	15	All outputs OFF.
Overvoltage lockout (OVLO)	15	All outputs OFF. Function can be deactivated by bit No. 15.

H = failure;  
L = no failure.

## 2 Electrical Characteristics

### 2.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		

#### Voltages

Supply voltage	$V_S$	- 0.3	40	V	–
Supply voltage	$V_S$	- 1	–	V	$t < 0.5 \text{ s}; I_S > - 2 \text{ A}$
Logic supply voltage	$V_{CC}$	- 0.3	5.5	V	$0 \text{ V} < V_S < 40 \text{ V}$
Logic input voltages (DI, CLK, CSN, INH)	$V_I$	- 0.3	5.5	V	$0 \text{ V} < V_S < 40 \text{ V}$ $0 \text{ V} < V_{CC} < 5.5 \text{ V}$
Logic output voltage (DO)	$V_{DO}$	- 0.3	$V_{CC}$	V	$0 \text{ V} < V_S < 40 \text{ V}$ $0 \text{ V} < V_{CC} < 5.5 \text{ V}$

#### Currents

Output current (cont.), if Bit13 (OCSD) is set.	$I_{OUT1-6}$	–	–	A	internal limited
Output current (cont.), if Bit13 (OCSD) is deactivated.	$I_{OUT1-6}$	- 1.5	1.5	A	$V_{DS} = 12 \text{ V}$
		- 0.7	0.7	A	$V_{DS} = 20 \text{ V}$
		- 0.25	0.25	A	$V_{DS} = 40 \text{ V}$
Output current (peak), if Bit13 (OCSD) is set.	$I_{OUT1-6}$	–	–	A	internal limited
Output current (peak), if Bit13 (OCSD) is deactivated. $t_P < 50 \text{ ms}; t = 1 \text{ s};$	$I_{OUT1-6}$	- 2	2	A	$V_{DS} = 12 \text{ V}$
		- 0.9	0.9	A	$V_{DS} = 20 \text{ V}$
		- 0.3	0.3	A	$V_{DS} = 40 \text{ V}$

#### Temperatures

Junction temperature	$T_j$	- 40	150	°C	–
Storage temperature	$T_{stg}$	- 50	150	°C	–

*Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.*

## 2.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	$V_S$	$V_{UV\ OFF}$	40	V	After $V_S$ rising above $V_{UV\ ON}$
Supply voltage slew rate	$dV_S/dt$	–	10	V/ $\mu$ s	–
Logic supply voltage	$V_{CC}$	4.75	5.50	V	–
Supply voltage increasing	$V_S$	– 0.3	$V_{UV\ ON}$	V	Outputs in tristate
Supply voltage decreasing	$V_S$	– 0.3	$V_{UV\ OFF}$	V	Outputs in tristate
Logic input voltage (DI, CLK, CSN, INH)	$V_I$	– 0.3	$V_{CC}$	V	–
SPI clock frequency	$f_{CLK}$	–	2	MHz	–
Junction temperature	$T_j$	– 40	150	°C	–

## Thermal Resistances

Junction pin	$R_{thj-pin}$	–	25	K/W	measured to pin 7
Junction ambient	$R_{thjA}$	–	65	K/W	–

## 2.3 Electrical Characteristics

8 V <  $V_S$  < 40 V; 4.75 V <  $V_{CC}$  < 5.25 V; INH = High; all outputs open; – 40 °C <  $T_j$  < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

### Current Consumption

Quiescent current	$I_S$	–	10	20	μA	INH = Low; $V_S = 13.2$ V; $T_j = 25$ °C
Quiescent current	$I_S$	–	–	40	μA	INH = Low; $V_S = 13.2$ V
Supply current	$I_S$	–	2.0	4.0	mA	–
Logic-Supply current	$I_{CC}$	–	2	10	μA	INH = Low
Logic-Supply current	$I_{CC}$	–	1.6	3.0	mA	SPI not active

### Over- and Under-Voltage Lockout

UV-Switch-ON voltage	$V_{UV\ ON}$	–	6.5	7.0	V	$V_S$ increasing
UV-Switch-OFF voltage	$V_{UV\ OFF}$	5.5	6.0	6.6	V	$V_S$ decreasing
UV-ON/OFF-Hysteresis	$V_{UV\ HY}$	–	0.5	–	V	$V_{UV\ ON} - V_{UV\ OFF}$
OV-Switch-OFF voltage	$V_{OV\ OFF}$	34	37	40	V	$V_S$ increasing
OV-Switch-ON voltage	$V_{OV\ ON}$	28	32	36	V	$V_S$ decreasing
OV-ON/OFF-Hysteresis	$V_{OV\ HY}$	–	5.0	–	V	$V_{OV\ OFF} - V_{OV\ ON}$

## 2.3 Electrical Characteristics (cont'd)

$8\text{ V} < V_S < 40\text{ V}$ ;  $4.75\text{ V} < V_{CC} < 5.25\text{ V}$ ; INH = High; all outputs open;  $-40\text{ °C} < T_j < 150\text{ °C}$ ; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

### Outputs OUTH1-6 and OUTL1-6

#### Static Drain-Source-On Resistance

Source (High-Side) $I_{OUT} = -0.5\text{ A}$	$R_{DS\ ON\ H}$	–	0.9	1.3	$\Omega$	$8\text{ V} < V_S < 40\text{ V}$ $T_j = 25\text{ °C}$
			–	2.0	$\Omega$	$8\text{ V} < V_S < 40\text{ V}$
			2.0	–	$\Omega$	$V_{S\ OFF} < V_S \leq 8\text{ V}$ $T_j = 25\text{ °C}$
			–	4.0	$\Omega$	$V_{S\ OFF} < V_S \leq 8\text{ V}$
Sink (Low-Side) $I_{OUT} = 0.5\text{ A}$	$R_{DS\ ON\ L}$	–	0.8	1.2	$\Omega$	$8\text{ V} < V_S < 40\text{ V}$ $T_j = 25\text{ °C}$
			–	2.0	$\Omega$	$8\text{ V} < V_S < 40\text{ V}$
			2.0	–	$\Omega$	$V_{S\ OFF} < V_S \leq 8\text{ V}$ $T_j = 25\text{ °C}$
			–	4.0	$\Omega$	$V_{S\ OFF} < V_S \leq 8\text{ V}$

*Note: Values of  $R_{DS\ ON}$  for  $V_{S\ OFF} < V_S \leq 8\text{ V}$  are guaranteed by design.*

#### Leakage Current

Source-Output-Stage 1 to 6	$I_{QLH}$	– 50	–	–	$\mu\text{A}$	$V_{OUTH1-6} = 0\text{ V}$
Sink-Output-Stage 1 to 6	$I_{QLL}$	–	–	50	$\mu\text{A}$	$V_{OUTL1-6} = V_S$

#### Overcurrent

Source shutdown threshold	$I_{SDU}$	– 2.0	– 1.5	– 1.0	A	–
Sink shutdown threshold	$I_{SDL}$	1.0	1.5	2.0	A	–
Current limit	$I_{OCL}$	–	3.0	5.0	A	sink and source
Shutdown delay time	$t_{dSD}$	10	25	50	$\mu\text{s}$	sink and source

## 2.3 Electrical Characteristics (cont'd)

8 V <  $V_S$  < 40 V; 4.75 V <  $V_{CC}$  < 5.25 V; INH = High; all outputs open; – 40 °C <  $T_j$  < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

### Open Circuit

Detection current	$I_{OCD}$	15	30	50	mA	–
Delay time	$t_{dOC}$	200	350	600	μs	–

### Delay Time from Stand-by to Data In

Setup time	$t_{set}$	–	–	100	μs	–
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*Note: setup time is guaranteed by design*

### Output Delay Times; $V_S = 13.2$ V; $R_{Load} = 25$ Ω (device not in stand-by for $t > 1$ ms)

Source (high-side) ON	$t_{d ON H}$	–	7.5	12	μs	–
Source (high-side) OFF	$t_{d OFF H}$	–	3	6	μs	–
Sink (low-side) ON	$t_{d ON L}$	–	6.5	12	μs	–
Sink (low-side) OFF	$t_{d OFF L}$	–	2	5	μs	–
Dead time H to L	$t_{D HL}$	1.5	–	–	μs	$t_{d ON L} - t_{d OFF H}$
Dead time L to H	$t_{D LH}$	2.5	–	–	μs	$t_{d ON H} - t_{d OFF L}$

### Output Switching Times; $V_S = 13.2$ V; $R_{Load} = 25$ Ω (device not in stand-by for $t > 1$ ms)

Source (high-side) rise-time	$t_{ON H}$	–	4	8	μs	–
Source (high-side) fall-time	$t_{OFF H}$	–	2	3	μs	–
Sink (low-side) fall-time	$t_{ON L}$	–	1	3	μs	–
Sink (low-side) rise-time	$t_{OFF L}$	–	1	2	μs	–

### Clamp Diodes Forward Voltage

Upper	$V_{FU}$	–	0.9	1.3	V	$I_F = 0.5$ A
Lower	$V_{FL}$	–	0.9	1.3	V	$I_F = 0.5$ A

## 2.3 Electrical Characteristics (cont'd)

8 V <  $V_S$  < 40 V; 4.75 V <  $V_{CC}$  < 5.25 V; INH = High; all outputs open; – 40 °C <  $T_j$  < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

### Inhibit Input

H-input voltage threshold	$V_{IH}$	–	–	0.7	$V_{CC}$	–
L-input voltage threshold	$V_{IL}$	0.2	–	–	$V_{CC}$	–
Hysteresis of input voltage	$V_{IHY}$	50	200	500	mV	–
Pull down current	$I_I$	10	25	50	μA	$V_I = 0.2 \times V_{CC}$
Input capacitance	$C_I$	–	10	15	pF	0 V < $V_{CC}$ < 5.25 V

*Note: Capacitances are guaranteed by design*

### SPI-Interface

#### Delay Time from Stand-by to Data In

Setup time	$t_{set}$	–	–	100	μs	–
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### Logic Inputs DI, CLK and CSN

H-input voltage threshold	$V_{IH}$	–	–	0.7	$V_{CC}$	–
L-input voltage threshold	$V_{IL}$	0.2	–	–	$V_{CC}$	–
Hysteresis of input voltage	$V_{IHY}$	50	200	500	mV	–
Pull up current at pin CSN	$I_{ICSN}$	– 50	– 25	– 10	μA	$V_{CSN} = 0.7 \times V_{CC}$
Pull down current at pin DI	$I_{IDI}$	10	25	50	μA	$V_{DI} = 0.2 \times V_{CC}$
Pull down current at pin CLK	$I_{ICLK}$	10	25	50	μA	$V_{CLK} = 0.2 \times V_{CC}$
Input capacitance at pin CSN, DI or CLK	$C_I$	–	10	15	pF	0 V < $V_{CC}$ < 5.25 V

*Note: Capacitances are guaranteed by design*

## 2.3 Electrical Characteristics (cont'd)

8 V <  $V_S$  < 40 V; 4.75 V <  $V_{CC}$  < 5.25 V; INH = High; all outputs open; – 40 °C <  $T_j$  < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

### Logic Output DO

H-output voltage level	$V_{DOH}$	$V_{CC}$ – 1.0	$V_{CC}$ – 0.7	–	V	$I_{DOH} = 1 \text{ mA}$
L-output voltage level	$V_{DOL}$	–	0.2	0.4	V	$I_{DOL} = -1.6 \text{ mA}$
Tri-state leakage current	$I_{DOLK}$	– 10	–	10	µA	$V_{CSN} = V_{CC}$ $0 \text{ V} < V_{DO} < V_{CC}$
Tri-state input capacitance	$C_{DO}$	–	10	15	pF	$V_{CSN} = V_{CC}$ $0 \text{ V} < V_{CC} < 5.25 \text{ V}$

*Note: Capacitances are guaranteed by design*

### Data Input Timing

Clock period	$t_{pCLK}$	1000	–	–	ns	–
Clock high time	$t_{CLKH}$	500	–	–	ns	–
Clock low time	$t_{CLKL}$	500	–	–	ns	–
Clock low before CSN low	$t_{bef}$	500	–	–	ns	–
CSN setup time	$t_{lead}$	500	–	–	ns	–
CLK setup time	$t_{lag}$	500	–	–	ns	–
Clock low after CSN high	$t_{beh}$	500	–	–	ns	–
DI setup time	$t_{DISU}$	250	–	–	ns	–
DI hold time	$t_{DIHO}$	250	–	–	ns	–
Input signal rise time at pin DI, CLK and CSN	$t_{rIN}$	–	–	200	ns	–
Input signal fall time at pin DI, CLK and CSN	$t_{fIN}$	–	–	200	ns	–

### 2.3 Electrical Characteristics (cont'd)

8 V <  $V_S$  < 40 V; 4.75 V <  $V_{CC}$  < 5.25 V; INH = High; all outputs open;  $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$ ; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

#### Data Output Timing

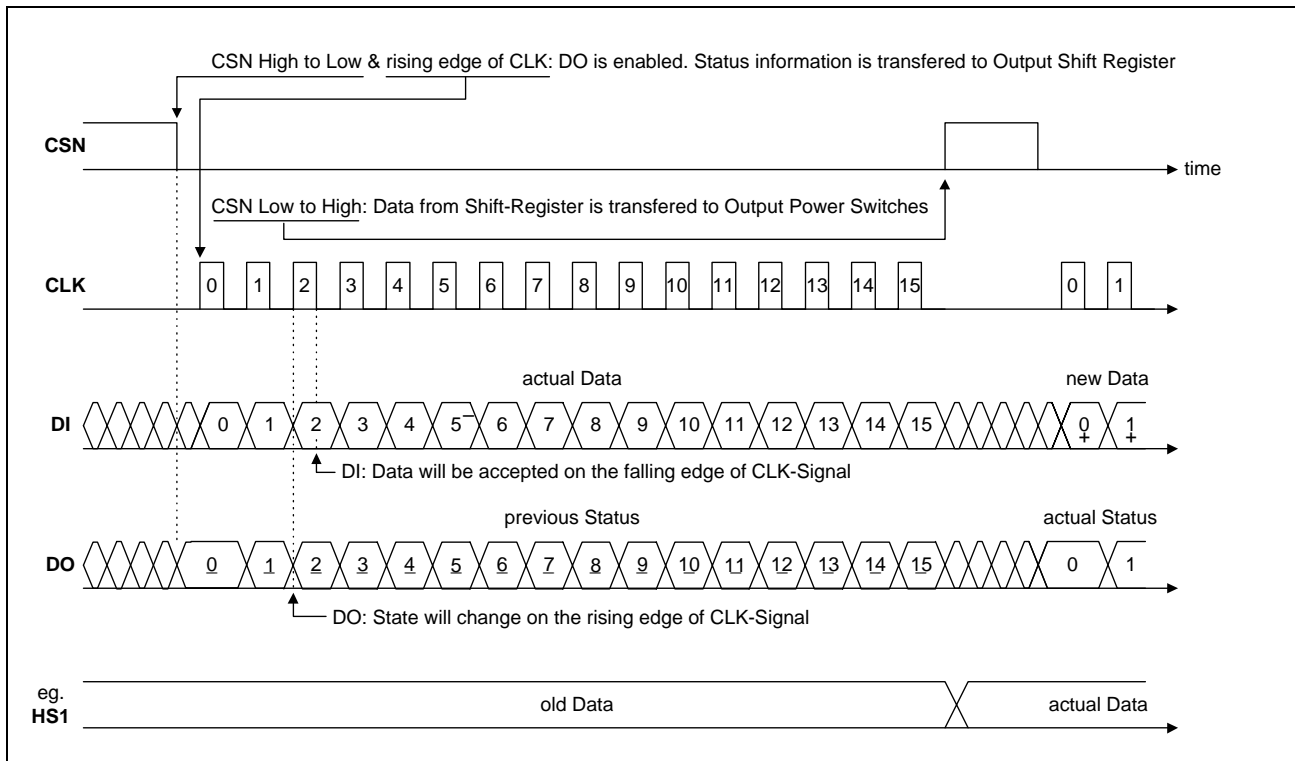
DO rise time	$t_{rDO}$	–	50	100	ns	$C_L = 100\text{ pF}$
DO fall time	$t_{fDO}$	–	50	100	ns	$C_L = 100\text{ pF}$
DO enable time	$t_{ENDO}$	–	–	250	ns	low impedance
DO disable time	$t_{DISDO}$	–	–	250	ns	high impedance
DO valid time	$t_{VADO}$	–	100	250	ns	$V_{DO} < 0.2 V_{CC}$ ; $V_{DO} > 0.7 V_{CC}$ ; $C_L = 100\text{ pF}$

#### Thermal Prewarning and Shutdown

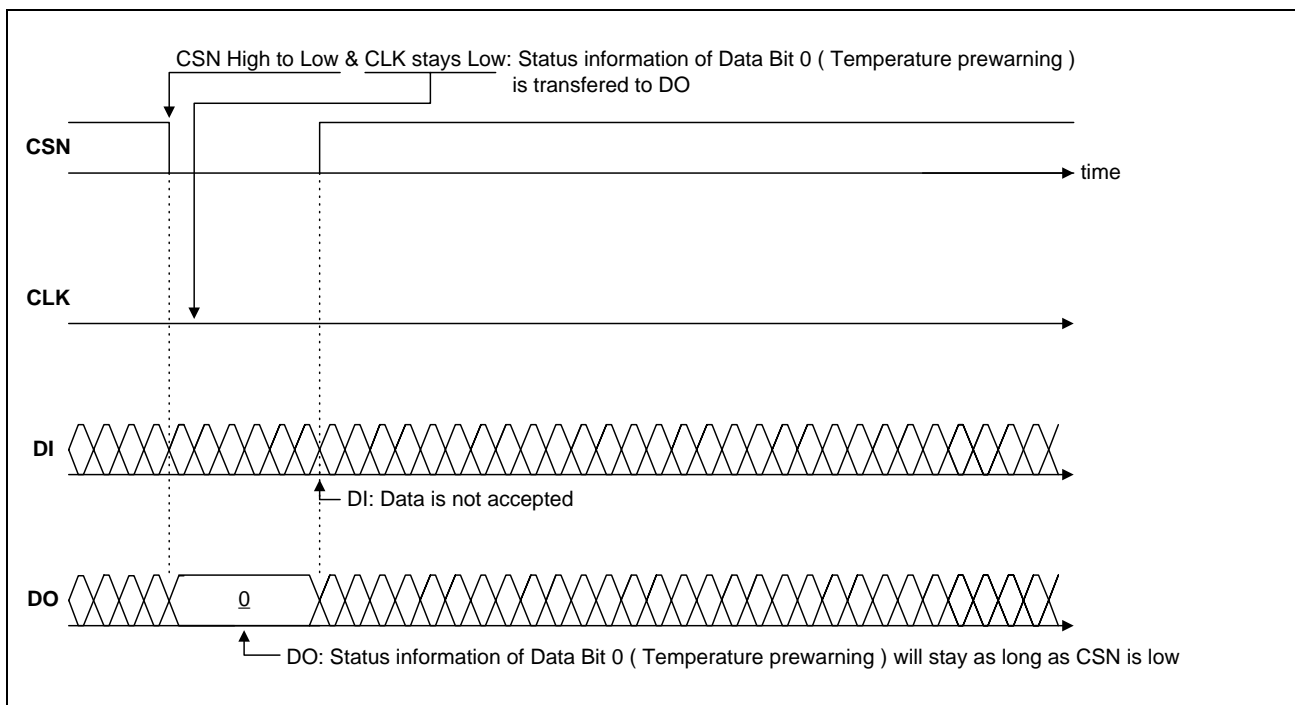
Thermal prewarning junction temperature	$T_{jPW}$	120	145	170	$^{\circ}\text{C}$	–
Temperature prewarning hysteresis	$\Delta T$	–	30	–	K	–
Thermal shutdown junction temperature	$T_{jSD}$	150	175	200	$^{\circ}\text{C}$	–
Thermal switch-on junction temperature	$T_{jSO}$	120	–	170	$^{\circ}\text{C}$	–
Temperature shutdown hysteresis	$\Delta T$	–	30	–	K	–
Ratio of SD to PW temperature	$T_{jSD} / T_{jPW}$	1.05	1.20	–	–	–

*Note: Temperatures are guaranteed by design*

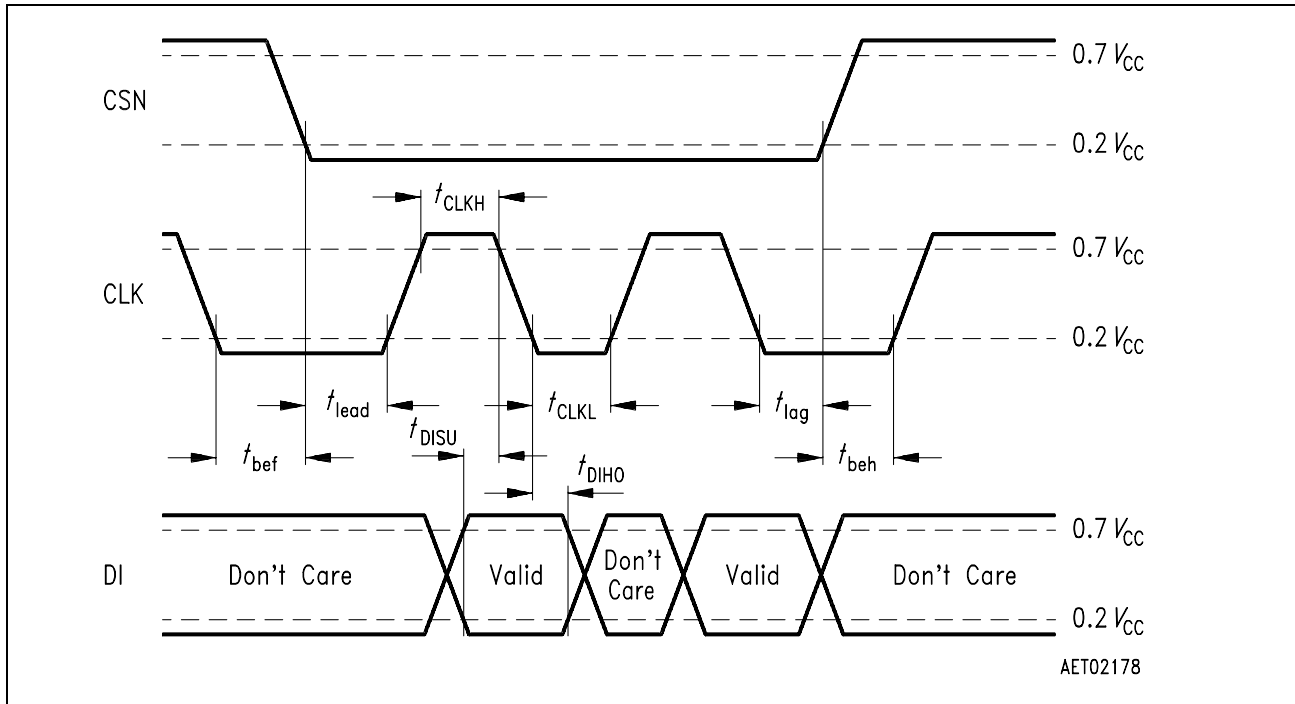
### 3 Timing Diagrams



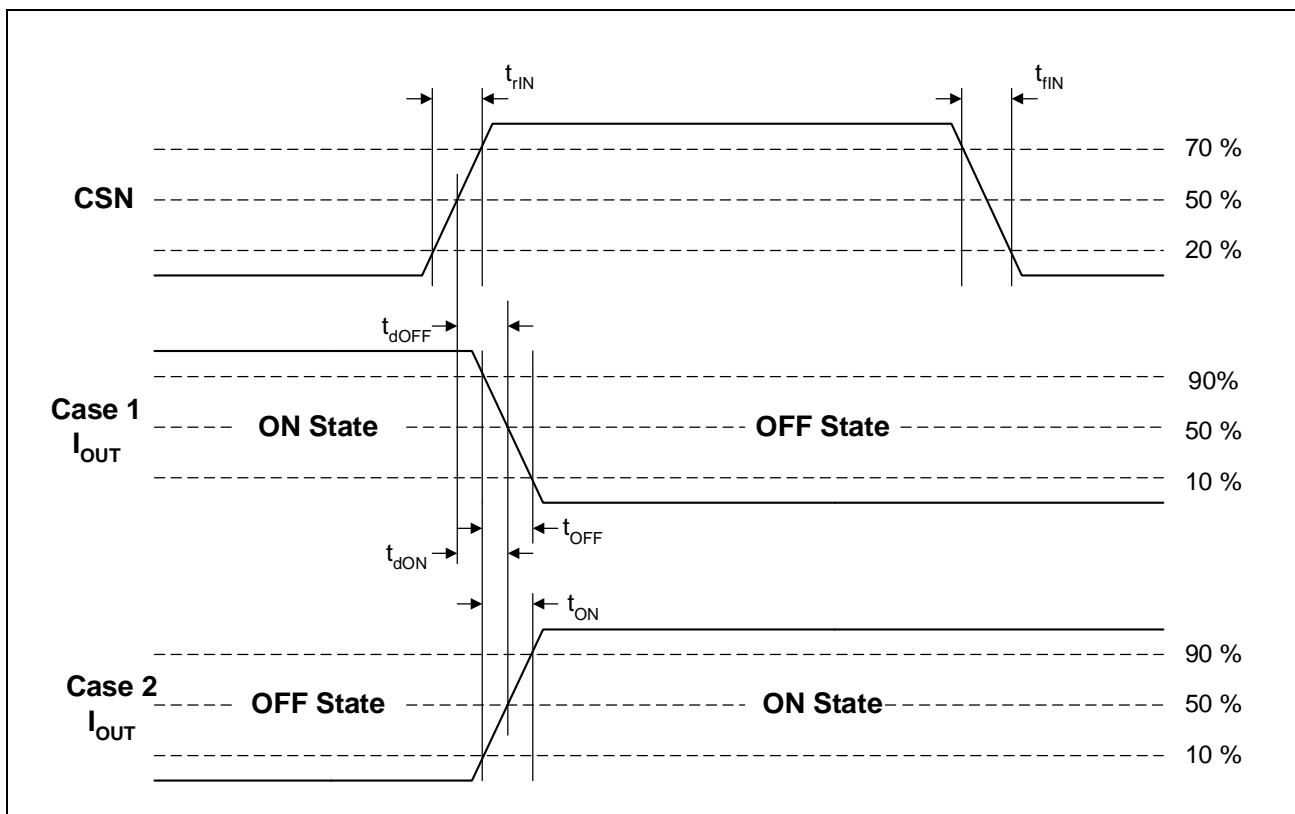
**Figure 4**  
**Standard Data Transfer Timing**



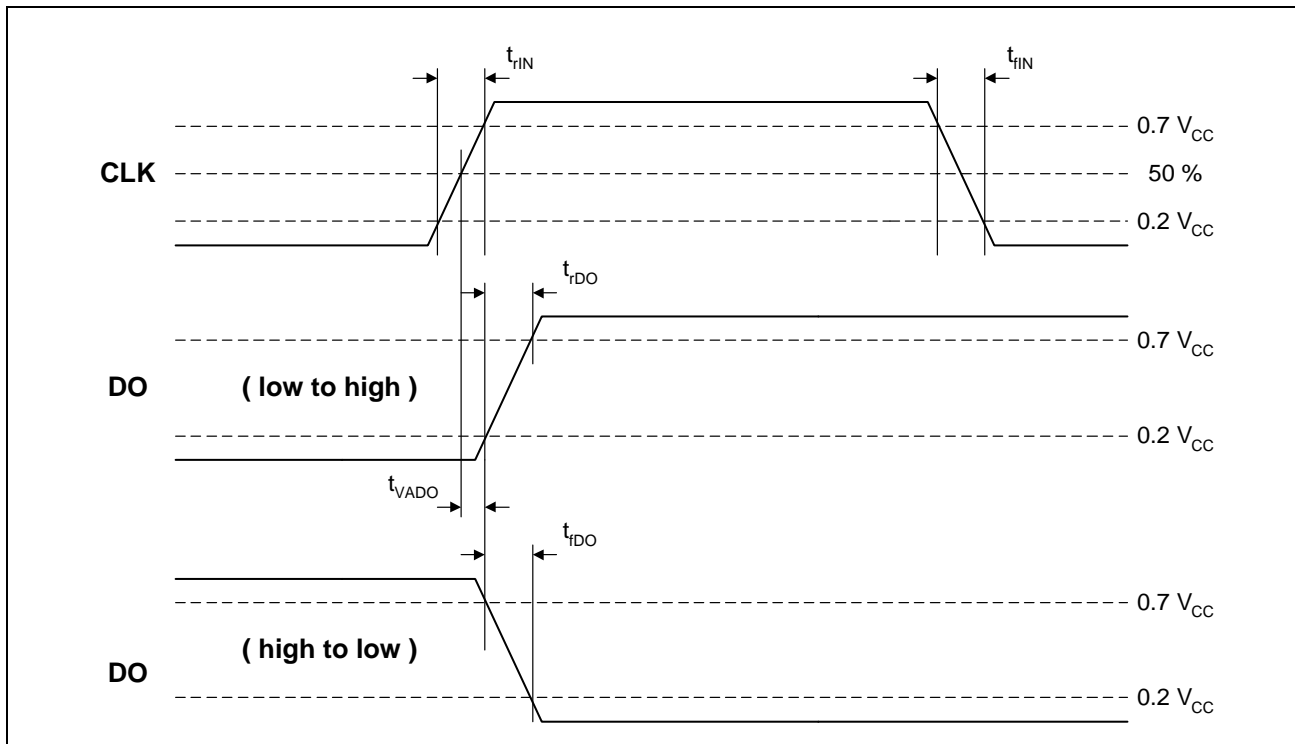
**Figure 5**  
**Timing for Temperature Prewarning only**



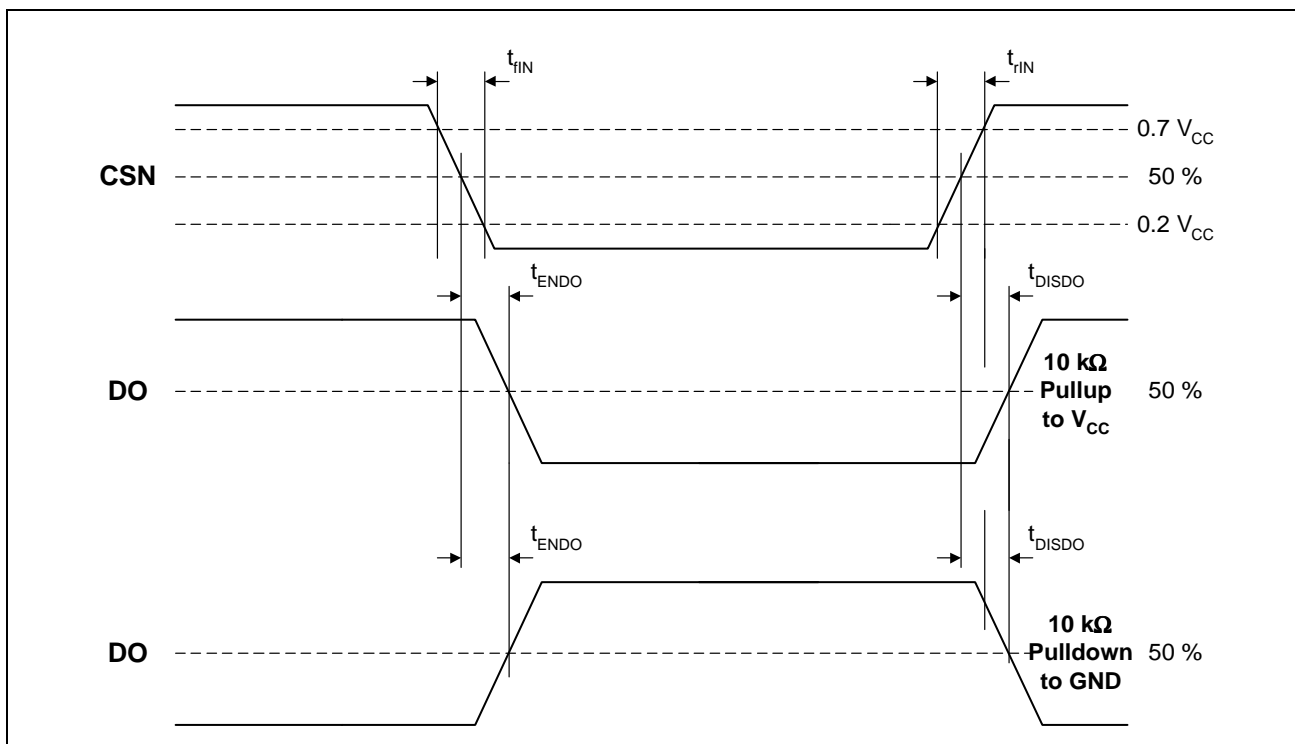
**Figure 6**  
**SPI-Input Timing**



**Figure 7**  
**Turn OFF/ON Time**

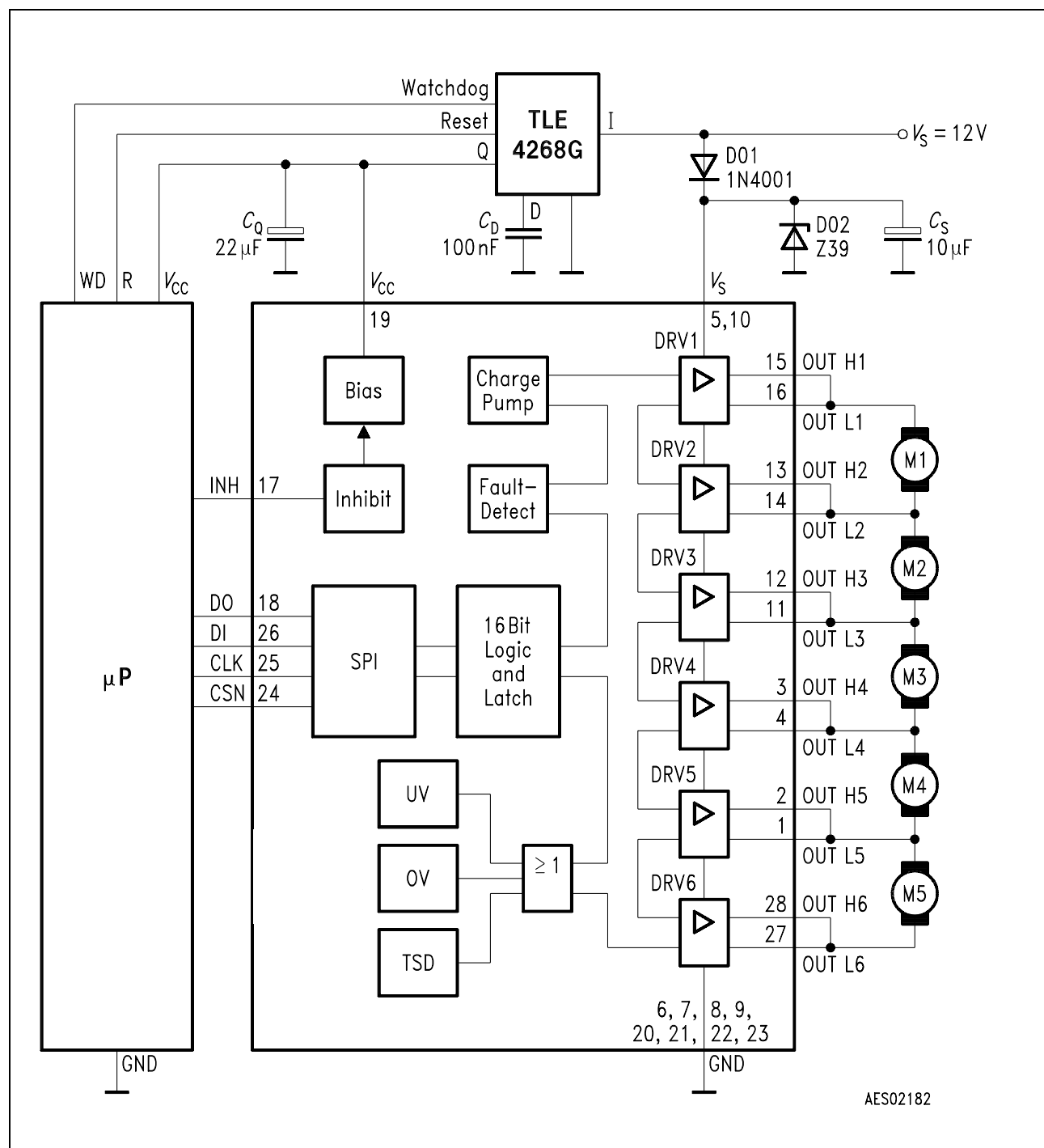


**Figure 8**  
**DO Valid Data Delay Time and Valid Time**



**Figure 9**  
**DO Enable and Disable Time**

## 4 Application

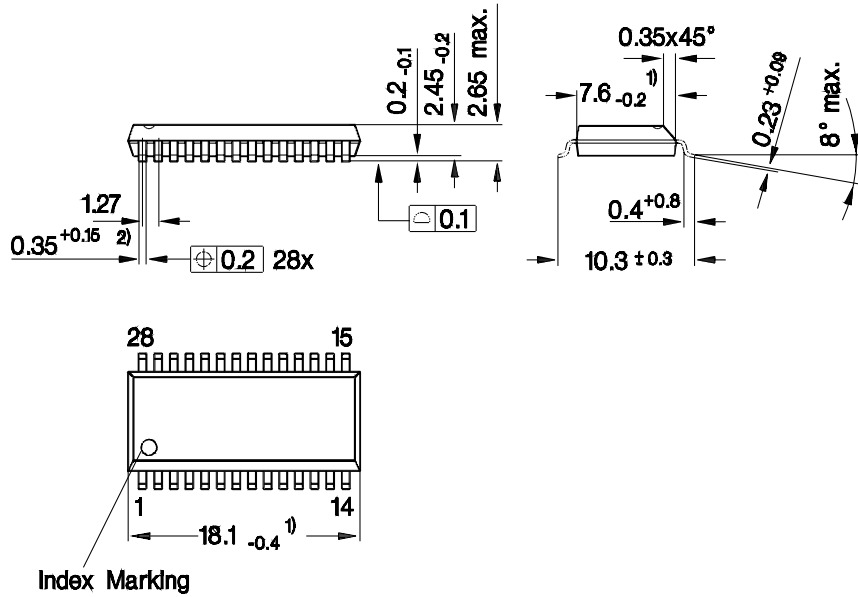


**Figure 10**  
**Application Circuit**

## 5 Package Outlines

### P-DSO-28-6

(Plastic Dual Small Outline Package)



- 1) Does not include plastic or metal protrusion of 0.15 max. per side
- 2) Does not include dambar protrusion

GPS05123

### Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm