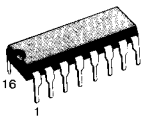
T54LS175
T74LS175

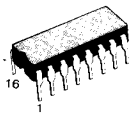
QUAD D FLIP-FLOP

DESCRIPTION

The LSTTL/MSI T54LS175/T74LS175 is a high speed Quad D Flip-Flop. The device is useful for general flip-flop requirements where clock anc clear inputs are common. The information on the D inputs is stored during the LOW to HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.
The LS175 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all SGS TTL families.



B1
Plastic Package



D1/D2
Ceramic Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:
T54LS175 D2
T74LS175 D1
T74LS175 B1
T74LS175 C1
T74LS175 M1

- EDGE-TRIGGERED D-TYPE INPUTS
- BUFFERED-POSITIVE EDGE TRIGGERED CLOCK
- ASYNCHRONOUS COMMON RESET
- TRUE AND COMPLEMENT OUTPUT
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

TRUTH TABLE

Inputs (t = n, $\overline{MR}$ = H)	Outputs (t = n + 1) Note 1	
D	Q	$\overline{Q}$
L	L	H
H	H	L

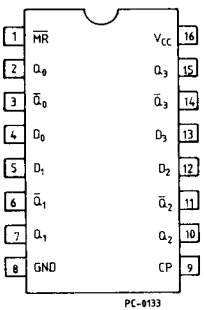
Note 1: t = n + 1 indicates conditions after next clock.

PIN NAMES

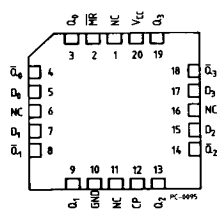
D_0-D_3	Data Input
CP	Clock (Active HIGH Going-Edge) Input
$\overline{MR}$	Master Reset (Active LOW) Input
Q_0-Q_3	True Outputs
$\overline{Q}_0$-$\overline{Q}_3$	Complemented Outputs

PIN CONNECTION
(top view)

DUAL IN LINE

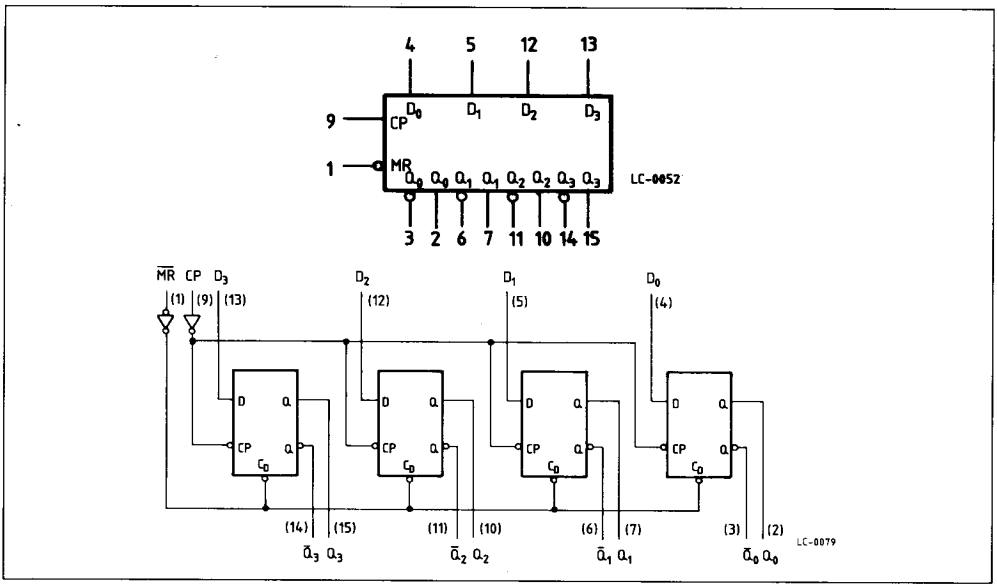


CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL AND LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 15	V
V_O	Output Voltage, Applied to Output	−0.5 to 10	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS175D2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS175XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

FUNCTIONAL DESCRIPTION

The LS175 consist of four edge-triggered D flip-flops with individual inputs and Q and $\overline{Q}$ outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW to HIGH Clock (CP) transition, causing individual Q and $\overline{Q}$ outputs to follow. A LOW input on the Master Reset ($\overline{MR}$) will force all Q outputs LOW and $\overline{Q}$ outputs HIGH indipendent of Clock or Data inputs.

The LS175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Test Conditions (Note 1)	Units
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Threshold Voltage for all Inputs	V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Threshold Voltage for all Inputs	V
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V_{CC} = MIN, I_{IN} = −18mA	V
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V_{CC} = MIN, I_{OH} = −400μA, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 4.0mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74		0.35	0.5	I_{OL} = 8.0mA	
I_{IH}	Input HIGH Current				20 0.1	V_{CC} = MAX, V_{IN} = 2.7V V_{CC} = MAX, V_{IN} = 7.0V	μA mA
I_{IL}	Input LOW Current				−0.4	V_{CC} = MAX, V_{IN} = 0.4V	mA
I_{OS}	Output Short Circuit Current (Note 2)		−20		−100	V_{CC} = MAX, V_{OUT} = 0V	mA
I_{CC}	Power Supply Current			11	18	V_{CC} = MAX	mA

AC CHARACTERISTICS: T_A = 25°C

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Test Conditions		Units
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		13 16	25 25	Fig. 1		ns
t_{PLH}	Propagation Delay, $\overline{MR}$ to Q Output		20	30	Fig. 2		ns
t_{PLH}	Propagation Delay, MR to $\overline{Q}$ Output		20	30	Fig. 2		ns
f_{MAX}	Maximum Input Clock Frequency	30	40		Fig. 1		MHz

Notes:

1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2) Not more than one output should be shorted at a time.
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

AC SET-UP REQUIREMENTS: $T_A = 25°C$

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
$t_{W(CP)}$	Clock Pulse Width	20			Fig. 1	ns
t_s	Set-up Time, Data to Clock	20			Fig. 1	ns
t_h	Hold Time, Data to Clock (HIGH or LOW)	5			Fig. 1	ns
t_{rec}	Recovery Time for $\overline{MR}$	25			Fig. 2	ns
$t_{W(MR)}$	Minimum $\overline{MR}$ Pulse Width	20			Fig. 2	ns

AC WAVEFORMS

Fig. 1 - Clock to Output Delays, Clock Pulse Width, Frequency Set-up and Hold Times Data to Clock

* The shaded areas indicate when the input is permitted to change for predictable output performance

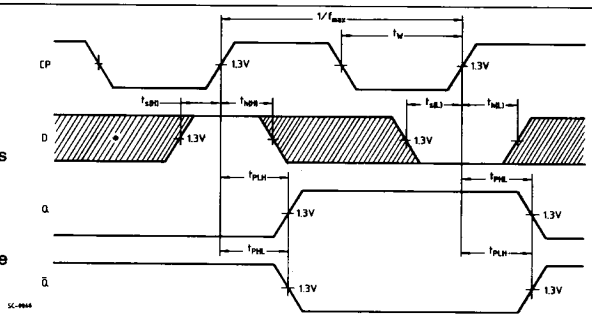
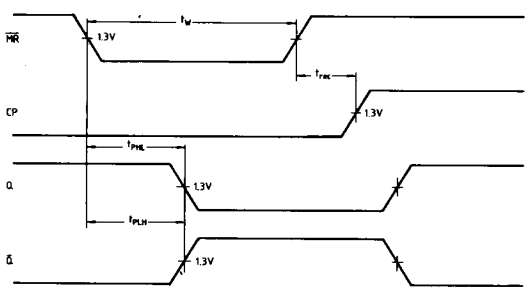


Fig. 2 - Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time



DEFINITION OF TERMS:

SET-UP TIME (t_s) - is defined as the minimum time required for the correct logic level to be present at the logic input prior the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.
HOLD TIME (t_h) - is defined as the minimum time following the clock transition from LOW to HIGH at which the logic level must be mantained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be relased prior to the clock transition from LOW to HIGH and still be recognized.
RECOVERY TIME (t_{rec}) - is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.