SCLS305A - JANUARY 1996 - REVISED MAY 1997

- High-Current 3-State Outputs Drive Bus Lines Directly or up to 15 LSTTL Loads
- Data Flow-Through Pinout (All Inputs on Opposite Side From Outputs)
- Package Options Include Plastic Small-Outline (DW), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

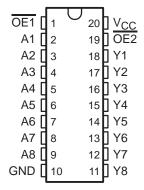
description

These octal buffers and line drivers feature the performance of the 'HC240 and a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout.

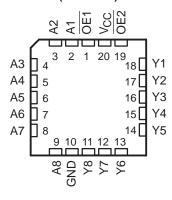
The 3-state control gate is a 2-input NOR. If either output-enable (OE1 or OE2) input is high, all eight outputs are in the high-impedance state. The 'HC541 provide true data at the outputs.

The SN54HC541 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC541 is characterized for operation from –40°C to 85°C.

SN54HC541 . . . J OR W PACKAGE SN74HC541 . . . DW, N, OR PW PACKAGE (TOP VIEW)



SN54HC541 . . . FK PACKAGE (TOP VIEW)



FUNCTION TABLE (each buffer/driver)

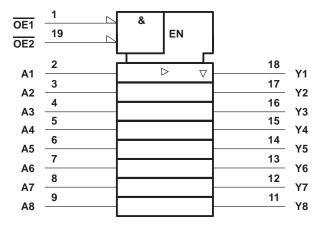
	OUTPUT		
OE1	OE2	Α	Y
L	L	L	L
L	L	Н	н
Н	X	Χ	Z
Х	Н	Χ	Z



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

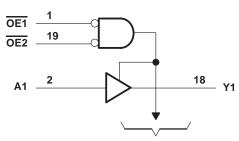


logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels

absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V _{CC}	0.5 V to 7 V
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC}) (see Note 1)	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC}) (see Note 1)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V _{CC} or GND	±70 mA
Package thermal impedance, θ _{JA} (see Note 2): DW package	97°C/W
N package	67°C/W
PW package	128°C/W
Storage temperature range, T _{stg}	. -65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.



recommended operating conditions

			SN	SN54HC541		SN74HC541			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNII
Vcc	Supply voltage		2	5	6	2	5	6	V
		V _{CC} = 2 V	1.5			1.5			
ViH	High-level input voltage	V _{CC} = 4.5 V	3.15			3.15			V
		V _{CC} = 6 V	4.2			4.2			
	Low-level input voltage	V _{CC} = 2 V	0		0.5	0		0.5	V
VIL		V _{CC} = 4.5 V	0		1.35	0		1.35	
		V _{CC} = 6 V	0		1.8	0		1.8	
٧ı	Input voltage		0		VCC	0		VCC	V
Vo	Output voltage		0		VCC	0		VCC	V
		V _{CC} = 2 V	0		1000	0		1000	
t _t	Input transition (rise and fall) time	$V_{CC} = 4.5 \text{ V}$	0		500	0		500	ns
		V _{CC} = 6 V	0		400	0		400	
TA	Operating free-air temperature		-55		125	-40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		\ \ \	Т	A = 25°C	;	SN54HC541		SN74HC541		
PARAMETER			VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V	1.9	1.998		1.9		1.9		
		I _{OH} = -20 μA	4.5 V	4.4	4.499		4.4		4.4		
Voн	VI = VIH or VIL		6 V	5.9	5.999		5.9		5.9		V
		I _{OH} = -6 mA	4.5 V	3.98	4.3		3.7		3.84		
		$I_{OH} = -7.8 \text{ mA}$	6 V	5.48	5.8		5.2		5.34		
	VI = VIH or VIL	I _{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	
			4.5 V		0.001	0.1		0.1		0.1	
VOL			6 V		0.001	0.1		0.1		0.1	V
		$I_{OL} = 6 \text{ mA}$	4.5 V		0.17	0.26		0.4		0.33	
		$I_{OL} = 7.8 \text{ mA}$	6 V		0.15	0.26		0.4		0.33	
lį	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
loz	$V_O = V_{CC}$ or 0		6 V		±0.01	±0.5		±10		±5	μΑ
Icc	$V_I = V_{CC}$ or 0,	I _O = 0	6 V			8		160		80	μΑ
Ci			2 V to 6 V		3	10		10		10	рF

SN54HC541, SN74HC541 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	V	T,	λ = 25°C	;	SN54H	C541	SN74H	IC541	UNIT		
PARAMETER	(INPUT)	(OUTPUT)	vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT		
			2 V		40	115		171		144			
^t pd	Α	Y	4.5 V		12	23		34		29	ns		
			6 V		10	20		29		25			
			2 V		80	150		224		188			
^t en	ŌĒ	Y	4.5 V		17	30		45		38	ns		
				6 V		15	26		38		32		
	ŌĒ	Y	2 V		40	150		224		188			
^t dis			Υ	4.5 V		18	30		45		38	ns	
			6 V		17	26		38		32			
t _t	Y		2 V		28	60		90		75			
			Υ	Υ	Y	4.5 V		8	12		18		15
			6 V		6	10		15		13			

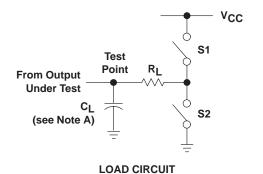
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	Vaa	T _A = 25°C			SN54F	IC541	SN74HC541					
PARAMETER	(INPUT)	(OUTPUT)	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT			
			2 V		65	165		246		206				
t _{pd}	А	Y	4.5 V		16	33		49		41	ns			
							6 V		14	28		42		35
	ŌĒ	Y	2 V		100	200		298		250				
t _{en}			Y	4.5 V		20	40		60		50	ns		
				6 V		17	34		51		43			
t _t		Y		Y	Y	2 V		45	210		315		265	
			Υ			4.5 V		17	42		63		53	ns
			6 V		13	36		53		45				

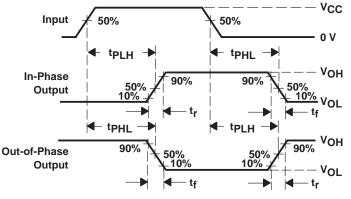
operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per buffer/driver	No load	35	pF

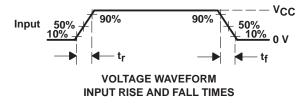
PARAMETER MEASUREMENT INFORMATION

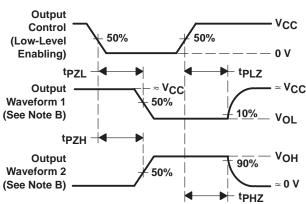


PARAI	PARAMETER		RL CL		S2	
	tPZH	1 k Ω	50 pF		Closed	
ten	tPZL	1 K22	or 150 pF	Closed	Open	
f.u	tPHZ	1 kΩ	50 pF	Open	Closed	
^t dis	tPLZ	1 K22	30 pr	Closed	Open	
t _{pd} or t _t		_	50 pF or 150 pF	Open	Open	



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES





VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

- NOTES: A. C_L includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



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