

SN54HC165, SN74HC165 8-BIT PARALLEL-LOAD SHIFT REGISTERS

SCLS116C – DECEMBER 1982 – REVISED MAY 1997

- Complementary Outputs
- Direct Overriding Load (Data) Inputs
- Gated Clock Inputs
- Parallel-to-Serial Data Conversion
- Package Options Include Plastic Small-Outline (D), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

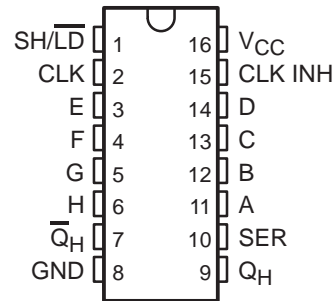
description

The 'HC165 are 8-bit parallel-load shift registers that, when clocked, shift the data toward a serial (Q_H) output. Parallel-in access to each stage is provided by eight individual direct data (A–H) inputs that are enabled by a low level at the shift/load (SH/\overline{LD}) input. The 'HC165 also feature a clock-inhibit (CLK INH) function and a complementary serial (\overline{Q}_H) output.

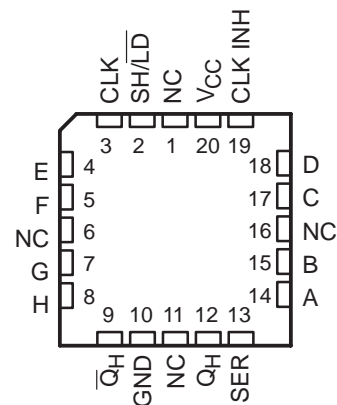
Clocking is accomplished by a low-to-high transition of the clock (CLK) input while SH/\overline{LD} is held high and CLK INH is held low. The functions of CLK and CLK INH are interchangeable. Since a low CLK and a low-to-high transition of CLK INH also accomplish clocking, CLK INH should be changed to the high level only while CLK is high. Parallel loading is inhibited when SH/\overline{LD} is held high. While SH/\overline{LD} is low, the parallel inputs to the register are enabled independently of the levels of the CLK, CLK INH, or serial (SER) inputs.

The SN54HC165 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HC165 is characterized for operation from -40°C to 85°C .

SN54HC165 . . . J OR W PACKAGE
SN74HC165 . . . D, N, OR PW PACKAGE
(TOP VIEW)



SN54HC165 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUTS			FUNCTION
SH/\overline{LD}	CLK	CLK INH	
L	X	X	Parallel load
H	H	X	No change
H	X	H	No change
H	L	↑	Shift†
H	↑	L	Shift†

† Shift = content of each internal register shifts toward serial output Q_H . Data at SER is shifted into the first register.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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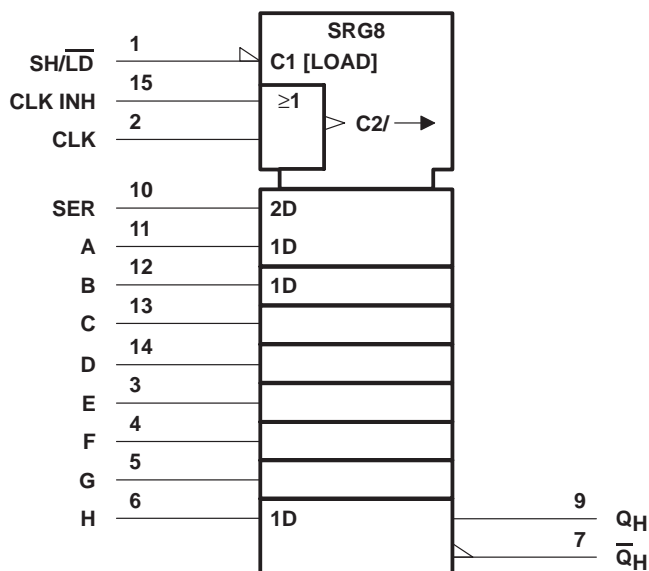
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SN54HC165, SN74HC165

8-BIT PARALLEL-LOAD SHIFT REGISTERS

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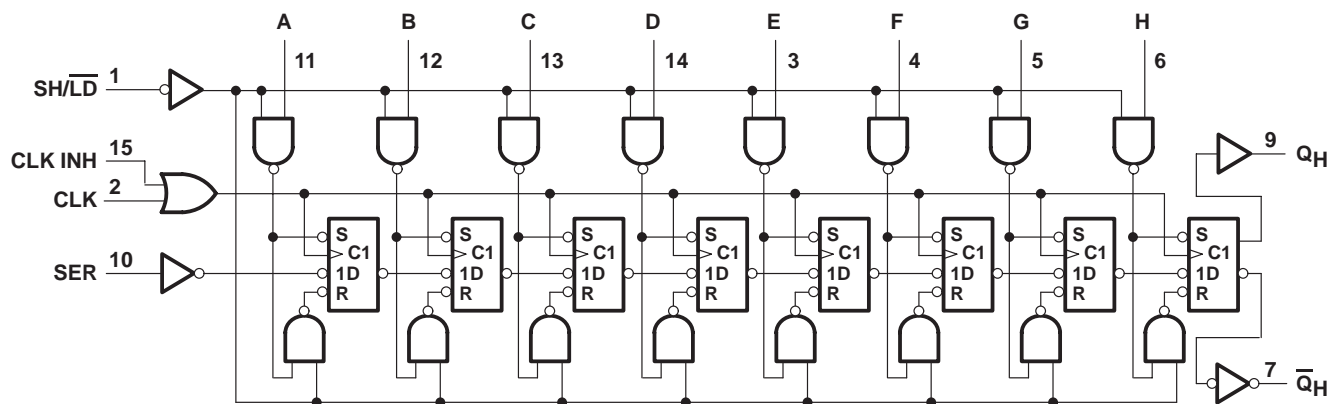
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

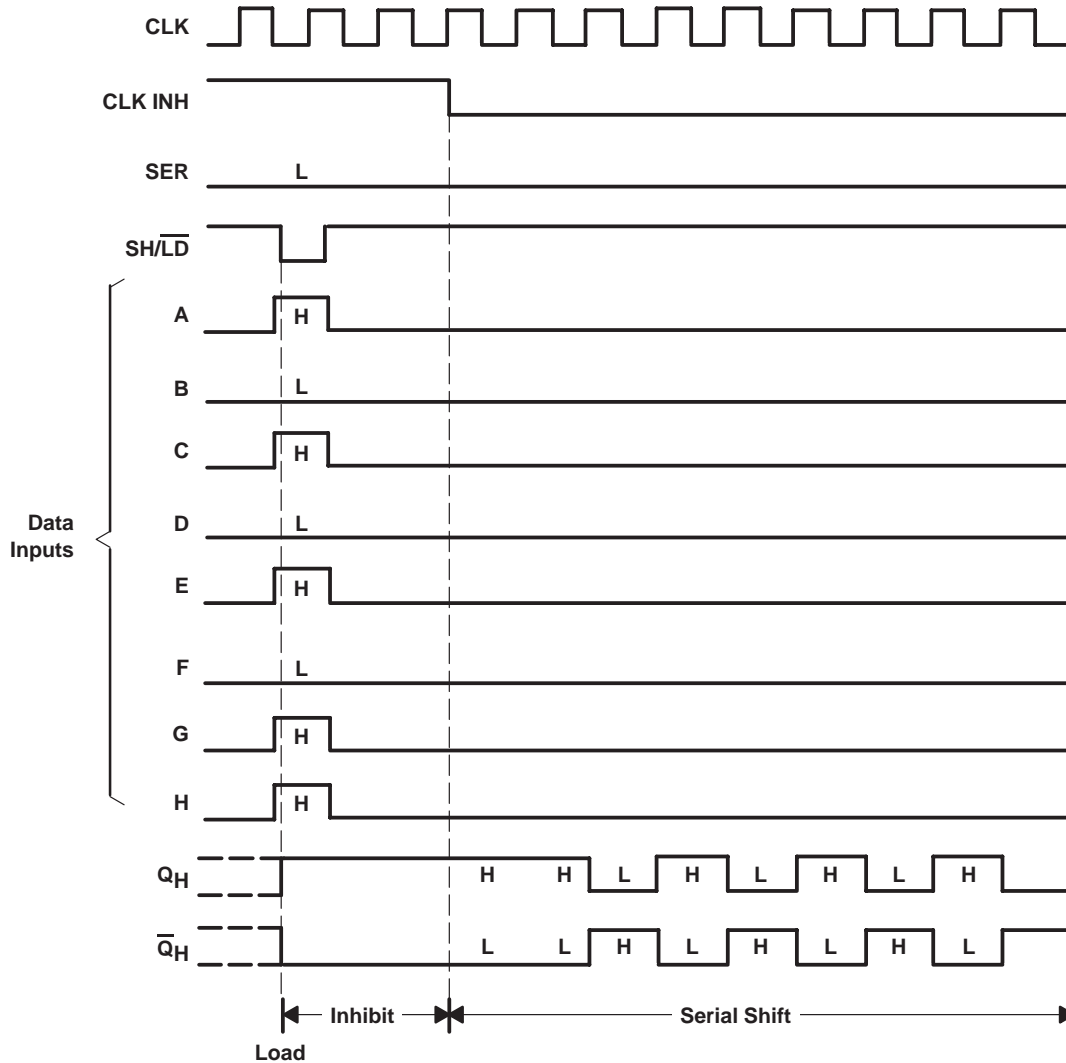
Pin numbers shown are for the D, J, N, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, PW, and W packages.

typical shift, load, and inhibit sequence



absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	113°C/W
N package	78°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

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recommended operating conditions

			SN54HC165			SN74HC165			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		2	5	6	2	5	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5			1.5			V
		V _{CC} = 4.5 V	3.15			3.15			
		V _{CC} = 6 V	4.2			4.2			
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0			0			V
		V _{CC} = 4.5 V	0			1.35			
		V _{CC} = 6 V	0			1.8			
V _I	Input voltage		0		V _{CC}	0		V _{CC}	V
V _O	Output voltage		0		V _{CC}	0		V _{CC}	V
t _t [†]	Input transition (rise and fall) time	V _{CC} = 2 V	0		1000	0		1000	ns
		V _{CC} = 4.5 V	0		500	0		500	
		V _{CC} = 6 V	0		400	0		400	
T _A	Operating free-air temperature		−55		125	−40		85	°C

[†] If this device is used in the threshold region (from $V_{IL\text{max}} = 0.5\text{ V}$ to $V_{IH\text{min}} = 1.5\text{ V}$), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at $t_t = 1000\text{ ns}$ and $V_{CC} = 2\text{ V}$ does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC165		SN74HC165		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}\text{ or }V_{IL}$	$I_{OH} = -20\text{ }\mu\text{A}$	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		$I_{OH} = -4\text{ mA}$	4.5 V	3.98	4.3		3.7		3.84		
		$I_{OH} = -5.2\text{ mA}$	6 V	5.48	5.8		5.2		5.34		
V_{OL}	$V_I = V_{IH}\text{ or }V_{IL}$	$I_{OL} = 20\text{ }\mu\text{A}$	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		$I_{OL} = 4\text{ mA}$	4.5 V		0.17	0.26		0.4		0.33	
		$I_{OL} = 5.2\text{ mA}$	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}\text{ or }0$		6 V		± 0.1	± 100		± 1000		± 1000	nA
I_{CC}	$V_I = V_{CC}\text{ or }0, I_O = 0$		6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V _{CC}	T _A = 25°C		SN54HC165		SN74HC165		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	2 V	0	6	0	4.2	0	5	MHz
		4.5 V	0	31	0	21	0	25	
		6 V	0	36	0	25	0	29	
t _w	SH/ $\overline{\text{LD}}$ low	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
	CLK high or low	2 V	80		120		100		
		4.5 V	16		24		20		
		6 V	14		20		17		
t _{su}	SH/ $\overline{\text{LD}}$ high before CLK \uparrow	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
	SER before CLK \uparrow	2 V	40		60		50		
		4.5 V	8		12		10		
		6 V	7		10		9		
	CLK INH low before CLK \uparrow	2 V	100		150		125		
		4.5 V	20		30		25		
		6 V	17		25		21		
	CLK INH high before CLK \uparrow	2 V	40		60		50		
		4.5 V	8		12		10		
		6 V	7		10		9		
t _h	SER data after CLK \uparrow	2 V	5		5		5		ns
		4.5 V	5		5		5		
		6 V	5		5		5		
	PAR data after SH/ $\overline{\text{LD}}$ \downarrow	2 V	5		5		5		
		4.5 V	5		5		5		
		6 V	5		5		5		

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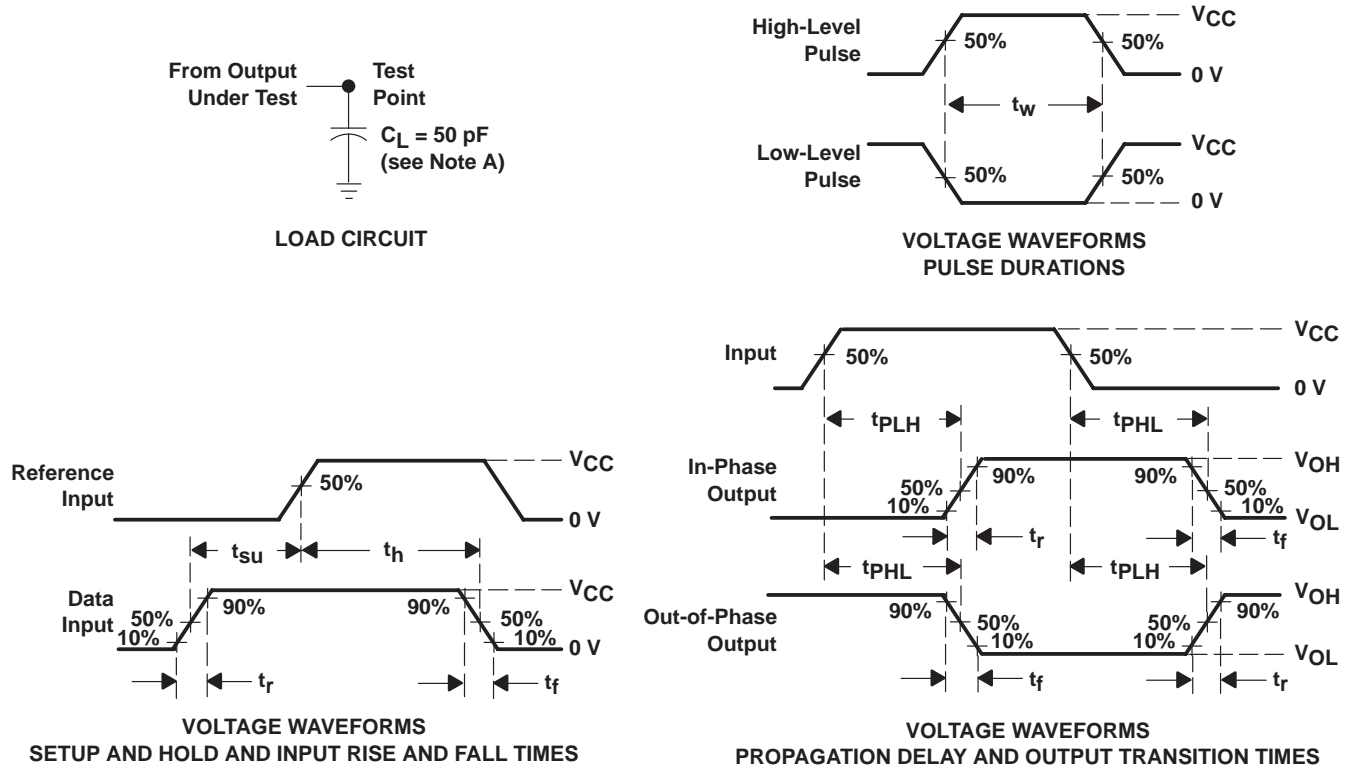
switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC165		SN74HC165		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{\max}			2 V	6	13		4.2		5		MHz
			4.5 V	31	50		21		25		
			6 V	36	62		25		29		
t_{pd}	SH/ \overline{LD}	Q_H or \overline{Q}_H	2 V		80	150		225		190	ns
			4.5 V		20	30		45		38	
			6 V		16	26		38		32	
	CLK	Q_H or \overline{Q}_H	2 V		75	150		225		190	
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
	H	Q_H or \overline{Q}_H	2 V		75	150		225		190	
			4.5 V		15	30		45		38	
			6 V		13	26		38		32	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	75	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 - C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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