Burr-Brown Products
from Texas Instruments

PCM1753
PCM1754
PCM1755

SLES092 − OCTOBER 2003

24-BIT, 192 kHz SAMPLING ENHANCED MULTI-LEVEL, DELTA-SIGMA, AUDIO DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **24-Bit Resolution**
- **Analog Performance (V_{CC} = 5 V):**
  - **Dynamic Range: 106 dB**
  - **SNR: 106 dB, Typical**
  - **THD+N: 0.002%, Typical**
  - **Full-Scale Output: 4 V p-p, Typical**
- **4×/8× Oversampling Digital Filter:**
  - **Stop-Band Attenuation: −50 dB**
  - **Pass-Band Ripple: ±0.04 dB**
- **Sampling Frequency: 5 kHz to 200 kHz**
- **System Clock: 128 f_S, 192 f_S, 256 f_S, 384 f_S, 512 f_S, 768 f_S, 1152 f_S With Auto Detect**
- **Software Control (PCM1753, PCM1755):**
  - **Accepts 16-, 18-, 20-, and 24-Bit Audio Formats: Standard, I²S, and Left-Justified**
  - **Digital Attenuation: 0 dB to −63 dB, 0.5 dB/Step**
  - **Digital De-Emphasis**
  - **Digital Filter Rolloff: Sharp or Slow**
  - **Soft Mute**
  - **Zero Flags for Each Output**
  - **Open-Drain Output Zero Flag (PCM1755)**
- **Hardware Control (PCM1754):**
  - **I²S and 16-Bit Word, Right-Justified**
  - **44.1 kHz Digital De-Emphasis**
  - **Soft Mute**
  - **Zero Flag for L-, R-Channel Common Output**
- **Power Supply: 5-V Single Supply**
- **Small 16-Lead SSOP Package, Lead-Free**

APPLICATIONS

- **A/V Receivers**
- **DVD Movie Players**
- **DVD Add-On Cards For High-End PCs**
- **DVD Audio Players**
- **HDTV Receivers**
- **Car Audio Systems**
- **Other Applications Requiring 24-Bit Audio**

DESCRIPTION

The PCM1753/54/55 is a CMOS, monolithic, integrated circuit, which includes stereo digital-to-analog converters and support circuitry in a small 16-lead SSOP package. The data converters use TI’s enhanced multilevel delta-sigma architecture, which employs 4th-order noise shaping and 8-level amplitude quantization to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1753/54/55 accepts industry-standard audio data formats with 16- to 24-bit data, providing easy interfacing to audio DSP and decoder chips. Sampling rates up to 200 kHz are supported. A full set of user-programmable functions is accessible through a three-wire serial control port, which supports register write functions.

The PCM1753/55 is pin compatible with the PCM1748, PCM1742, and PCM1741, except for pin 5.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE CODE	OPERATION TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(1)	TRANSPORT MEDIA
PCM1753DBQ	16-pin SSOP	16DBQ	−25°C to 85°C	PCM1753	PCM1753DBQ	Tube
					PCM1753DBQR	Tape and reel
PCM1754DBQ	16-pin SSOP	16DBQ	−40°C to 85°C	PCM1754	PCM1754DBQ	Tube
					PCM1754DBQR	Tape and reel
PCM1755DBQ	16-pin SSOP	16DBQ	−25°C to 85°C	PCM1755	PCM1755DBQ	Tube
					PCM1755DBQR	Tape and reel

(1) For the most current specification and package information, refer to our web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	UNIT
Supply voltage: V_{CC}	−0.3 V to 6.5 V
Ground voltage differences: AGND, DGND	±0.1 V
Input voltage	−0.3 V to 6.5 V
Input current (any pins except supplies)	±10 mA
Ambient temperature under bias	−40°C to 125°C
Storage temperature	−55°C to 150°C
Junction temperature	150°C
Lead temperature (soldering)	260°C, 5 s
Package temperature (IR reflow, peak)	260°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 44.1 kHz, system clock = 384 f_S and 24-bit data, unless otherwise noted

	PARAMETER		TEST CONDITIONS	PCM1753DBQ, PCM1754DBQ, PCM1755DBQ MIN	TYP	MAX	UNIT
	Resolution				24		Bits
DATA FORMAT							
	Audio-data interface format	PCM1753 PCM1755			Standard, I^2S, left-justified		
		PCM1754			I^2S, standard		
	Audio-data bit length	PCM1753 PCM1755			16-, 18-, 20-, 24-bit, selectable		
		PCM1754			16−24-bit (I^2S), 16-bit (standard)		
	Audio data format				MSB first, 2s complement		
f_S	Sampling frequency			5		200	kHz
	System clock frequency				128 f_S, 192 f_S, 256 f_S, 384 f_S, 512 f_S, 768 f_S, 1152 f_S		

ELECTRICAL CHARACTERISTICS CONTINUED

All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 44.1 kHz, system clock = 384 f_S and 24-bit data, unless otherwise noted

	PARAMETER	TEST CONDITIONS	PCM1753DBQ, PCM1754DBQ, PCM1755DBQ MIN	TYP	MAX	UNIT
DIGITAL INPUT/OUTPUT						
	Logic family			TTL compatible		
V_{IH}	Input logic level		2.0			VDC
V_{IL}	Input logic level				0.8	VDC
I_{IH} (1)	Input logic current	$V_{IN} = V_{CC}$			10	µA
I_{IL} (1)	Input logic current	V_{IN} = 0 V			−10	µA
I_{IH} (2)	Input logic current	$V_{IN} = V_{CC}$		65	100	µA
I_{IL} (2)	Input logic current	V_{IN} = 0 V			−10	µA
V_{OH} (3)	Output logic level	I_{OH} = −1 mA	2.4			VDC
V_{OL} (4)	Output logic level	I_{OL} = 1 mA			0.4	VDC
DYNAMIC PERFORMANCE (5) (6)						
	THD+N at V_{OUT} = 0 dB	f_S = 44.1 kHz		0.002%	0.006%	
		f_S = 96 kHz		0.003%		
		f_S = 192 kHz		0.004%		
	THD+N at V_{OUT} = −60 dB	f_S = 44.1 kHz		0.65%		
		f_S = 96 kHz		0.8%		
		f_S=192 kHz		0.95%		
	Dynamic range	EIAJ, A-weighted, f_S = 44.1 kHz	100	106		dB
		A-weighted, f_S = 96 kHz		104		
		A-weighted, f_S = 192 kHz		102		
	Signal-to-noise ratio	EIAJ, A-weighted, f_S = 44.1 kHz	100	106		dB
		A-weighted, f_S = 96 kHz		104		
		A-weighted, f_S = 192 kHz		102		
	Channel separation	f_S = 44.1 kHz	97	103		dB
		f_S = 96 kHz		101		
		f_S =192 kHz		100		
	Level linearity error	V_{OUT} = −90 dB		±0.5		dB
DC ACCURACY						
	Gain error			±1	±6	% of FSR
	Gain mismatch, channel-to-channel			±1	±3	% of FSR
	Bipolar zero error	V_{OUT} = 0.5 V_{CC} at BPZ		±30	±60	mV
ANALOG OUTPUT						
	Output voltage	Full scale (−0 dB)		80% of V_{CC}		Vp-p
	Center voltage			50% of V_{CC}		VDC
	Load impedance	AC-coupled load	5			kΩ
DIGITAL FILTER PERFORMANCE						
FILTER CHARACTERISTICS (SHARP ROLLOFF)						
	Pass band	±0.04 dB			0.454 f_S	
	Stop band		0.546 f_S			
	Pass-band ripple			0.04		dB
	Stop-band attenuation	Stop band = 0.546 f_S	−50			dB

ELECTRICAL CHARACTERISTICS CONTINUED

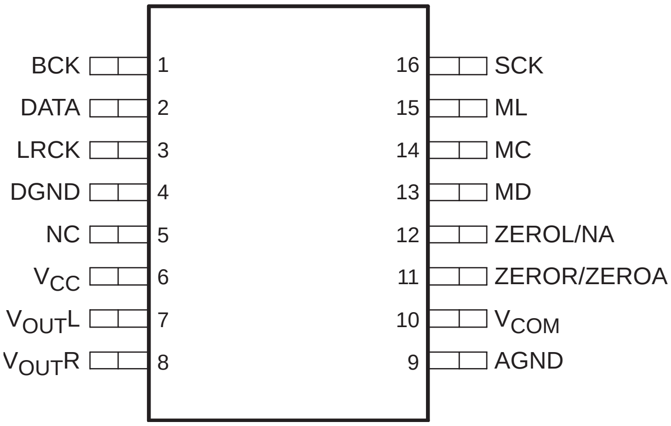
All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 44.1 kHz, system clock = 384 f_S and 24-bit data, unless otherwise noted

PARAMETER			TEST CONDITIONS	PCM1753DBQ, PCM1754DBQ, PCM1755DBQ			UNIT
				MIN	TYP	MAX	
FILTER CHARACTERISTICS (SLOW ROLL OFF, PCM1753/PCM1755)							
	Pass band		±0.5 dB			0.198 f_S	
	Stop band			0.884 f_S			
	Pass-band ripple					±0.5	dB
	Stop-band attenuation		Stop band = 0.884 f_S	−35			dB
	Delay time				20/f_S		s
	De-emphasis error				±0.1		dB
ANALOG FILTER PERFORMANCE							
	Frequency response		At 20 kHz		−0.03		dB
			At 44 kHz		−0.20		dB
POWER SUPPLY REQUIREMENTS (6)							
V_{CC}	Voltage range			4.5	5.0	5.5	VDC
I_{CC}	Supply current		f_S = 44.1 kHz		16	21	mA
			f_S = 96 kHz		25		
			f_S = 192 kHz		30		
	Power dissipation		f_S = 44.1 kHz		80	105	mW
			f_S = 96 kHz		125		
			f_S = 192 kHz		150		
TEMPERATURE RANGE							
	Operation temperature	PCM1753 PCM1755		−25		85	°C
		PCM1754		−40		85	°C
θ_{JA}	Thermal resistance		16-pin SSOP		115		°C/W

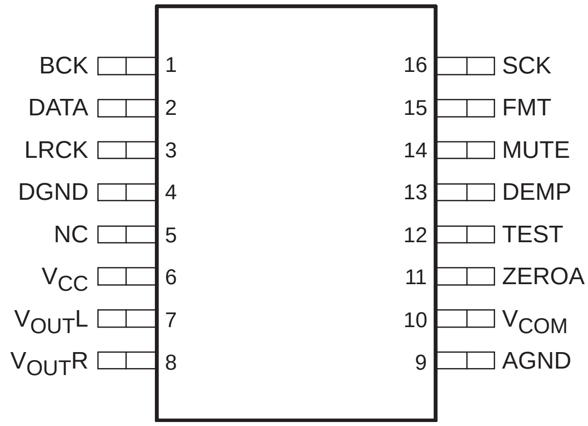
(1) Pins 16, 1, 2, 3: SCK, BCK, DATA, LRCK.
(2) Pins 13−15: MD, MC, ML (PCM1753/PCM1755). Pins 12−15: TEST, DEMP, MUTE, FMT (PCM1754).
(3) Pins 11, 12: ZEROR, ZEROL (PCM1753). Pin 11: ZEROA (PCM1754).
(4) Pins 11, 12: ZEROR, ZEROL (PCM1753/PCM1755). Pin 11: ZEROA (PCM1754).
(5) Analog performance specifications are measured using the System Two™ Cascade audio measurement system by Audio Precision™ in the averaging mode.
(6) Conditions in 192-kHz operation are system clock = 128 f_S and oversampling rate = 64 f_S of register 18.

PIN ASSIGNMENTS

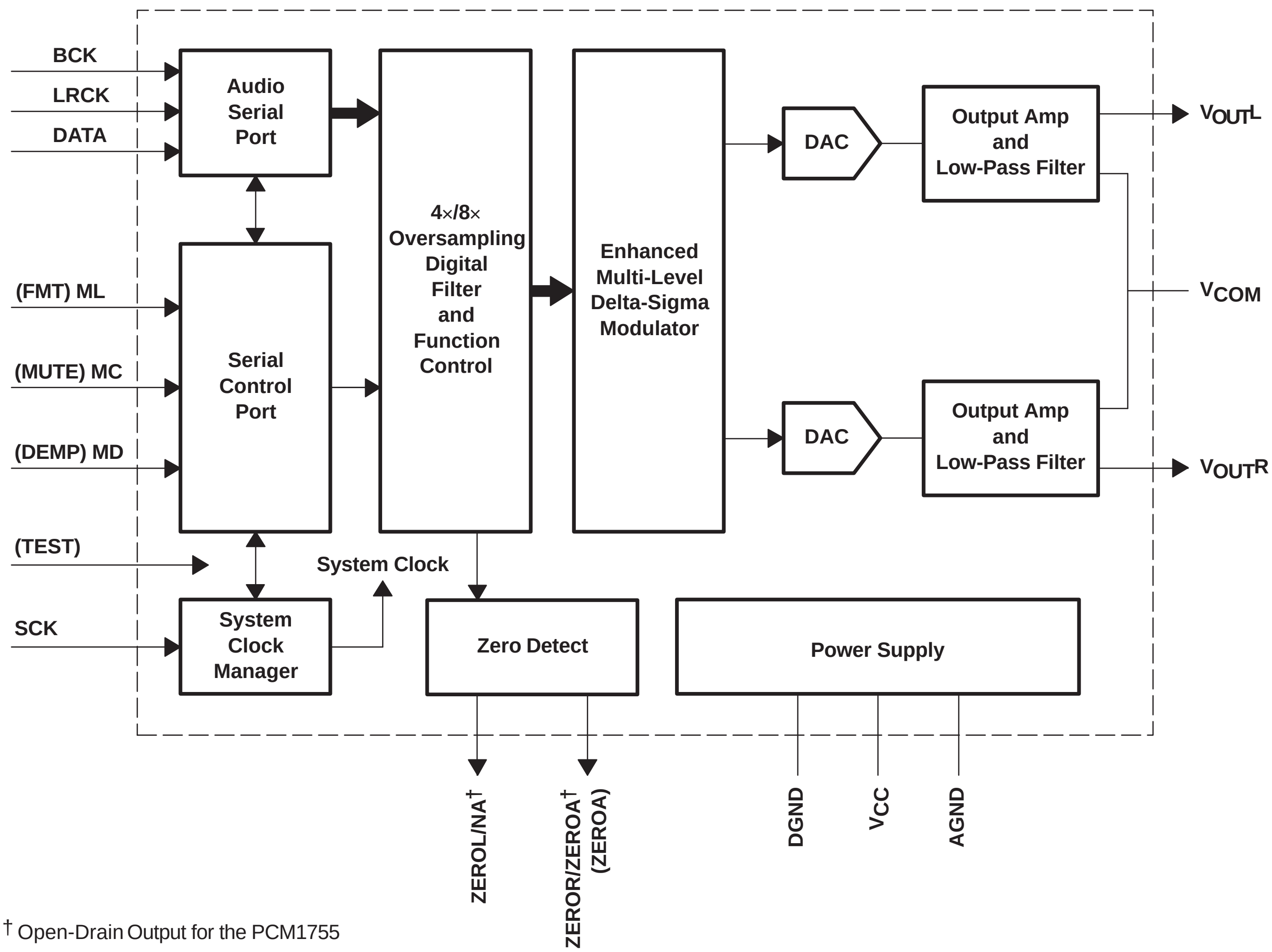
PCM1753/PCM1755
(TOP VIEW)



PCM1754
(TOP VIEW)



FUNCTIONAL BLOCK DIAGRAM



† Open-Drain Output for the PCM1755

( ): PCM1754

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
PCM1753/PCM1755			
AGND	9	−	Analog ground
BCK	1	I	Audio data bit clock input
DATA	2	I	Audio data digital input
DGND	4	−	Digital ground
LRCK	3	I	L-channel and R-channel audio data latch enable input
MC	14	I	Mode control clock input(1)
MD	13	I	Mode control data input (1)
ML	15	I	Mode control latch input (1)
NC	5	−	
SCK	16	I	System clock input
V_{CC}	6	−	Analog power supply, 5 V
V_{COM}	10	−	Common voltage decoupling
$V_{OUT}L$	7	O	Analog output for L-channel
$V_{OUT}R$	8	O	Analog output for R-channel
ZEROR/ZEROA	11	O	Zero flag output for R-channel/Zero flag output for L-/R-channels (2)
ZEROL/NA	12	O	Zero flag output for L-channel/Not assigned (2)
PCM1754			
AGND	9	−	Analog ground
BCK	1	I	Audio data bit clock input
DATA	2	I	Audio data digital input
DEMP	13	I	De-emphasis control (1)
DGND	4	−	Digital ground
FMT	15	I	Data format select (1)
LRCK	3	I	L-channel and R-channel audio data latch enable input
MUTE	14	I	Analog mixing control (1)
NC	5	−	
SCK	16	I	System clock input
TEST	12	I	Test pin. Ground or open (1)
V_{CC}	6	−	Analog power supply, 5 V
V_{COM}	10	−	Common voltage decoupling
$V_{OUT}L$	7	O	Analog output for L-channel
$V_{OUT}R$	8	O	Analog output for R-channel
ZEROA	11	O	Zero flag output for L/R channels

(1) Schmitt-trigger input with internal pulldown.
(2) Open-drain output (PCM1755).

TYPICAL PERFORMANCE CURVES

DIGITAL FILTER (DE-EMPHASIS OFF)

AMPLITUDE
vs
FREQUENCY

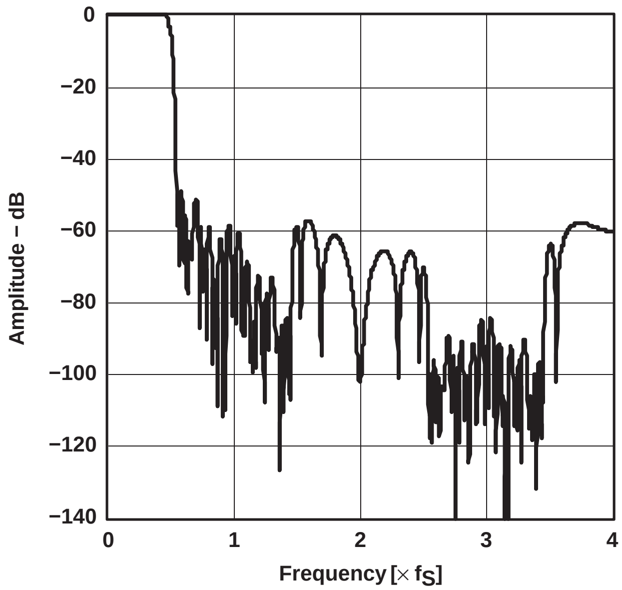


Figure 1. Frequency Response, Sharp Rolloff

AMPLITUDE
vs
FREQUENCY

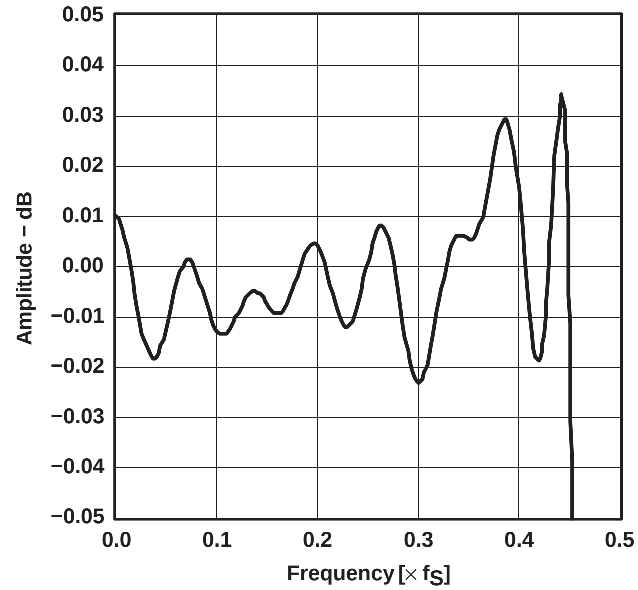


Figure 2. Pass-Band Ripple, Sharp Rolloff

AMPLITUDE
vs
FREQUENCY

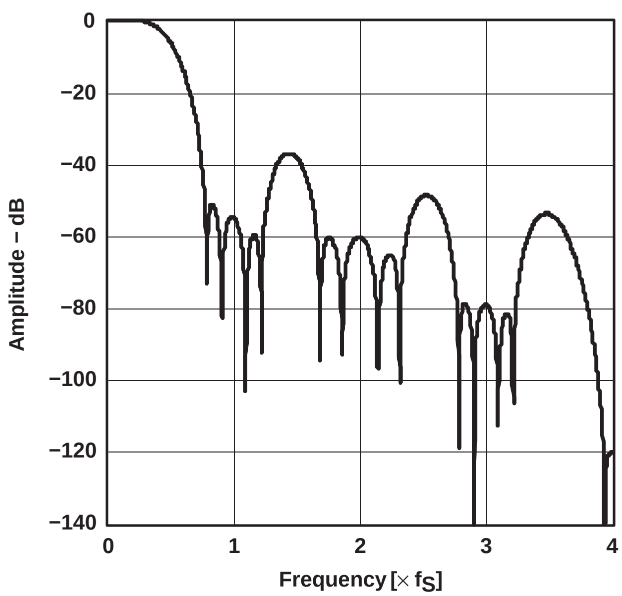


Figure 3. Frequency Response, Slow Rolloff

AMPLITUDE
vs
FREQUENCY

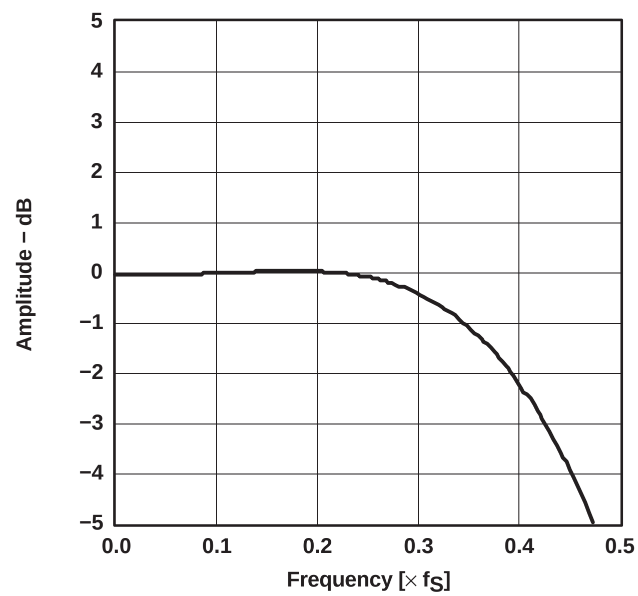


Figure 4. Transition Characteristics, Slow Rolloff

(1) All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit data, unless otherwise noted

DE-EMPHASIS CURVES

DE-EMPHASIS LEVEL vs FREQUENCY

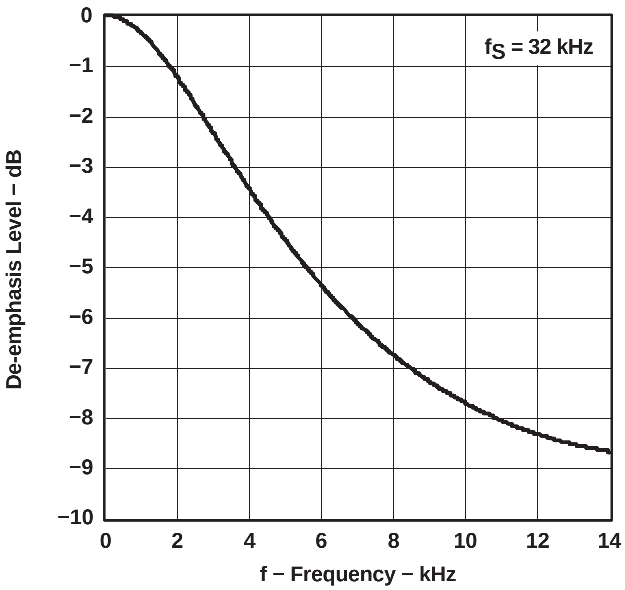


Figure 5

DE-EMPHASIS ERROR vs FREQUENCY

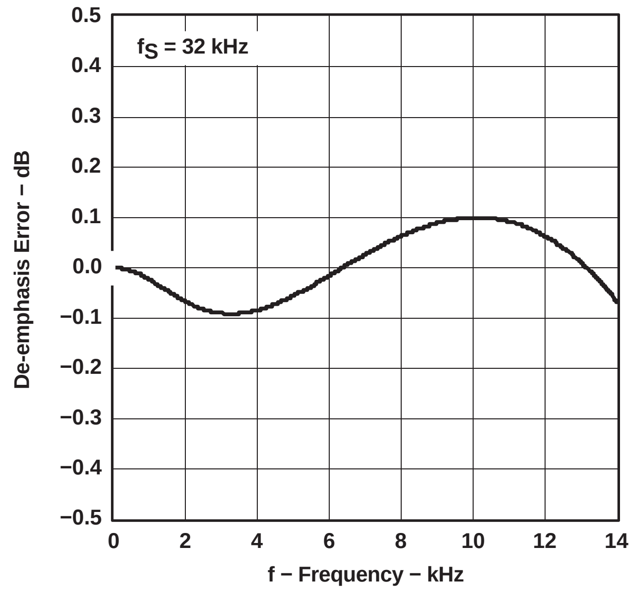


Figure 6

DE-EMPHASIS LEVEL vs FREQUENCY

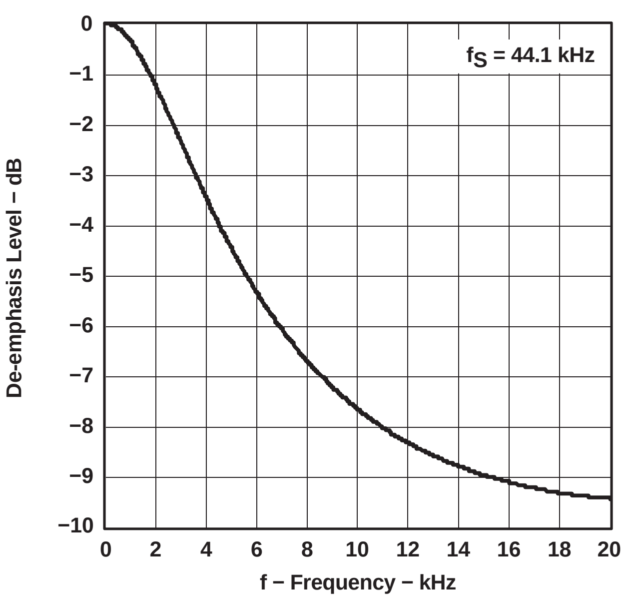


Figure 7

DE-EMPHASIS ERROR vs FREQUENCY

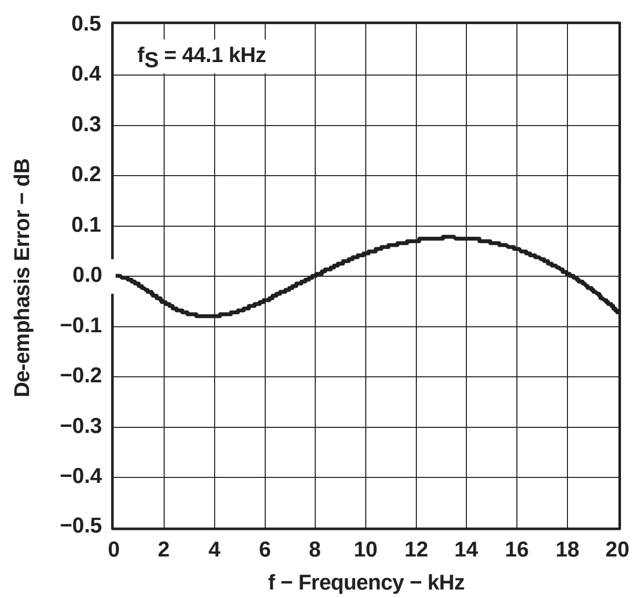


Figure 8

(1) All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit data, unless otherwise noted

DE-EMPHASIS CURVES (CONTINUED)

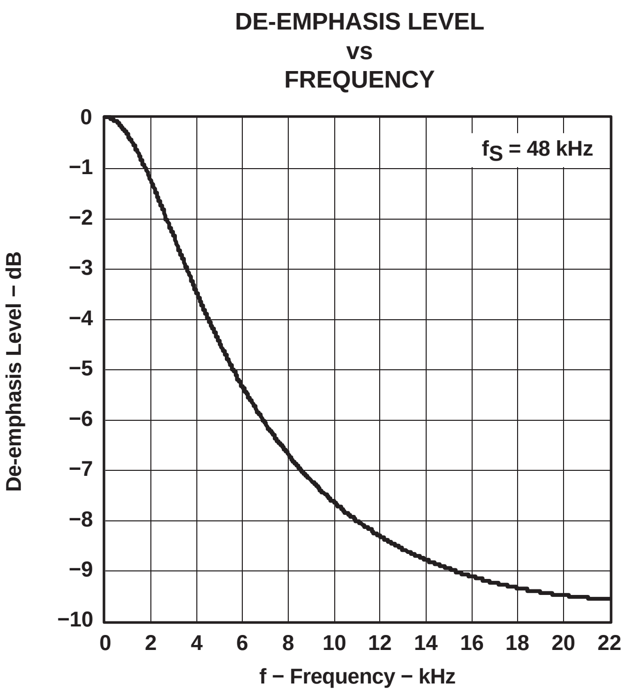


Figure 9

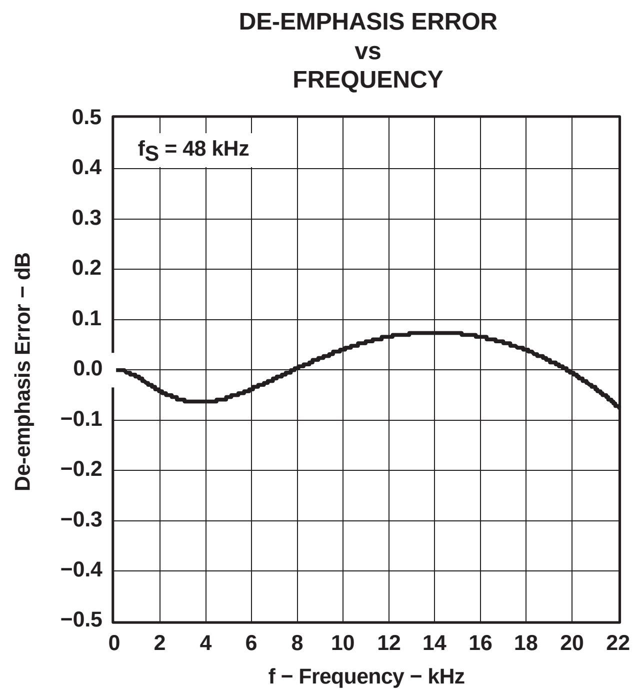


Figure 10

(1) All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit data, unless otherwise noted

ANALOG DYNAMIC PERFORMANCE (SUPPLY VOLTAGE CHARACTERISTICS)

**TOTAL HARMONIC DISTORTION + NOISE
vs
SUPPLY VOLTAGE**

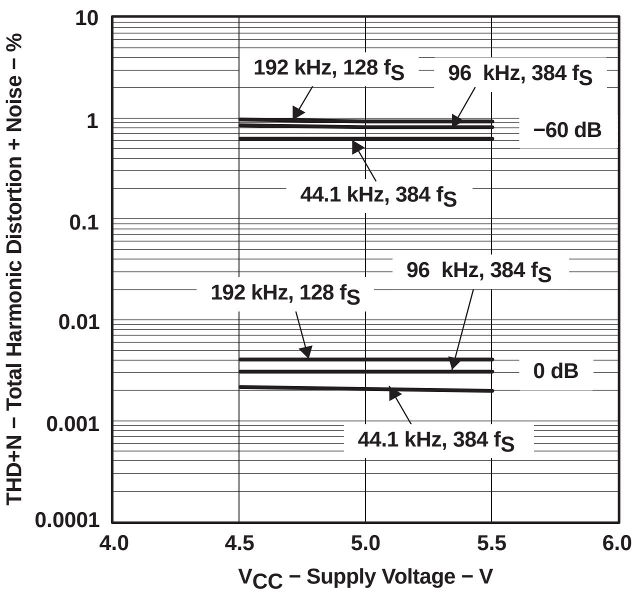


Figure 11

**DYNAMIC RANGE
vs
SUPPLY VOLTAGE**

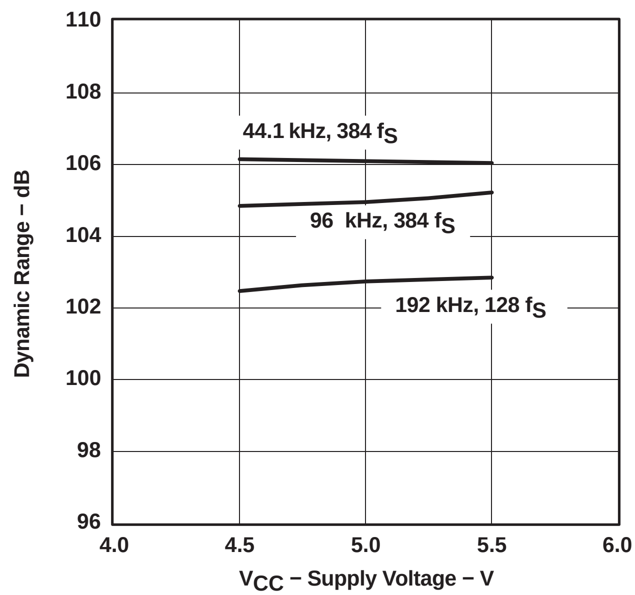


Figure 12

**SIGNAL-to-NOISE RATIO
vs
SUPPLY VOLTAGE**

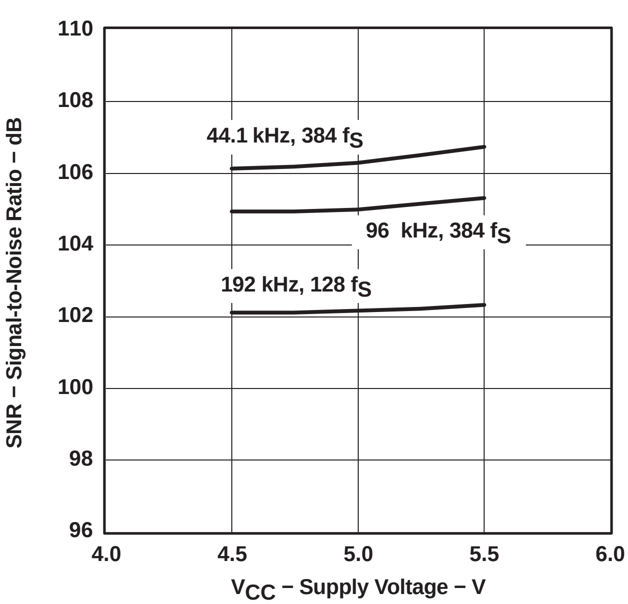


Figure 13

**CHANNEL SEPARATION
vs
SUPPLY VOLTAGE**

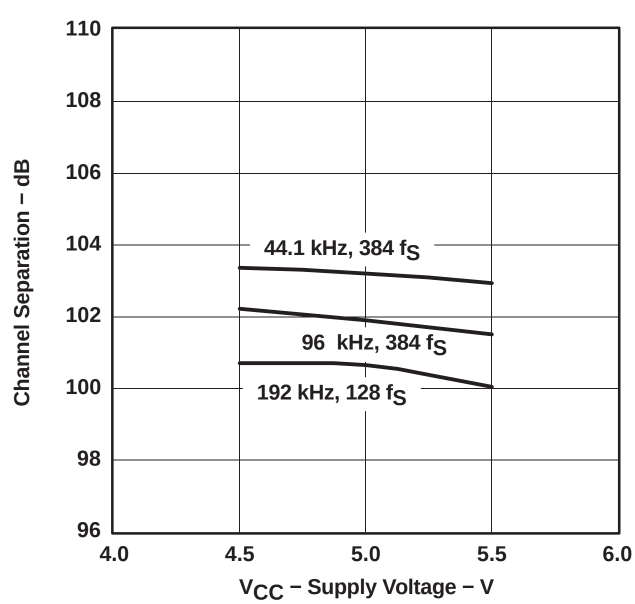


Figure 14

(1) All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit data, unless otherwise noted

ANALOG DYNAMIC PERFORMANCE (TEMPERATURE CHARACTERISTICS)

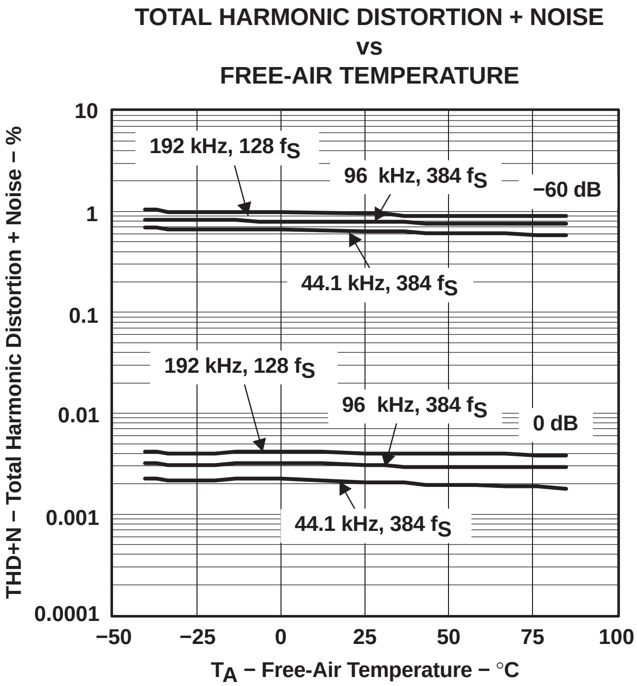


Figure 15

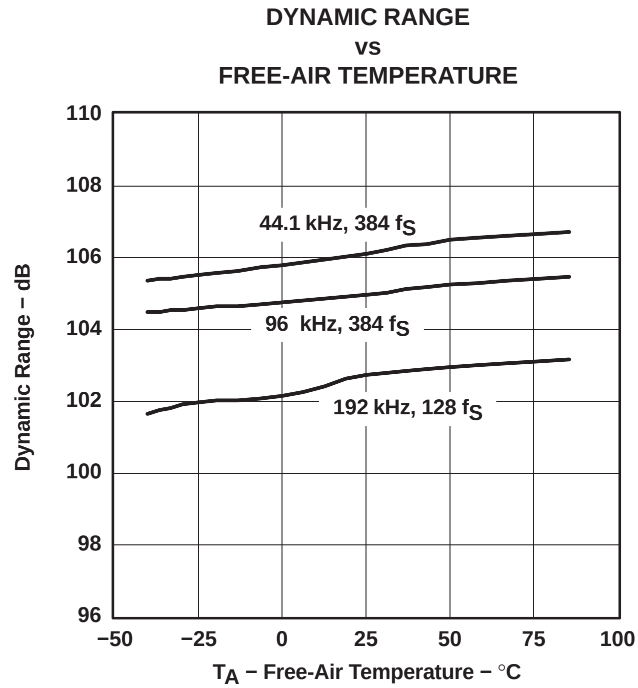


Figure 16

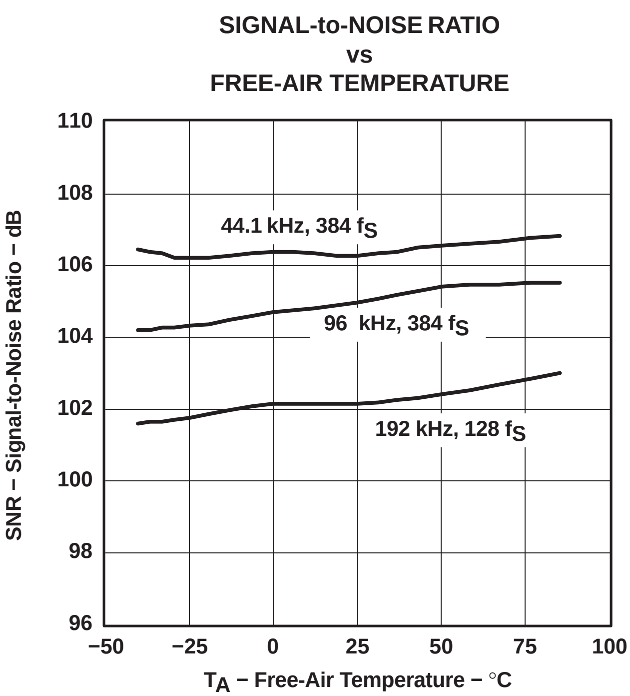


Figure 17

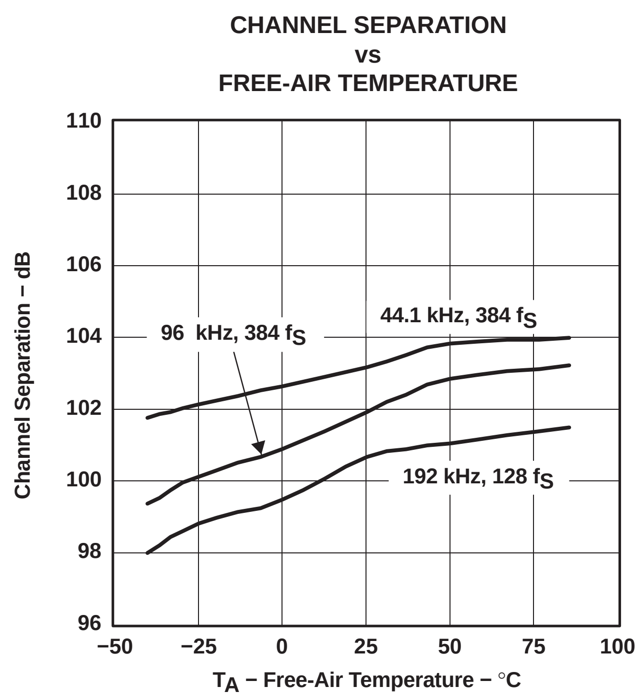


Figure 18

(1) All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit data, unless otherwise noted
(2) −25°C to 85°C for the PCM1753/55, −40°C to 85°C for the PCM1754

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SYSTEM CLOCK AND RESET FUNCATIONS

System Clock Input

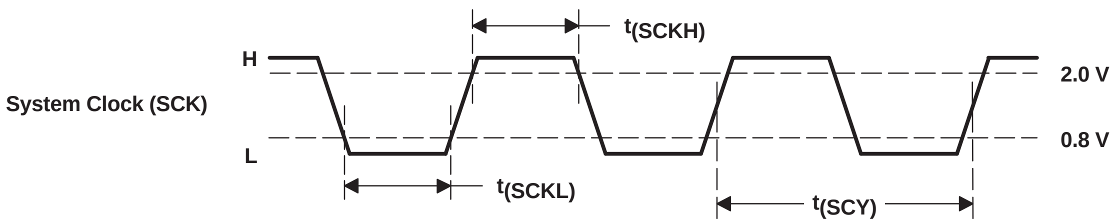
The PCM1753/54/55 requires a system clock for operating the digital interpolation filters and multilevel delta-sigma modulators. The system clock is applied at the SCK input (pin 16). Table 1 shows examples of system clock frequencies for common audio sampling rates.

Figure 19 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase-jitter and noise. TI's PLL170x family of multiclock generators is an excellent choice for providing the PCM1753/54/55 system clock.

Table 1. System Clock Rates for Common Audio Sampling Frequencies

SAMPLING FREQUENCY	SYSTEM CLOCK FREQUENCY (f_{SCLK}) (MHz)						
	128 f_S	192 f_S	256 f_S	384 f_S	512 f_S	768 f_S	1152 f_S
8 kHz	1.0240	1.5360	2.0480	3.0720	4.0960	6.1440	9.2160
16 kHz	2.0480	3.0720	4.0960	6.1440	8.1920	12.2880	18.4320
32 kHz	4.0960	6.1440	8.1920	12.2880	16.3840	24.5760	36.8640
44.1 kHz	5.6448	8.4672	11.2896	16.9344	22.5792	33.8688	(1)
48 kHz	6.1440	9.2160	12.2880	18.4320	24.5760	36.8640	(1)
88.2 kHz	11.2896	16.9344	22.5792	33.8688	45.1584	(1)	(1)
96 kHz	12.2880	18.4320	24.5760	36.8640	49.1520	(1)	(1)
192 kHz	24.5760	36.8640	49.1520	(1)	(1)	(1)	(1)

(1) This system clock rate is not supported for the given sampling frequency.



PARAMETERS	SYMBOL	MIN	TYP	MAX	UNITS
System clock pulse duration, high	t_{SCKH}	7			ns
System clock pulse duration, low	t_{SCKL}	7			ns

(1) 1/128 f_S, 1/256 f_S, 1/384 f_S, 1/512 f_S, 1/768 f_S, or 1/1152 f_S

Figure 19. System Clock Input Timing

Power-On Reset Functions

The PCM1753/54/55 includes a power-on reset function. Figure 20 shows the operation of this function. With the system clock active and V_{CC} > 3 V (typical, 2.2 V to 3.7 V), the power-on reset function is enabled. The initialization sequence requires 1024 system clocks from the time V_{CC} > 3 V (typical, 2.2 V to 3.7 V). After the initialization period, the PCM1753/55 is set to its reset default state, as described in the *Mode Control Registers* section of this data sheet.

During the reset period (1024 system clocks), the analog output is forced to the bipolar zero level, or $V_{CC}/2$. After the reset period, an internal register is initialized in the next $1/f_S$ period and if SCK, BCK and LRCK are provided continuously, the PCM1753/54/55 provides proper analog output with unit group delay against the input data.

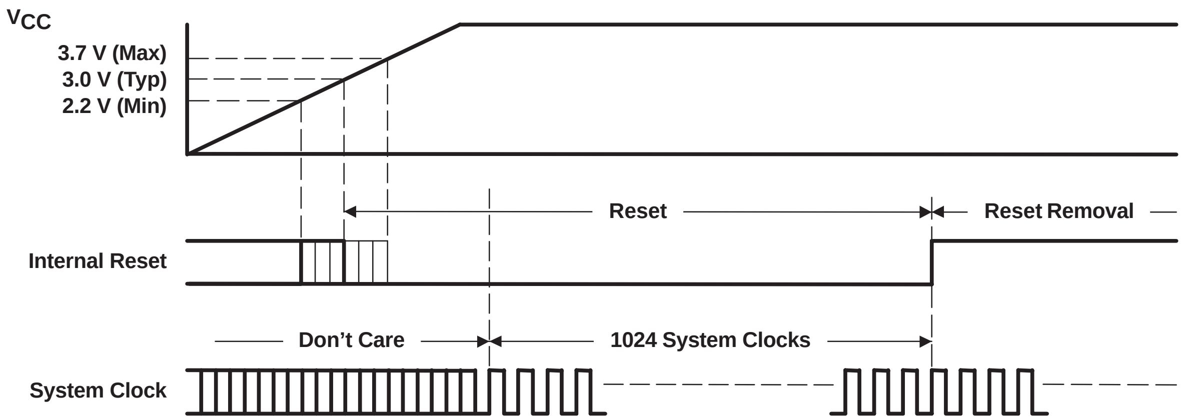


Figure 20. Power-On Reset Timing

AUDIO SERIAL INTERFACE

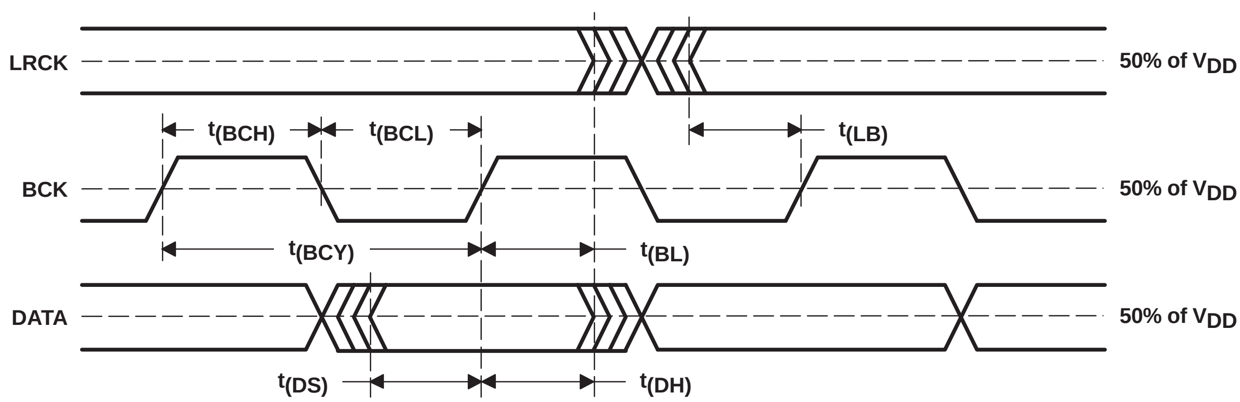
The audio serial interface for the PCM1753/54/55 consists of a 3-wire synchronous serial port. It includes LRCK (pin 3), BCK (pin 1), and DATA (pin 2). BCK is the serial audio bit clock, and it is used to clock the serial data present on DATA into the serial shift register of the audio interface. Serial data is clocked into the PCM1753/54/55 on the rising edge of BCK. LRCK is the serial audio left/right word clock. It is used to latch serial data into the internal registers of the serial audio interface.

Both LRCK and BCK should be synchronous to the system clock. Ideally, it is recommended that LRCK and BCK be derived from the system clock input, SCK. LRCK is operated at the sampling frequency, f_S. BCK can be operated at 32, 48, or 64 times the sampling frequency for standard and left-justified formats. BCK can be operated at 48 or 64 times the sampling frequency for the I^2S format.

Internal operation of the PCM1753/54/55 is synchronized with LRCK. Accordingly, internal operation is held when the sampling rate clock of LRCK is changed or when SCK and/or BCK is interrupted for a 3-bit clock cycle or longer. If SCK, BCK, and LRCK are provided continuously after this held condition, the internal operation is re-synchronized automatically in a period of less than $3/f_S$. External resetting is not required.

Audio Data Formats and Timing

The PCM1753/55 supports industry-standard audio data formats, including standard, I^2S, and left-justified. The PCM1754 supports I^2S and 16-bit-word right-justified. The data formats are shown in Figure 22. Data formats are selected using the format bits, FMT[2:0], located in control register 20 of the PCM1753/55, and are selected using the FMT pin on the PCM1754. The default data format is 24-bit left-justified. All formats require binary 2s-complement, MSB-first audio data. Figure 21 shows a detailed timing diagram for the serial audio interface.

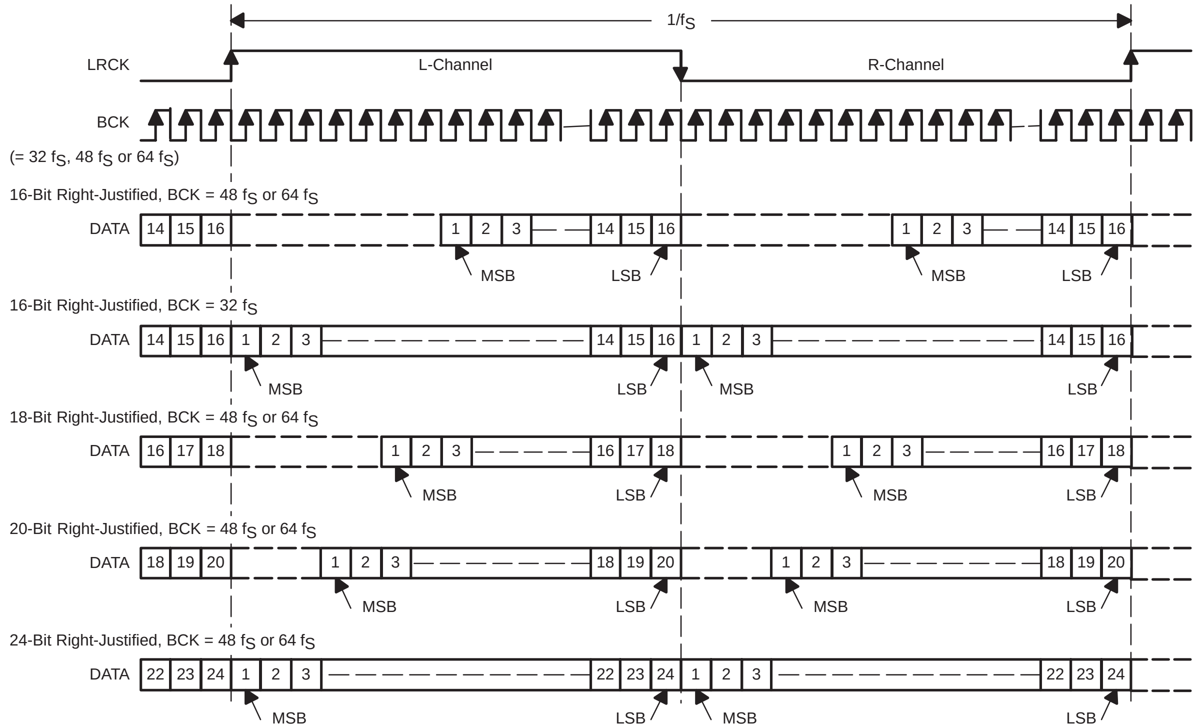


PARAMETERS	SYMBOL	MIN	MAX	UNITS
BCK pulse cycle time	t_{BCY}		$1/(32\ f_S)$, $1/(48\ f_S)$, $1/(64\ f_S)$ (1)	
BCK high-level time	t_{BCH}	35		ns
BCK low-level time	t_{BCL}	35		ns
BCK rising edge to LRCK edge	t_{BL}	10		ns
LRCK falling edge to BCK rising edge	t_{LB}	10		ns
DATA setup time	t_{DS}	10		ns
DATA hold time	t_{DH}	10		ns

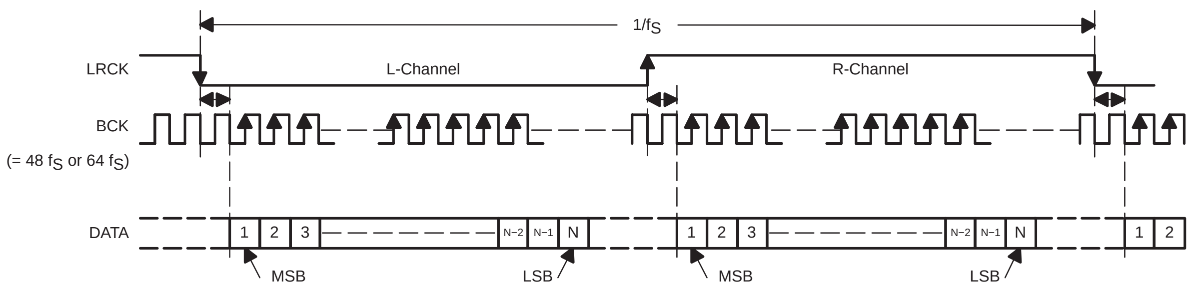
(1) f_S is the sampling frequency (e.g., 44.1 kHZ, 48 kHz, 96 kHz, etc.).

Figure 21. Audio Interface Timing

(1) Standard Data Format; L-Channel = HIGH, R-Channel = LOW



(2) I²S Data Format; L-Channel = LOW, R-Channel = HIGH



(3) Left-Justified Data Format; L-Channel = HIGH, R-Channel = LOW

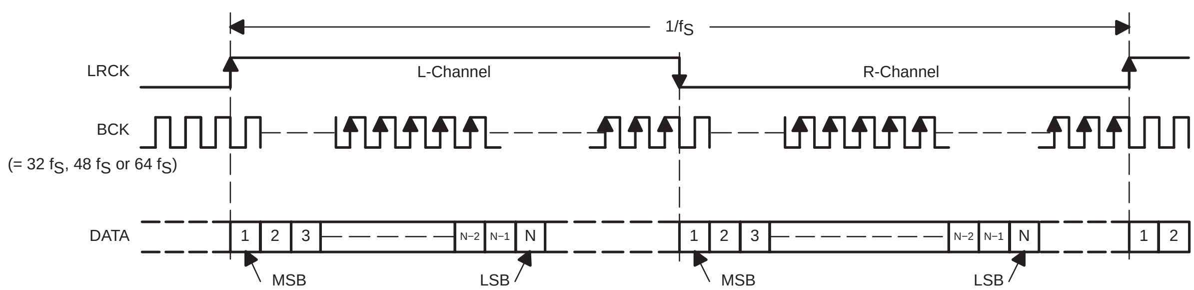


Figure 22. Audio Data Input Formats

ZERO FLAGS (PCM1753/55)

Zero-Detect Condition

Zero detection for either output channel is independent from the other channel. If the data for a given channel remains at a 0 level for 1024 sample periods (or LRCK clock periods), a zero-detect condition exists for that channel.

Zero Flag Outputs

If a zero-detect condition exists for one or more channels, the zero flag pins for those channels are set to a logic 1 state. There are zero flag pins for each channel, ZEROL (pin 12) and ZEROR (pin 11). These pins can be used to operate external mute circuits, or used as status indicators for a microcontroller, audio signal processor, or other digitally controlled function.

The active polarity of zero flag outputs can be inverted by setting the ZREV bit of control register 22 to 1. The reset default is active-high output, or ZREV = 0.

The L-channel and R-channel common zero flag can be selected by setting the AZRO bit of control register 22 to 1. The reset default is independent zero flags for L-channel and R-channel, or AZRO = 0.

In the case of the PCM1755, ZEROL and ZEROR are open-drain outputs.

ZERO FLAG (PCM1754)

The PCM1754 has a ZERO flag pin, ZEROA (pin 11). ZEROA is the L-channel and R-channel common zero flag pin. If the data for L-channel and R-channel remains at a 0 level for 1024 sampling periods (or LRCK clock periods), ZEROA is set to a logic 1 state.

HARDWARE CONTROL (PCM1754)

The digital functions of the PCM1754 are capable of hardware control. Table 2 shows selectable formats, Table 3 shows de-emphasis control, and Table 4 shows mute control.

Table 2. Data Format Select

FMT (PIN 15)	DATA FORMAT
LOW	16- to 24-bit, I^2S format
HIGH	16-bit right justified

Table 3. De-Emphasis Control

DEMP (PIN 13)	DE-EMPHASIS FUNCTION
LOW	44.1 kHz de-emphasis OFF
HIGH	44.1 kHz de-emphasis ON

Table 4. Mute Control

MUTE (PIN 14)	MUTE
LOW	Mute OFF
HIGH	Mute ON

OVERSAMPLING RATE CONTROL (PCM1754)

The PCM1754 automatically controls the oversampling rate of the delta-sigma D/A converters with the system clock rate. The oversampling rate is set to 64× oversampling with every system clock and sampling frequency.

SOFTWARE CONTROL (PCM1753/55)

The PCM1753/55 has many programmable functions which can be controlled in the software control mode. The functions are controlled by programming the internal registers using ML, MC, and MD.

The serial control interface is a 3-wire serial port, which operates asynchronously to the audio serial interface. The serial control interface is used to program the on-chip mode registers. The control interface includes MD (pin 13), MC (pin 14), and ML (pin 15). MD is the serial data input, used to program the mode registers. MC is the serial bit clock, used to shift data into the control port. ML is the control port latch clock.

Register Write Operation

All write operations for the serial control port use 16-bit data words. Figure 23 shows the control data word format. The most significant bit must be a 0. There are seven bits, labeled IDX[6:0], that set the register index (or address) for the write operation. The least significant eight bits, D[7:0], contain the data to be written to the register specified by IDX[6:0].

Figure 24 shows the functional timing diagram for writing to the serial control port. ML is held at a logic 1 state until a register needs to be written. To start the register write cycle, ML is set to logic 0. Sixteen clocks are then provided on MC, corresponding to the 16 bits of the control data word on MD. After the sixteenth clock cycle has completed, ML is set to logic 1 to latch the data into the indexed mode control register.

MSB															LSB
0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	D7	D6	D5	D4	D3	D2	D1	D0
Register Index (or Address)								Register Data							

Figure 23. Control Data Word Format for MD

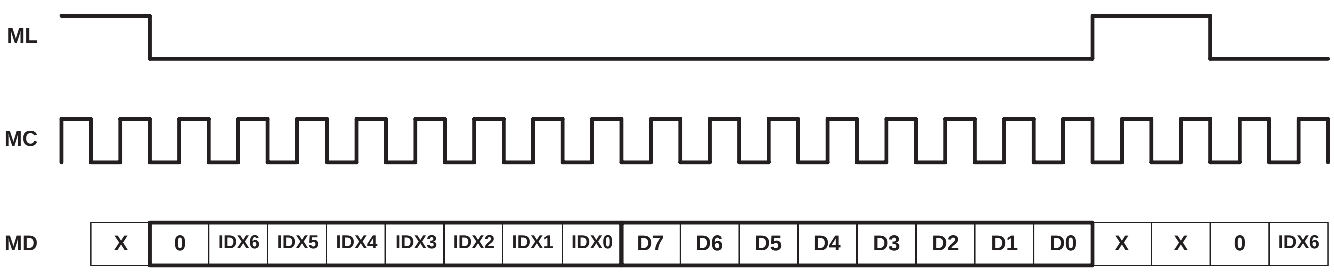
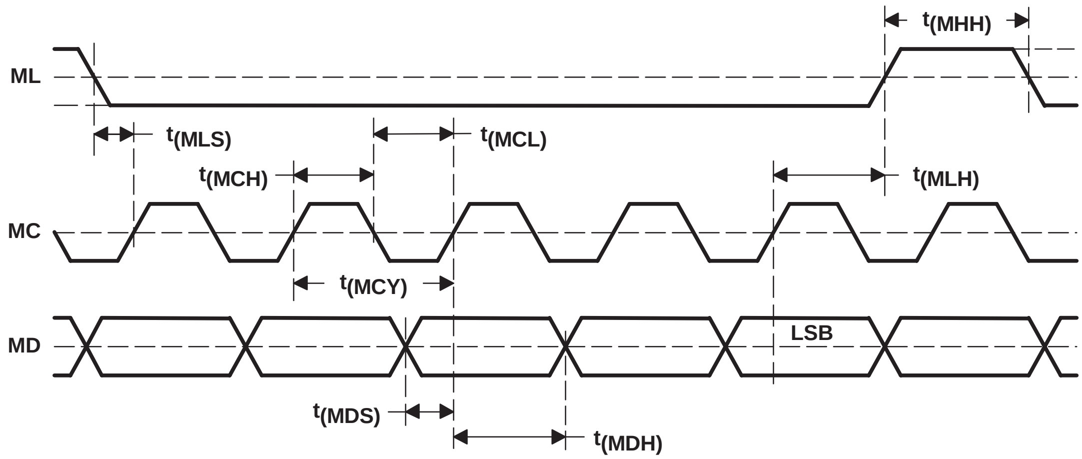


Figure 24. Register Write Operation

Control Interface Timing Requirements

Figure 25 shows a detailed timing diagram for the serial control interface. These timing parameters are critical for proper control port operation.



PARAMETERS	SYMBOL	MIN	TYP	MAX	UNITS
MC pulse cycle time	t_{MCY}	100			ns
MC low-level time	t_{MCL}	50			ns
MC high-level time	t_{MCH}	50			ns
ML high-level time	t_{MHH}	(2)			ns
ML falling edge to MC rising edge	t_{MLS}	20			ns
ML hold time (1)	t_{MLH}	20			ns
MD hold time	t_{MDH}	15			ns
MD setup time	t_{MDS}	20			ns

(1) MC rising edge for LSB to ML rising edge.

(2) $\frac{3}{256 \times f_S}$ sec (min); f_S: sampling rate

Figure 25. Control Interface Timing

MODE CONTROL REGISTERS (PCM1753/55)

User-Programmable Mode Controls

The PCM1753/55 includes a number of user programmable functions, which are accessed via control registers. The registers are programmed using the serial control interface, which was previously discussed in this data sheet. Table 5 lists the available mode control functions, along with their reset default conditions and associated register index.

Register Map

The mode control register map is shown in Table 6. Each register includes an index (or address) indicated by the IDX[6:0] bits.

Table 5. User-Programmable Mode Controls

FUNCTION	RESET DEFAULT	REGISTER	BIT(s)
Digital attenuation control, 0 dB to −63 dB in 0.5-dB steps	0 dB, no attenuation	16 and 17	AT1[7:0], AT2[7:0]
Soft mute control	Mute disabled	18	MUT[2:0]
Oversampling rate control (64 f_S or 128 f_S)	64 f_S oversampling	18	OVER
Soft reset control	Reset disabled	18	SRST
DAC operation control	DAC1 and DAC2 enabled	19	DAC[2:1]
De-emphasis function control	De-emphasis disabled	19	DM12
De-emphasis sample rate selection	44.1 kHz	19	DMF[1:0]
Audio data format control	24-bit left-justified	20	FMT[2:0]
Digital filter rolloff control	Sharp rolloff	20	FLT
Zero flag function select	L-, R-channel independent	22	AZRO
Output phase select	Normal phase	22	DREV
Zero flag polarity select	High	22	ZREV

Table 6. Mode Control Register Map

IDX (B8−B14)	REGISTER	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
10h	Register 16	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT17	AT16	AT15	AT14	AT13	AT12	AT11	AT10
11h	Register 17	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT27	AT26	AT25	AT24	AT23	AT22	AT21	AT20
12h	Register 18	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	SRST	OVER	RSV	RSV	RSV	RSV	MUT2	MUT1
13h	Register 19	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	DMF1	DMF0	DM12	RSV	RSV	DAC2	DAC1
14h	Register 20	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	FLT	RSV	RSV	FMT2	FMT1	FMT0
16h	Register 22	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	AZRO	ZREV	DREV

NOTE: RSV: Reserved for test operation. It should be set to 0 for regular operation.

Register Definitions

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 16	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT17	AT16	AT15	AT14	AT13	AT12	AT11	AT10

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 17	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT27	AT26	AT25	AT24	AT23	AT22	AT21	AT20

ATx[7:0]: Digital Attenuation Level Setting

Where x = 1 or 2, corresponding to the DAC output $V_{OUT}L$ (x = 1) and $V_{OUT}R$ (x = 2).

Default value: 1111 1111b

Each DAC channel ($V_{OUT}L$ and $V_{OUT}R$) includes a digital attenuation function. The attenuation level can be set from 0 dB to −63 dB in 0.5 dB steps. Changes in attenuator levels are made by incrementing or decrementing one step (0.5 dB) for every $8/f_S$ time internal until the programmed attenuator setting is reached. Alternatively, the attenuation level can be set to infinite attenuation (or mute).

The attenuation data for each channel can be set individually. The attenuation level is set using the following formula:

Attenuation level (dB) = $0.5 \bullet (ATx[7:0]_{DEC} - 255)$

where $ATx[7:0]_{DEC}$ = 0 through 255.

For $ATx[7:0]_{DEC}$ = 0 through 128, attenuation is set to infinite attenuation.

The following table shows the attenuation levels for various settings:

ATx[7:0]	DECIMAL VALUE	ATTENUATION LEVEL SETTING
1111 1111b	255	0 dB, No Attenuation. (default)
1111 1110b	254	−0.5 dB
1111 1101b	253	−1.0 dB
⋮	⋮	⋮
1000 0011b	131	−62.0 dB
1000 0010b	130	−62.5 dB
1000 0001b	129	−63.0 dB
1000 0000b	128	Mute
⋮	⋮	⋮
$0000\ 0000_B$	0	Mute

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 18	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	SRST	OVER	RSV	RSV	RSV	RSV	MUT2	MUT1

MUTx: Soft Mute Control

where x = 1 or 2, corresponding to the DAC outputs V_{OUT} L (x = 1) and $V_{OUT}R$ (x = 2).

Default value: 0

MUTx = 0	Mute disabled (default)
MUTx = 1	Mute enabled

The mute bits, MUT1 and MUT2, are used to enable or disable the soft mute function for the corresponding DAC outputs, $V_{OUT}L$ and $V_{OUT}R$. The soft mute function is incorporated into the digital attenuators. When mute is disabled (MUTx = 0), the attenuator and DAC operate normally. When mute is enabled by setting MUTx = 1, the digital attenuator for the corresponding output is decreased from the current setting to infinite attenuation, one attenuator step (0.5 dB) for every $8/f_S$ seconds. This provides pop-free muting of the DAC output.

By setting MUTx = 0, the attenuator is increased one step for every $8/f_S$ seconds to the previously programmed attenuation level.

OVER: Oversampling Rate Control

Default value: 0

System clock rate = 256 f_S, 384 f_S, 512 f_S, 768 f_S or 1152 f_S:

OVER = 0	64× oversampling (default)
OVER = 1	128× oversampling

System clock rate = 128 f_S or 192 f_S:

OVER = 0	32× oversampling (default)
OVER = 1	64× oversampling

The OVER bit is used to control the oversampling rate of the delta-sigma D/A converters. The OVER = 1 setting is recommended when sampling rate is 192 kHz (system clock rate is 128 f_S or 192 f_S).

SRST: Reset

Default value: 0

SRST = 0	Reset disabled (default)
SRST = 1	Reset enabled

The SRST bit is used to enable or disable the soft reset function. The operation is the same as power-on reset. All registers are initialized.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 19	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	DMF1	DMF0	DM12	RSV	RSV	DAC2	DAC1

DACx: DAC Operation Control

Where x = 1 or 2, corresponding to the DAC output $V_{OUT}L$ (x = 1) or $V_{OUT}R$ (x = 2).

Default value: 0

DACx = 0	DAC operation enabled (default)
DACx = 1	DAC operation disabled

The DAC operation controls are used to enable and disable the DAC outputs, $V_{OUT}L$ and $V_{OUT}R$. When DACx = 0, the corresponding output generates the audio waveform dictated by the data present on the DATA pin. When DACx = 1, the corresponding output is set to the bipolar zero level, or 0.5 V_{CC}.

DM12: Digital De-Emphasis Function Control

Default value: 0

DM12 = 0	De-emphasis disabled (default)
DM12 = 1	De-emphasis enabled

The DM12 bit is used to enable or disable the digital de-emphasis function. See the plots shown in the *Typical Performance Curves* section of this data sheet.

DMF[1:0]: Sampling Frequency Selection for the De-Emphasis Function

Default value: 00

The DMF[1:0] bits are used to select the sampling frequency used for the digital de-emphasis function when it is enabled.

DMF[1:0]	De-Emphasis Sample Rate Selection
00	44.1 kHz (default)
01	48 kHz
10	32 kHz
11	Reserved

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 20	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	FLT	RSV	RSV	FMT2	FMT1	FMT0

FMT[2:0]: Audio Interface Data Format

Default value: 101

The FMT[2:0] bits are used to select the data format for the serial audio interface. The following table shows the available format options.

FMT[2:0]	Audio Data Format Selection
000	24-bit standard format, right-justified data
001	20-bit standard format, right-justified data
010	18-bit standard format, right-justified data
011	16-bit standard format, right-justified data
100	16- to 24-bit I^2S format
101	16- to 24-bit left-justified format (default)
110	Reserved
111	Reserved

FLT: Digital Filter Rolloff Control

Default value: 0

FLT = 0	Sharp rolloff (default)
FLT = 1	Slow rolloff

The FLT bit allows the user to select the digital filter rolloff that is best suited to the application. Two filter rolloff selections are available, sharp and slow. The filter responses for these selections are shown in the *Typical Performance Curves* section of this data sheet.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 22	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	AZRO	ZREV	DREV

DREV: Output Phase Select

Default value: 0

DREV = 0	Normal output (default)
DREV = 1	Inverted output

The DREV bit is the output analog signal phase control.

ZREV: Zero Flag Polarity Select

Default value: 01h

ZREV = 0	High on zero flag pins indicates a zero detect (default)
ZREV = 1	Low on zero flag pins indicates a zero detect

The ZREV bit allows the user to select the polarity of zero flag pins.

AZRO: Zero Flag Function Select

Default value: 0

AZRO = 0	L-/R-channel independent zero flags (default)
AZRO = 1	L-/R-channel common zero flag

The AZRO bit allows the user to select the function of zero flag pins.

AZRO = 0:	Pin 11: ZEROR, zero flag output for R-channel
	Pin 12: ZEROL, zero flag output for L-channel
AZRO = 1:	Pin 11: ZEROA, zero flag output for L-/R-channels
	Pin 12: NA, not assigned

ANALOG OUTPUTS

The PCM1753/54/55 includes two independent output channels, $V_{OUT}L$ and $V_{OUT}R$. These are unbalanced outputs, each capable of driving 4 V p-p typical into a 5-kΩ ac-coupled load. The internal output amplifiers for $V_{OUT}L$ and $V_{OUT}R$ are biased to the dc common-mode (or bipolar zero) voltage, equal to 0.5 V_{CC}.

The output amplifiers include an RC continuous-time filter, which helps to reduce the out-of-band noise energy present at the DAC outputs due to the noise shaping characteristics of the PCM1753/54/55 delta-sigma D/A converters. The frequency response of this filter is shown in Figure 26. By itself, this filter is not enough to attenuate the out-of-band noise to an acceptable level for many applications. An external low-pass filter is required to provide sufficient out-of-band noise rejection. Further discussion of DAC post-filter circuits is provided in the *Applications Information* section of this data sheet.

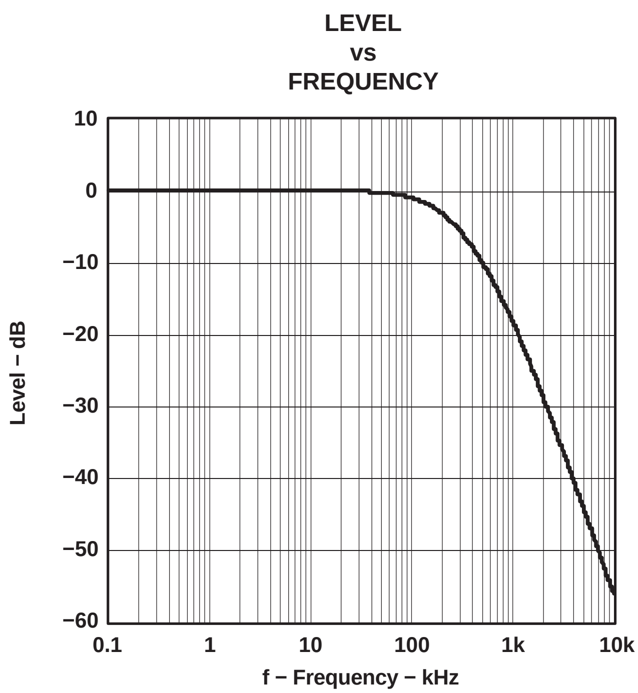
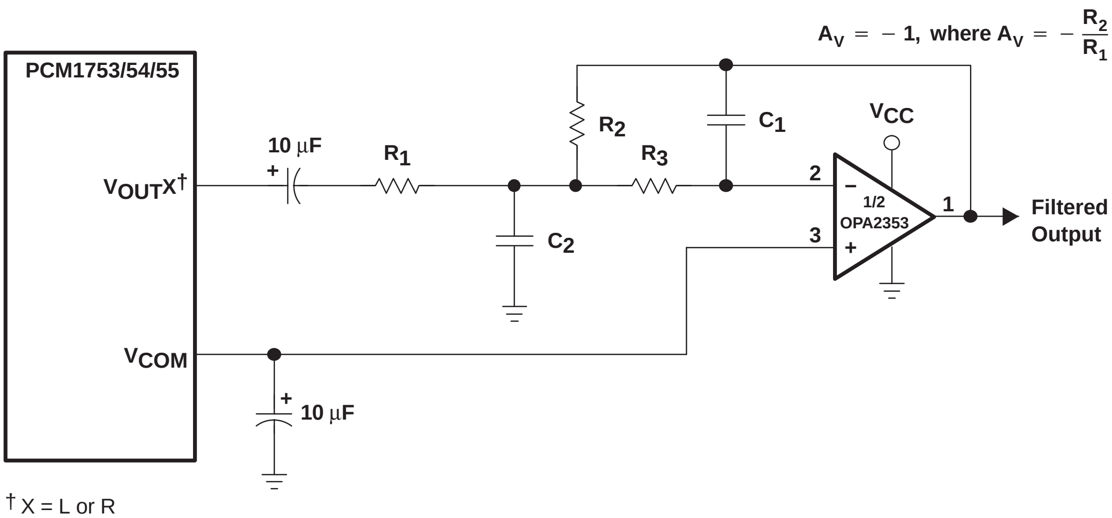


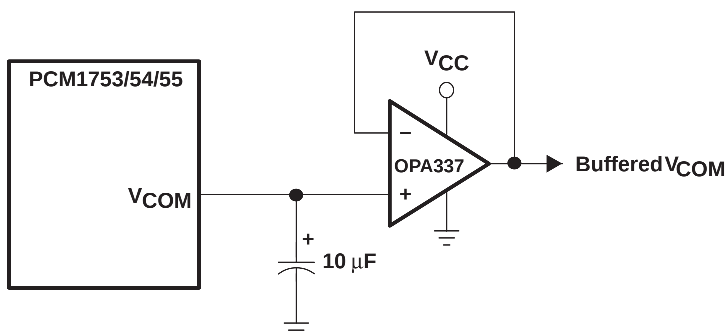
Figure 26. Output Filter Frequency Response

V_{COM} Output

One unbuffered common-mode voltage output pin, V_{COM} (pin 10) is brought out for decoupling purposes. This pin is nominally biased to a dc voltage level equal to 0.5 V_{CC}. This pin can be used to bias external circuits. Figure 27 shows an example of using the V_{COM} pin for external biasing applications.



(a) Using V_{COM} to Bias a Single-Supply Filter Stage



(b) Using a Voltage Follower to Buffer V_{COM} when Biasing Multiple Nodes

Figure 27. Biasing External Circuits Using the V_{COM} Pin

APPLICATION INFORMATION

CONNECTION DIAGRAMS

A basic connection diagram is shown in Figure 28, with the necessary power supply bypassing and decoupling components. TI recommends using the component values shown in Figure 28 for all designs.

The use of series resistors (22 Ω to 100 Ω) is recommended for the SCK, LRCK, BCK, and DATA inputs. The series resistor combines with the stray PCB and device input capacitance to form a low-pass filter, which reduces high-frequency noise emissions and helps to dampen glitches and ringing present on clock and data lines.

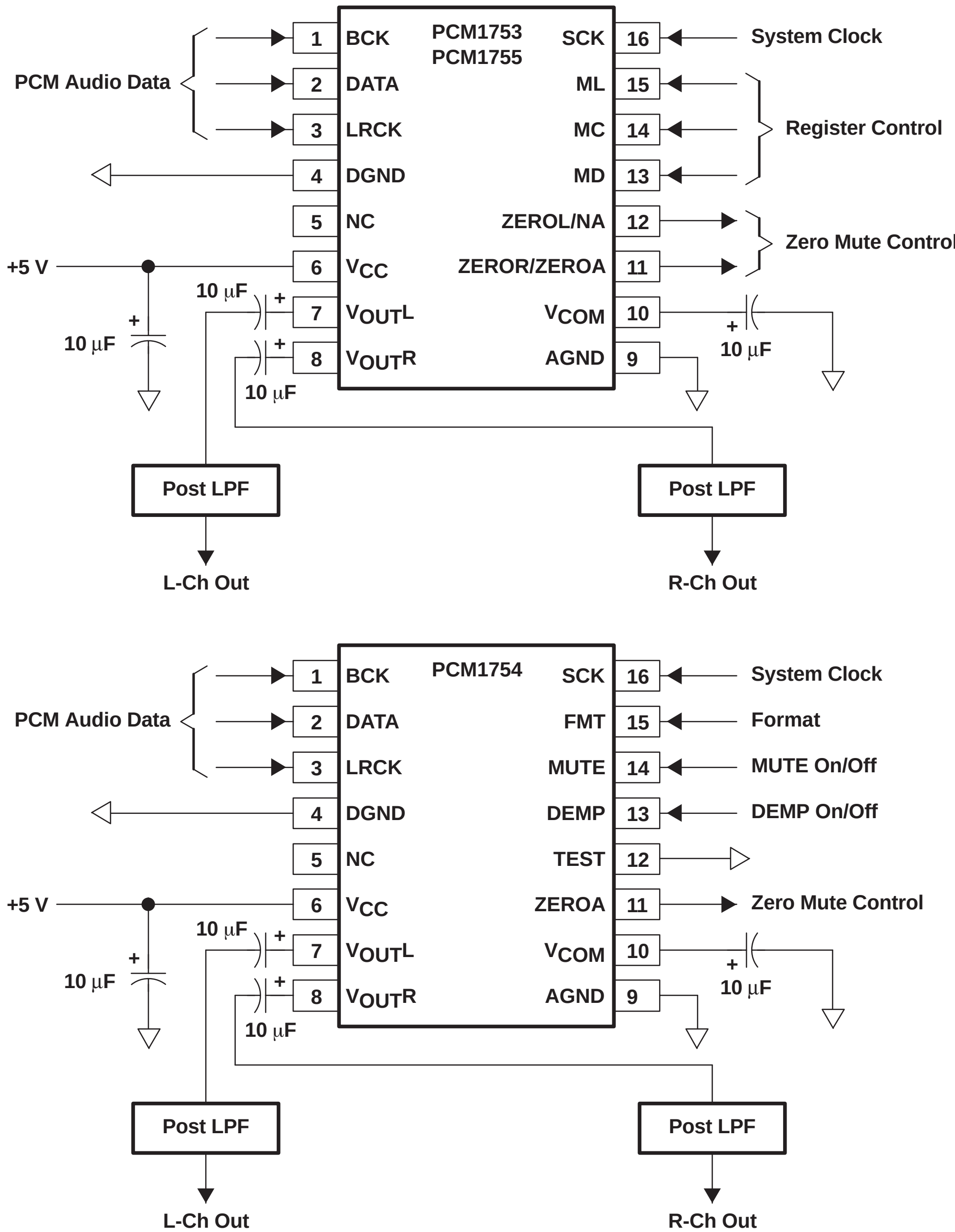


Figure 28. Basic Connection Diagram

POWER SUPPLIES AND GROUNDING

The PCM1753/54/55 requires 5 V for V_{CC}.

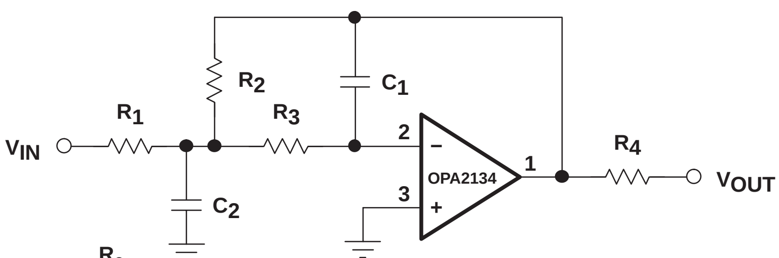
Proper power supply bypassing is shown in Figure 28. The 10-µF capacitors should be tantalum or aluminum electrolytic.

D/A OUTPUT FILTER CIRCUITS

Delta-sigma D/A converters use noise-shaping techniques to improve in-band signal-to-noise ratio (SNR) performance at the expense of generating increased out-of-band noise above the Nyquist frequency, or $f_S/2$. The out-of-band noise must be low-pass filtered in order to provide the optimal converter performance. This is accomplished by a combination of on-chip and external low-pass filtering.

Figure 27(a) and Figure 29 show the recommended external low-pass active filter circuits for single- and dual-supply applications. These circuits are 2nd-order Butterworth filters using the multiple feedback (MFB) circuit arrangement, which reduces sensitivity to passive component variations over frequency and temperature. For more information regarding MFB active filter design, please see Burr-Brown applications bulletin (SBAA055), available from our web site at http://www.ti.com.

Since the overall system performance is defined by the quality of the D/A converters and their associated analog output circuitry, high-quality audio op amps are recommended for the active filters. TI's OPA2353 and OPA2134 dual op amps are shown in Figure 27(a) and Figure 29, and are recommended for use with the PCM1753/54/55.



$$A_V \approx -\frac{R_2}{R_1}$$

Figure 29. Dual-Supply Filter Circuit

PCB LAYOUT GUIDELINES

A typical PCB floor plan for the PCM1753/54/55 is shown in Figure 30. A ground plane is recommended, with the analog and digital sections being isolated from one another using a split or cut in the circuit board. The PCM1753/54/55 should be oriented with the digital I/O pins facing the ground plane split/cut to allow for short, direct connections to the digital audio interface and control signals originating from the digital section of the board.

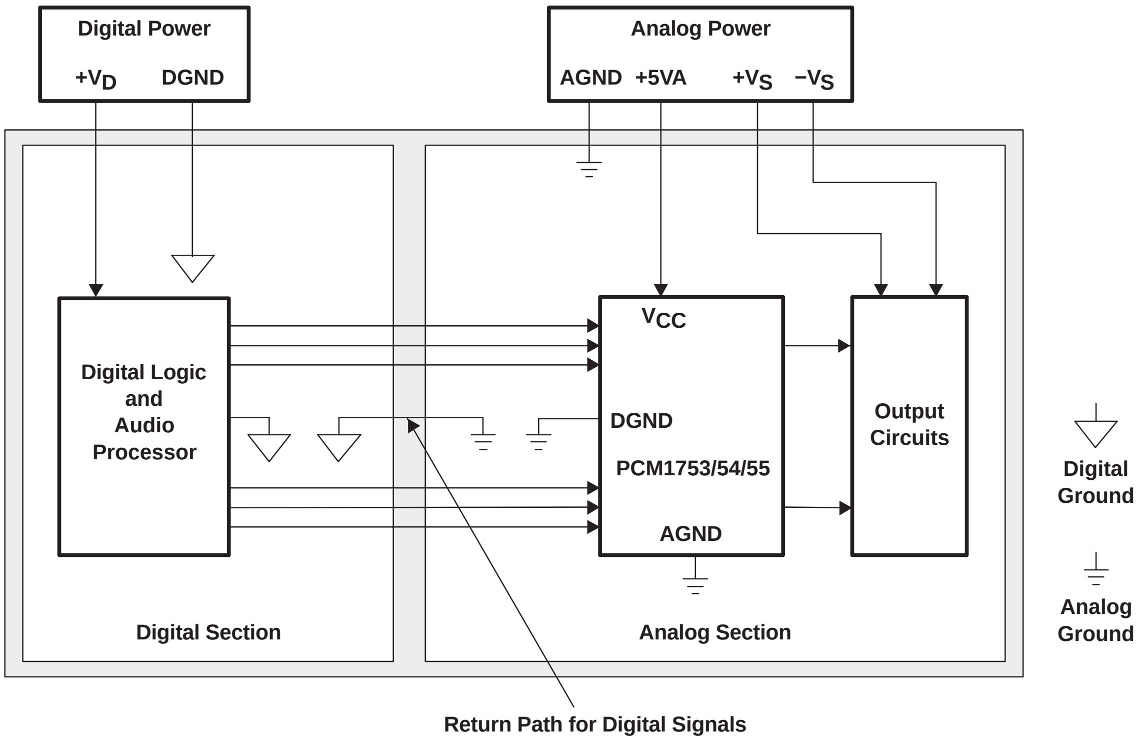


Figure 30. Recommended PCB Layout

Separate power supplies are recommended for the digital and analog sections of the board. This prevents the switching noise present on the digital supply from contaminating the analog power supply and degrading the dynamic performance of the PCM1753/54/55. In cases where a common 5-V supply must be used for the analog and digital sections, an inductance (RF choke, ferrite bead) should be placed between the analog and digital 5-V supply connections to avoid coupling of the digital switching noise into the analog circuitry. Figure 31 shows the recommended approach for single-supply applications.

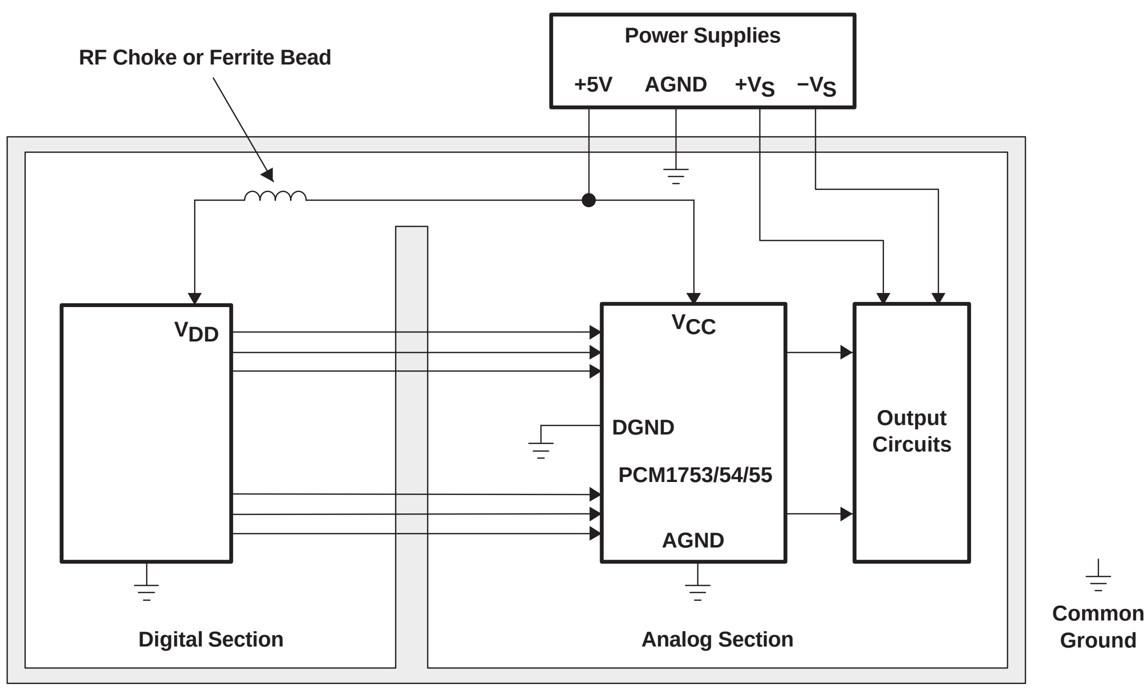


Figure 31. Single-Supply PCB Layout

THEORY OF OPERATION

The delta-sigma section of the PCM1753/54/55 is based on an 8-level amplitude quantizer and a 4th-order noise shaper. This section converts the oversampled input data to 8-level delta-sigma format. A block diagram of the 8-level delta-sigma modulator is shown in Figure 32. This 8-level delta-sigma modulator has the advantage of stability and clock jitter sensitivity over the typical one-bit (2-level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the interpolation filter is 64 f_S.

The theoretical quantization noise performance of the 8-level delta-sigma modulator is shown in Figure 33 and Figure 34. The enhanced multi-level delta-sigma architecture also has advantages for input clock jitter sensitivity due to the multilevel quantizer, with the simulated jitter sensitivity shown in Figure 35.

KEY PERFORMANCE PARAMETERS AND MEASUREMENT

This section provides information on how to measure key dynamic performance parameters for the PCM1753/54/55. In all cases, an Audio Precision System Two Cascade audio measurement system or equivalent is used to perform the testing.

Total Harmonic Distortion + Noise

Total harmonic distortion + noise (THD+N) is a significant figure of merit for audio D/A converters because it takes into account both harmonic distortion and all noise sources within a specified measurement bandwidth. The average value of the distortion and noise is referred to as THD+N.

For the PCM1753/54/55, THD+N is measured with a full-scale, 1-kHz digital sine wave as the test stimulus at the input of the DAC. The digital generator is set to 24-bit audio word length and a sampling frequency of 44.1 kHz or 96 kHz. The digital generator output is taken from the unbalanced S/PDIF connector of the measurement system. The S/PDIF data is transmitted via a coaxial cable to the digital audio receiver on the DEM-DAI1753 demo board. The receiver is then configured to output 24-bit data in either I^2S or left-justified data format. The DAC audio interface format is programmed to match the receiver output format. The analog output is then taken from the DAC post filter and connected to the analog analyzer input of the measurement system. The analog input is band limited using filters resident in the analyzer. The resulting THD+N is measured by the analyzer and displayed by the measurement system.

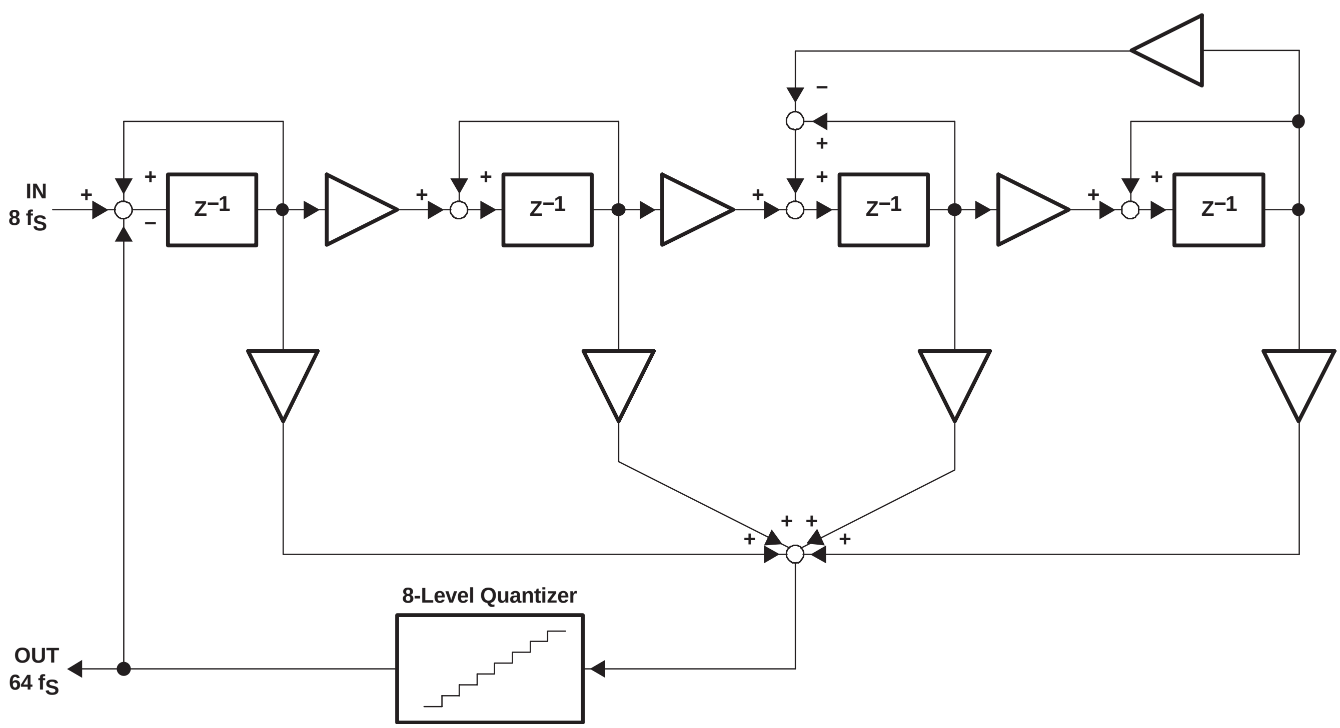


Figure 32. Eight-Level Delta-Sigma Modulator

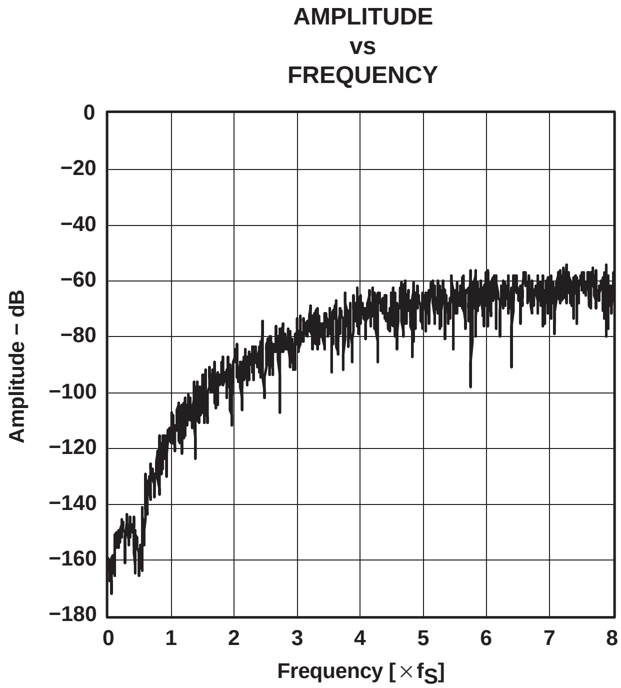


Figure 33. Quantization Noise Spectrum (× 64 Oversampling)

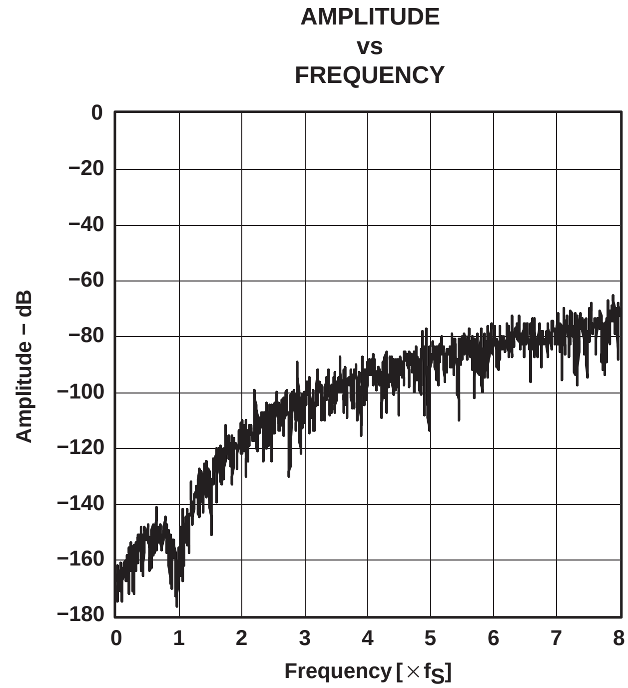


Figure 34. Quantization Noise Spectrum (× 128 Oversampling)

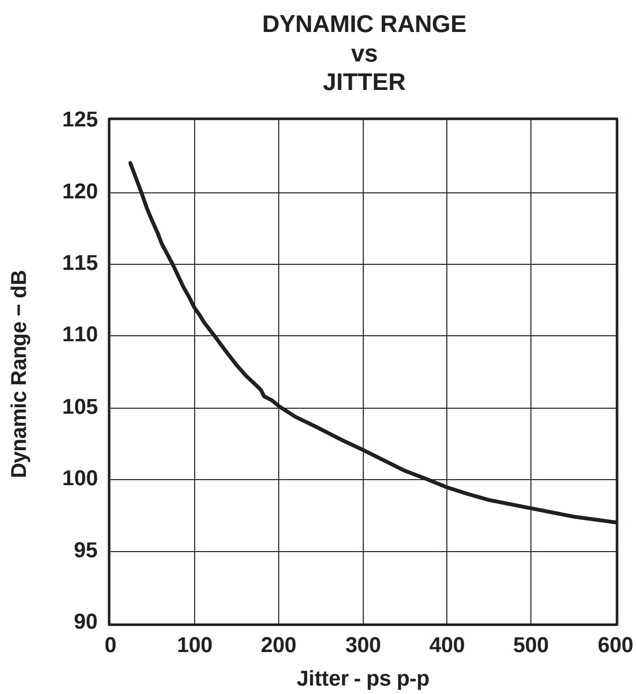


Figure 35. Jitter Dependence (× 64 Oversampling)

Dynamic Range

Dynamic range is specified as A-weighted THD+N measured with a −60-dB full-scale, 1-kHz digital sine wave stimulus at the input of the D/A converter. This measurement is designed to give a good indicator of how the DAC performs given a low-level input signal.

The measurement setup for the dynamic range measurement is shown in Figure 37, and is similar to the THD+N test setup discussed previously. The differences include the band limit filter selection, the additional A-weighting filter, and the −60-dB FS input level.

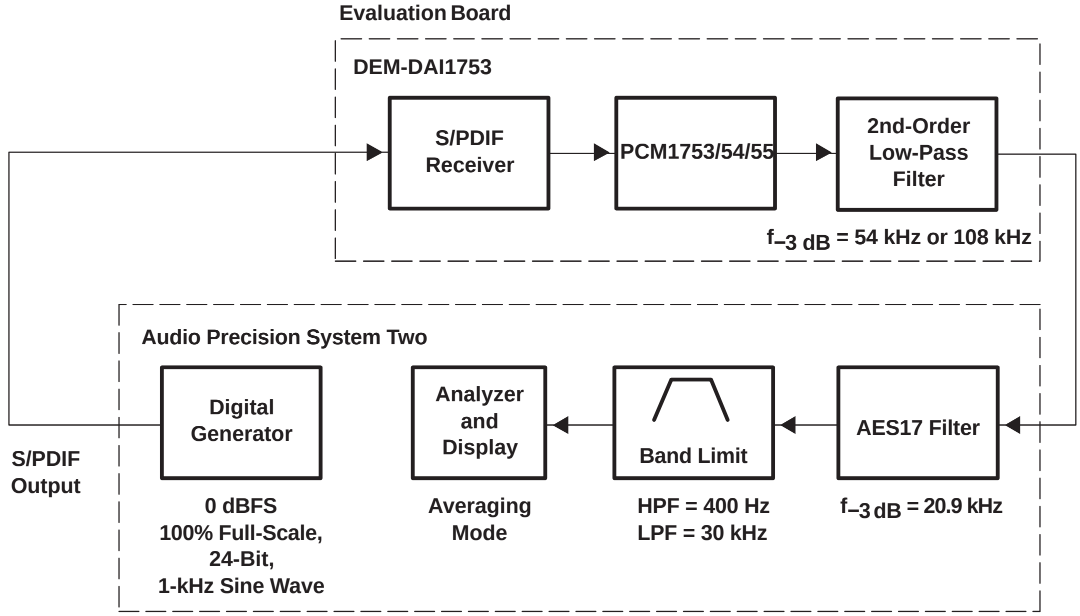


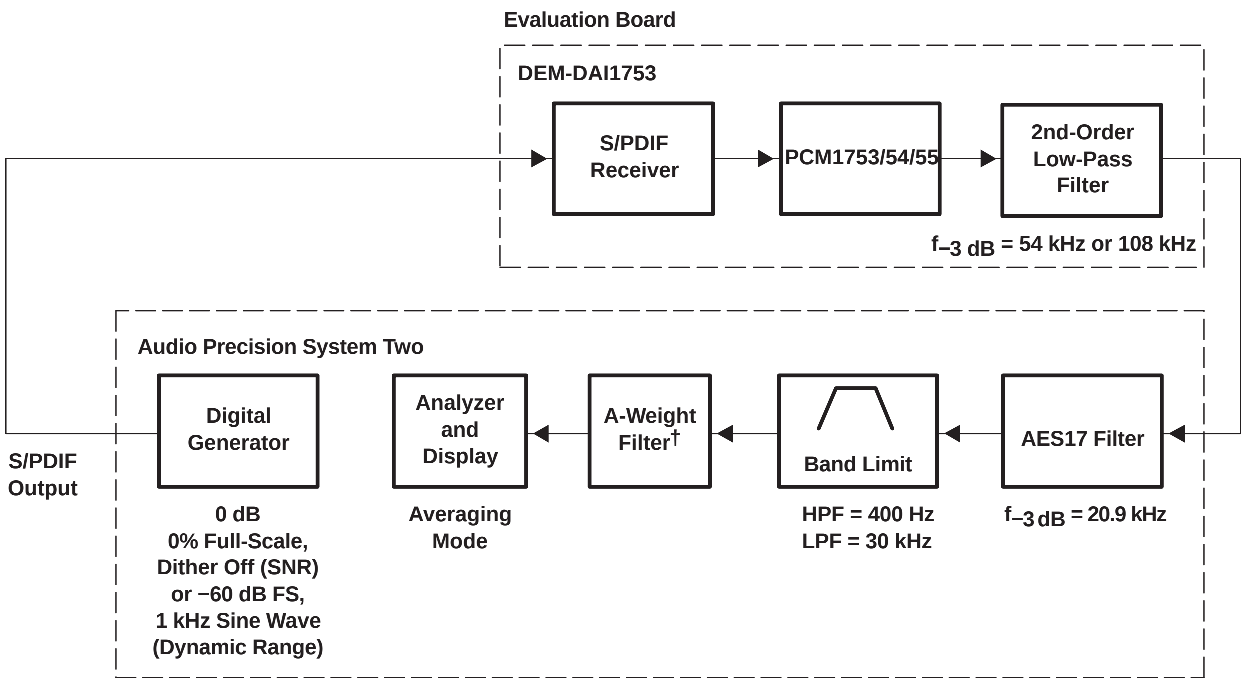
Figure 36. Test Setup for THD+N Measurement

Idle Channel Signal-to-Noise Ratio

The SNR test provides a measure of the noise floor of the D/A converter. The input to the D/A is all-0s data, and the dither function of the digital generator must be disabled to ensure an all-0s data stream at the input of the D/A converter.

The measurement setup for SNR is identical to that used for dynamic range, with the exception of the input signal level.

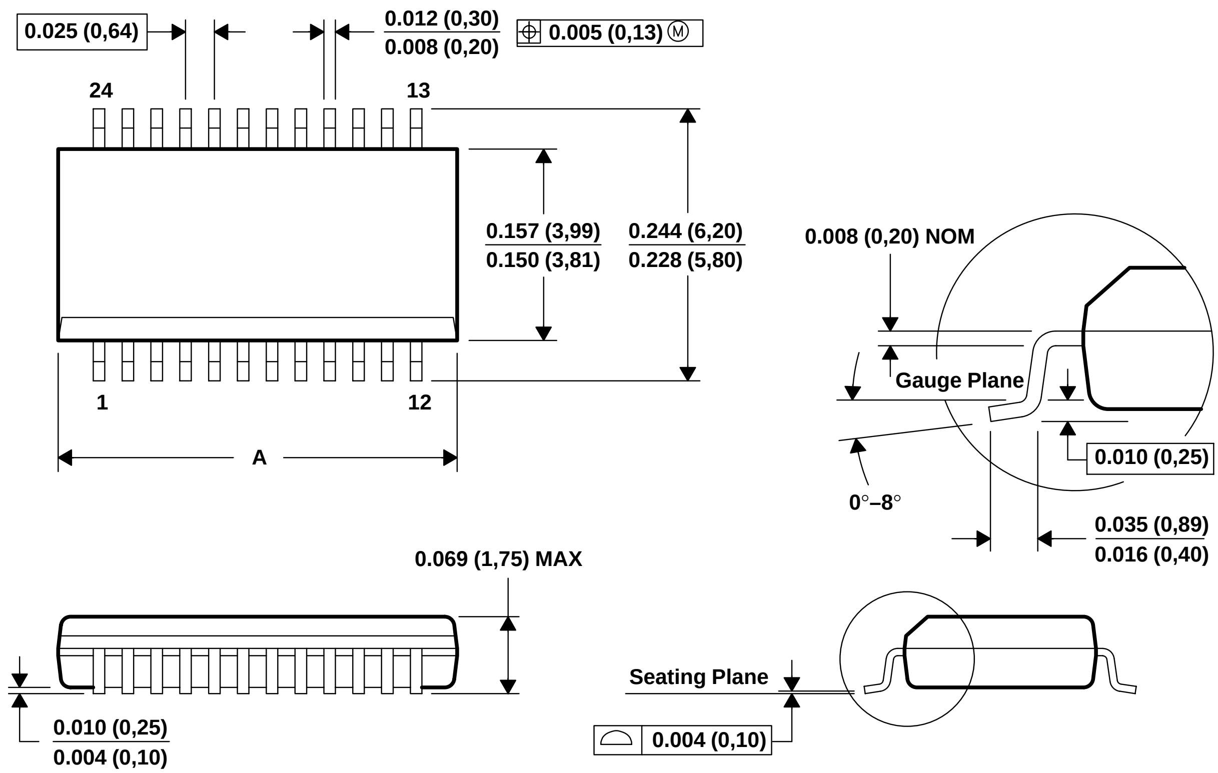
(See the notes provided in Figure 37).



† Results without A-Weighting are approximately 3 dB worse.

Figure 37. Test Setup for Dynamic Range and SNR Measurement

DBQ (R–PDSO–G)** **PLASTIC SMALL–OUTLINE PACKAGE**



PINS ** / DIM	16	20	24	28
A MAX	0.197 (5,00)	0.344 (8,74)	0.344 (8,74)	0.394 (10,01)
A MIN	0.189 (4,80)	0.337 (8,56)	0.337 (8,56)	0.386 (9,80)
D M0–137 VARIATION	AB	AD	AE	AF

4073301/F 02/02

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–137.

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