

# IRS2112(-1,-2,S)PbF

## HIGH AND LOW SIDE DRIVER

### Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage,  $dV/dt$  immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V logic compatible
- Separate logic supply range from 3.3 V to 20 V
- Logic and power ground +/- 5 V offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs
- RoHS compliant

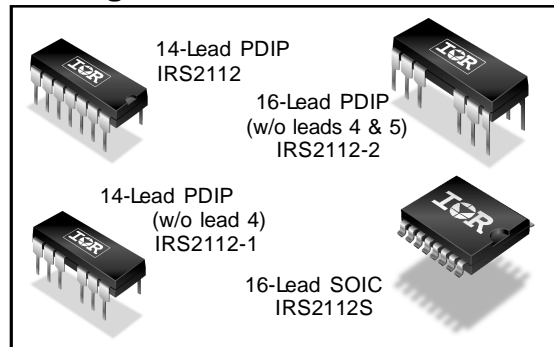
### Description

The IRS2112 is a high voltage, high speed power MOSFET and IGBT driver with independent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

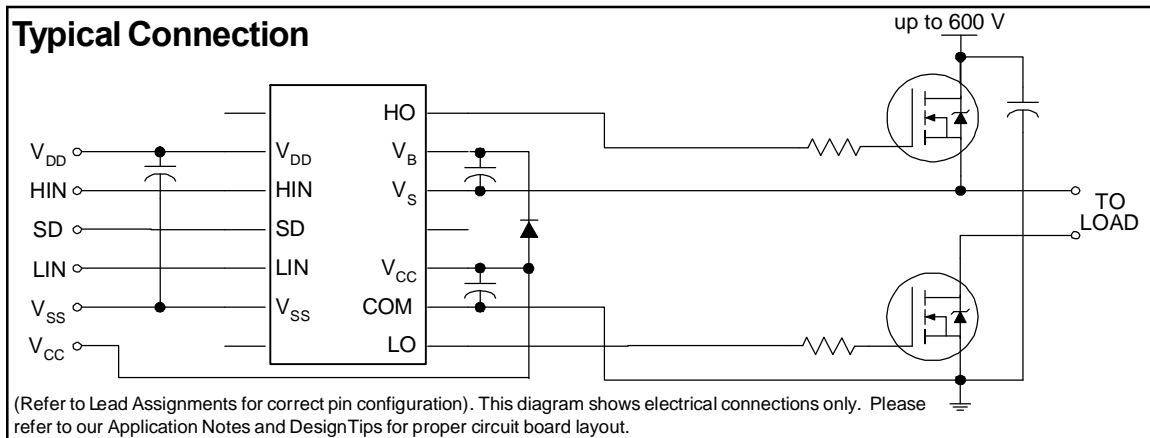
### Product Summary

$V_{\text{OFFSET}}$	600 V max.
$I_{\text{O}+/-}$	200 mA / 440 mA
$V_{\text{OUT}}$	10 V - 20 V
$t_{\text{on/off}}$ (typ.)	135 ns & 105 ns
Delay Matching	30 ns

### Packages



### Typical Connection



## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figs. 28 through 35.

Symbol	Definition	Min.	Max.	Units	
V <sub>B</sub>	High-side floating supply voltage	-0.3	625	V	
V <sub>S</sub>	High-side floating supply offset voltage	V <sub>B</sub> - 25	V <sub>B</sub> + 0.3		
V <sub>HO</sub>	High-side floating output voltage	V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3		
V <sub>CC</sub>	Low-side fixed supply voltage	-0.3	25		
V <sub>LO</sub>	Low-side output voltage	-0.3	V <sub>CC</sub> + 0.3		
V <sub>DD</sub>	Logic supply voltage	-0.3	V <sub>SS</sub> + 25		
V <sub>SS</sub>	Logic supply offset voltage	V <sub>CC</sub> - 25	V <sub>CC</sub> + 0.3		
V <sub>IN</sub>	Logic input voltage (HIN, LIN & SD)	V <sub>SS</sub> - 0.3	V <sub>DD</sub> + 0.3		
dV <sub>S</sub> /dt	Allowable offset supply voltage transient (Fig. 2)	—	50	V/ns	
P <sub>D</sub>	Package power dissipation @ T <sub>A</sub> ≤ +25 °C	(14 Lead DIP)	—	1.6	W
		(16 Lead SOIC)	—	1.25	
R <sub>THJA</sub>	Thermal resistance, junction to ambient	(14 Lead DIP)	—	75	°C/W
		(16 Lead SOIC)	—	100	
T <sub>J</sub>	Junction temperature	—	150	°C	
T <sub>S</sub>	Storage temperature	-55	150		
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)	—	300		

## Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The V<sub>S</sub> and V<sub>SS</sub> offset ratings are tested with all supplies biased at 15 V differential. Typical ratings at other bias conditions are shown in Figs. 36 and 37.

Symbol	Definition	Min.	Max.	Units
V <sub>B</sub>	High-side floating supply absolute voltage	V <sub>S</sub> + 10	V <sub>S</sub> + 20	V
V <sub>S</sub>	High-side floating supply offset voltage	Note 1	600	
V <sub>HO</sub>	High-side floating output voltage	V <sub>S</sub>	V <sub>B</sub>	
V <sub>CC</sub>	Low-side fixed supply voltage	10	20	
V <sub>LO</sub>	Low-side output voltage	0	V <sub>CC</sub>	
V <sub>DD</sub>	Logic supply voltage	V <sub>SS</sub> + 3	V <sub>SS</sub> + 20	
V <sub>SS</sub>	Logic supply offset voltage	-5 (Note 2)	5	
V <sub>IN</sub>	Logic input voltage (HIN, LIN & SD)	V <sub>SS</sub>	V <sub>DD</sub>	
T <sub>A</sub>	Ambient temperature	-40	125	°C

**Note 1:** Logic operational for V<sub>S</sub> of -5 V to +600 V. Logic state held for V<sub>S</sub> of -5 V to -V<sub>BS</sub>. (Please refer to the Design Tip DT97-3 for more details).

**Note 2:** When V<sub>DD</sub> < 5 V, the minimum V<sub>SS</sub> offset is limited to -V<sub>DD</sub>.

## Dynamic Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ,  $V_{DD}$ ) = 15 V,  $C_L$  = 1000 pF,  $T_A$  = 25 °C and  $V_{SS}$  = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Fig. 3.

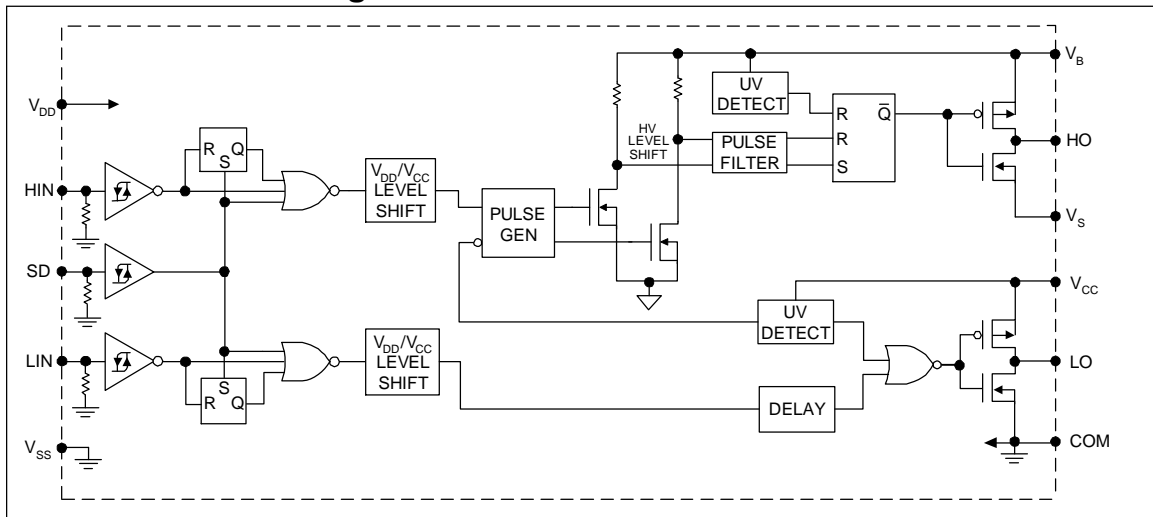
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$t_{on}$	Turn-on propagation delay	—	135	180	ns	$V_S = 0$ V
$t_{off}$	Turn-off propagation delay	—	130	160		$V_S = 600$ V
$t_{sd}$	Shutdown propagation delay	—	130	160		
$t_r$	Turn-on rise time	—	75	130		
$t_f$	Turn-off fall time	—	35	65		
MT	Delay matching, HS & LS Turn-on/off	—	—	30		

## Static Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ,  $V_{DD}$ ) = 15 V,  $T_A$  = 25 °C and  $V_{SS}$  = COM unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$ , and  $I_{IN}$  parameters are referenced to  $V_{SS}$  and are applicable to all three logic input leads: HIN, LIN, and SD. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$V_{IH}$	Logic "1" input voltage	9.5	—	—	V	$I_O = 2$ mA
$V_{IL}$	Logic "0" input voltage	—	—	6.0		
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$	—	0.05	0.2		
$V_{OL}$	Low level output voltage, $V_O$	—	0.02	0.1		
$I_{LK}$	Offset supply leakage current	—	—	50	$\mu$ A	$V_B = V_S = 600$ V
$I_{QBS}$	Quiescent $V_{BS}$ supply current	—	25	100		$V_{IN} = 0$ V or $V_{DD}$
$I_{QCC}$	Quiescent $V_{CC}$ supply current	—	80	180		$V_{IN} = V_{DD}$
$I_{QDD}$	Quiescent $V_{DD}$ supply current	—	2.0	30		$V_{IN} = 0$ V
$I_{IN+}$	Logic "1" input bias current	—	20	40		
$I_{IN-}$	Logic "0" input bias current	—	—	1.0		
$V_{BSUV+}$	$V_{BS}$ supply undervoltage positive going threshold	7.4	8.5	9.6	V	
$V_{BSUV-}$	$V_{BS}$ supply undervoltage negative going threshold	7.0	8.1	9.2		
$V_{CCUV+}$	$V_{CC}$ supply undervoltage positive going threshold	7.6	8.6	9.6		
$V_{CCUV-}$	$V_{CC}$ supply undervoltage negative going threshold	7.2	8.2	9.2		
$I_{O+}$	Output high short circuit pulsed current	200	290	—	mA	$V_O = 0$ V, $V_{IN} = V_{DD}$ $PW \leq 10$ $\mu$ s
$I_{O-}$	Output low short circuit pulsed current	420	600	—		$V_O = 15$ V, $V_{IN} = 0$ V $PW \leq 10$ $\mu$ s

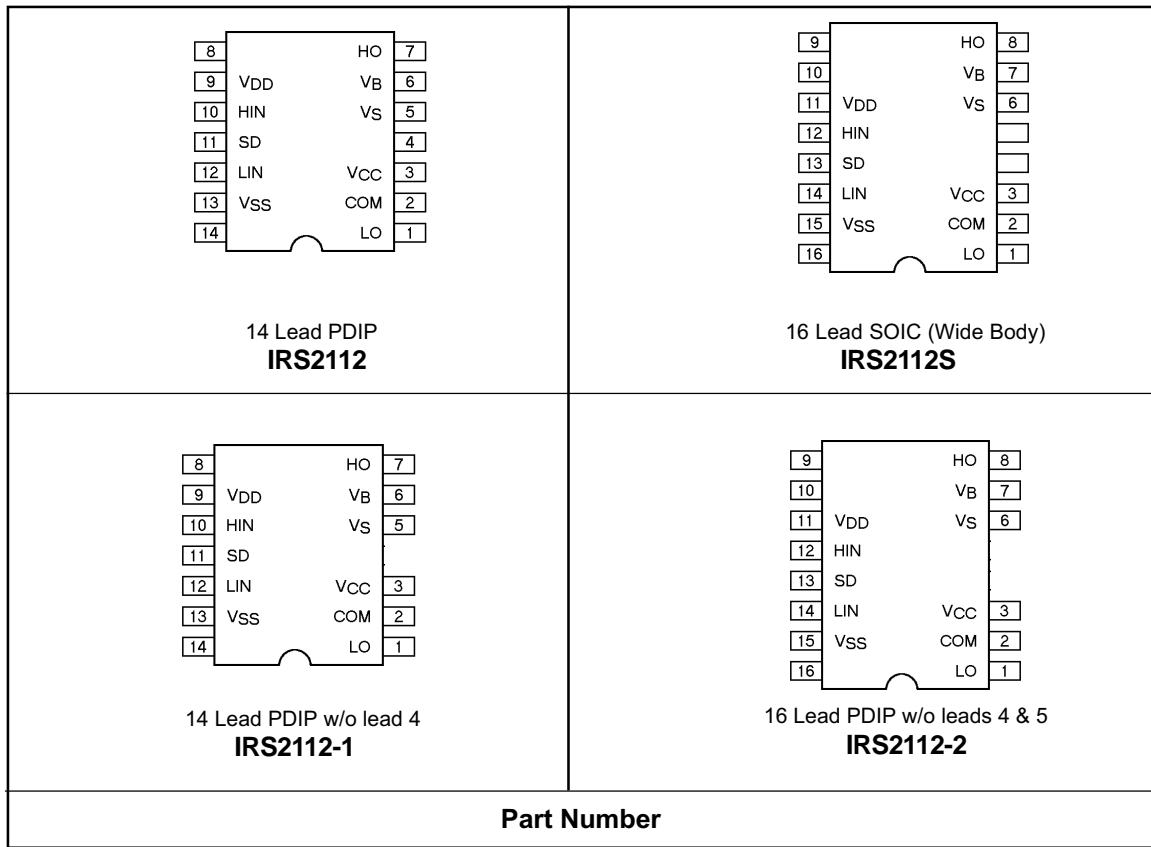
## Functional Block Diagram



## Lead Definitions

Symbol	Description
V <sub>DD</sub>	Logic supply
HIN	Logic input for high-side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low-side gate driver output (LO), in phase
V <sub>SS</sub>	Logic ground
V <sub>B</sub>	High-side floating supply
HO	High-side gate drive output
V <sub>S</sub>	High-side floating supply return
V <sub>CC</sub>	Low-side supply
LO	Low-side gate drive output
COM	Low-side return

## Lead Assignments



# IRS2112(-1,-2,S)PbF

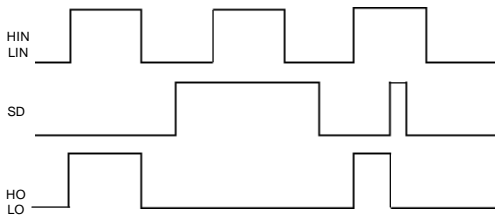


Figure 1. Input/Output Timing Diagram

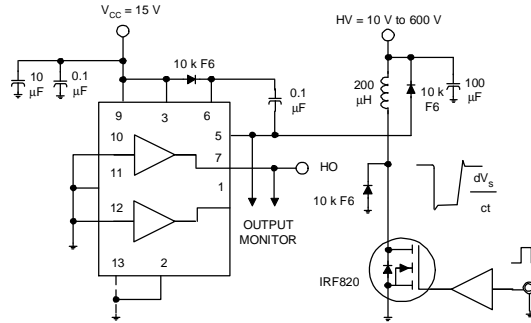


Figure 2. Floating Supply Voltage Transient Test Circuit

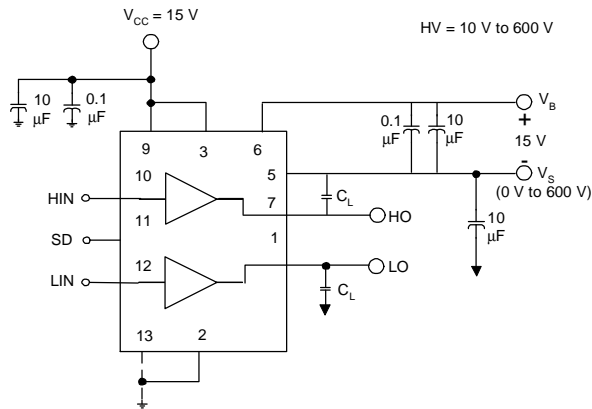


Figure 3. Switching Time Test Circuit

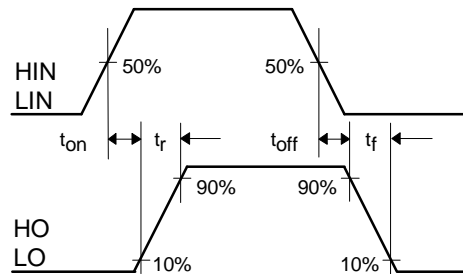


Figure 4. Switching Time Waveform Definition

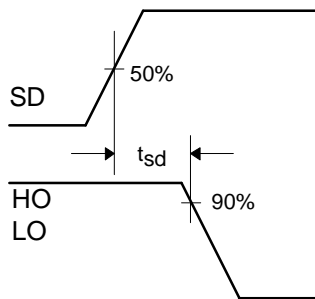


Figure 5. Shutdown Waveform Definitions

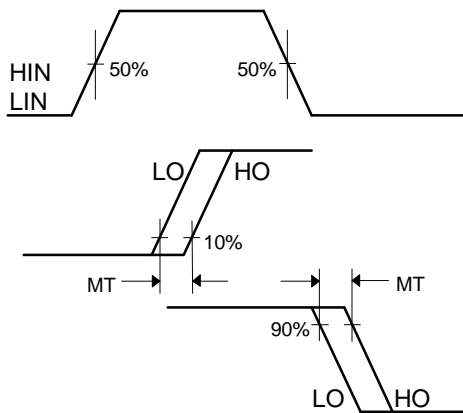
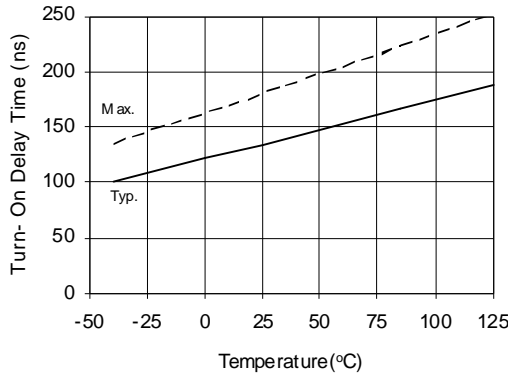
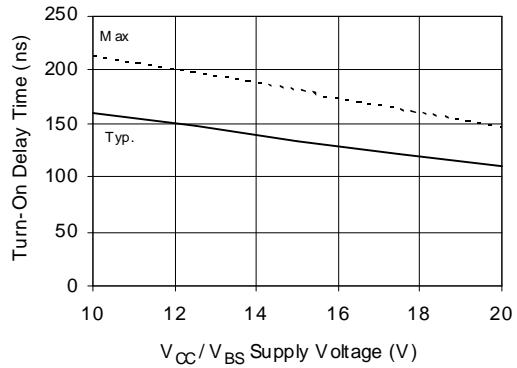


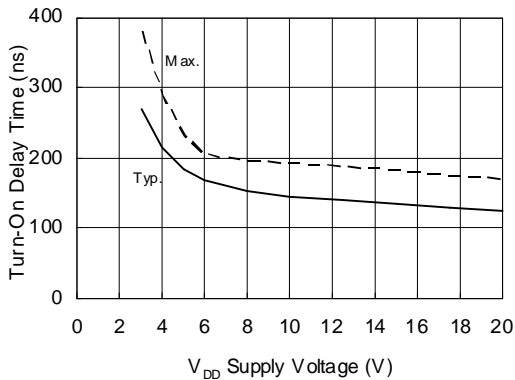
Figure 6. Delay Matching Waveform Definitions



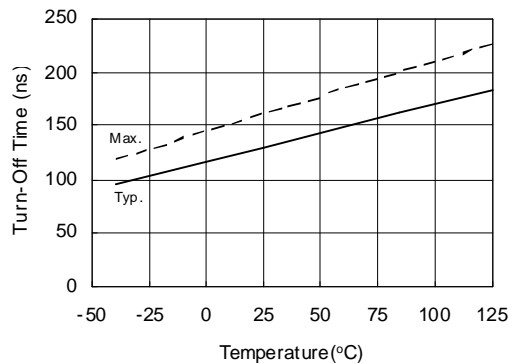
**Figure 7A. Turn-On Propagation Delay Time vs. Temperature**



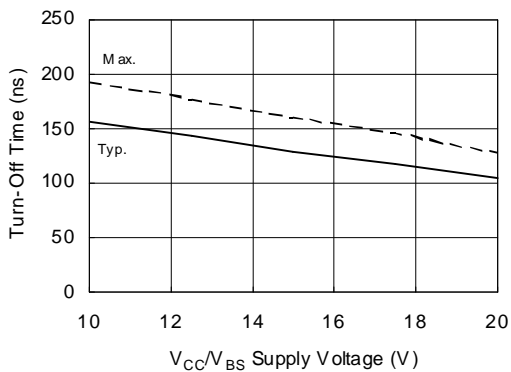
**Figure 7B. Turn-On Propagation Delay Time vs. V<sub>CC</sub>/V<sub>BS</sub> Supply Voltage**



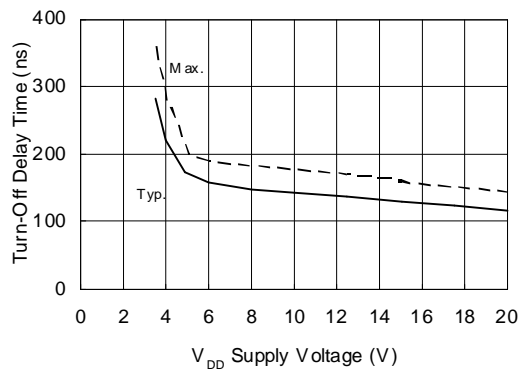
**Figure 7C. Turn-On Propagation Delay Time vs. V<sub>DD</sub> Supply Voltage**



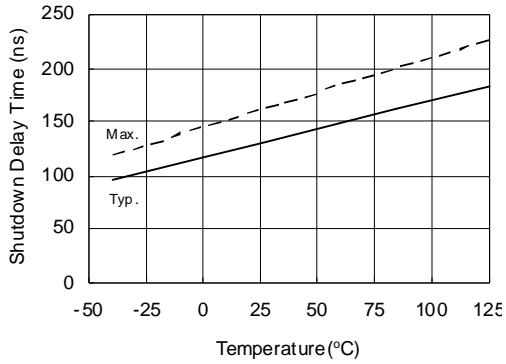
**Figure 8A. Turn-Off Propagation Delay Time vs. Temperature**



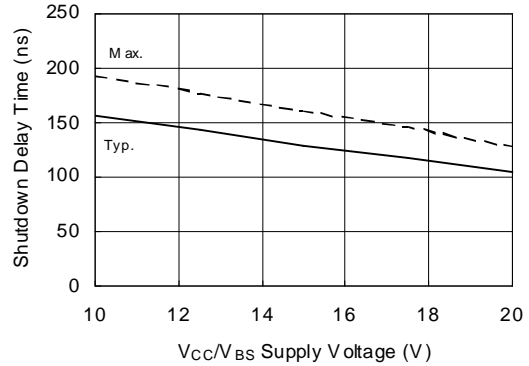
**Figure 8B. Turn-Off Propagation Delay Time vs. V<sub>CC</sub>/V<sub>BS</sub> Supply Voltage**



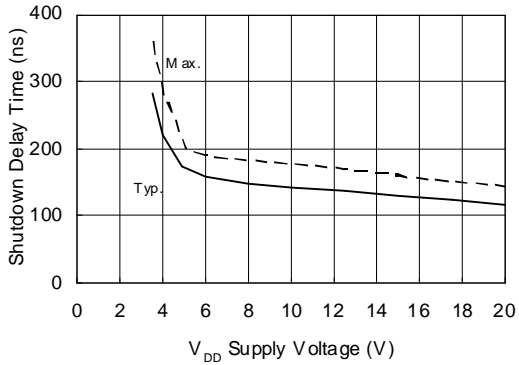
**Figure 8C. Turn-Off Propagation Delay Time vs. V<sub>DD</sub> Supply Voltage**



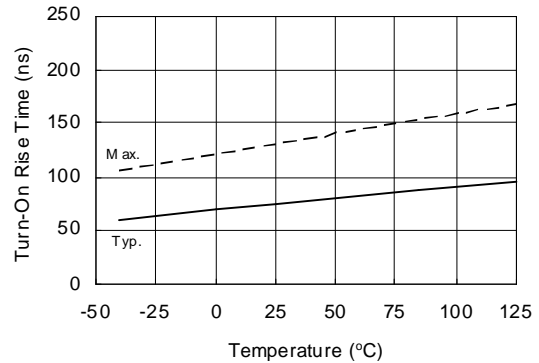
**Figure 9A. Shutdown Delay Time vs. Temperature**



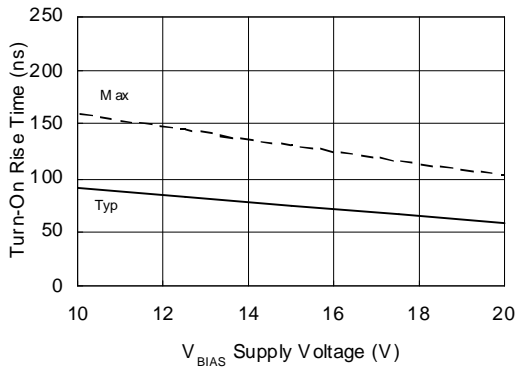
**Figure 9B. Shutdown Delay Time vs. V<sub>CC</sub>/V<sub>BS</sub> Supply Voltage**



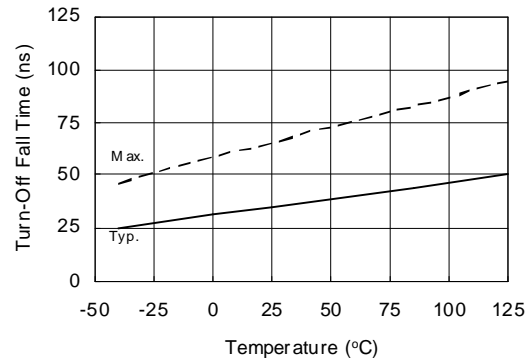
**Figure 9C. Shutdown Time vs. V<sub>DD</sub> Supply Voltage**



**Figure 10A. Turn-On Rise Time vs. Temperature**



**Figure 10B. Turn-On Rise Time vs. Voltage**



**Figure 11A. Turn-Off Fall Time vs. Temperature**



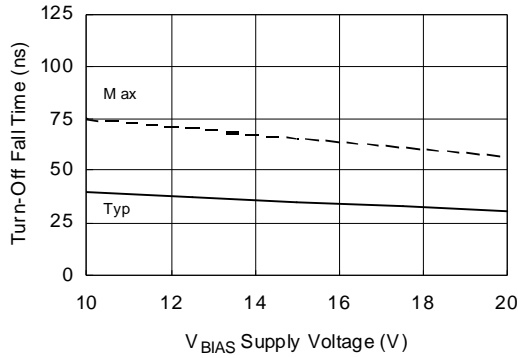


Figure 11B. Turn-Off Fall Time vs. Supply Voltage

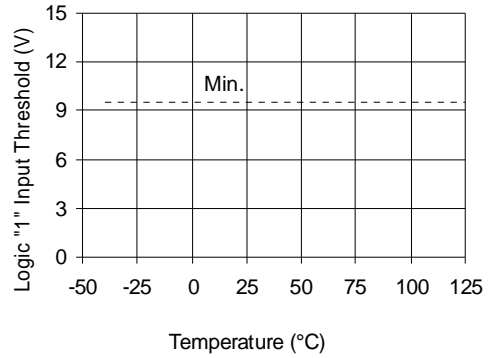


Figure 12A. Logic "1" Input Threshold vs. Temperature

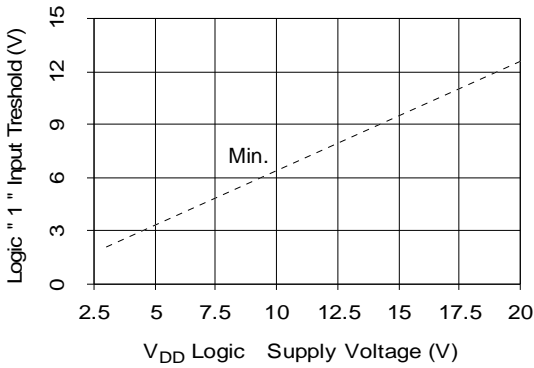


Figure 12B. Logic "1" Input Threshold vs. Voltage

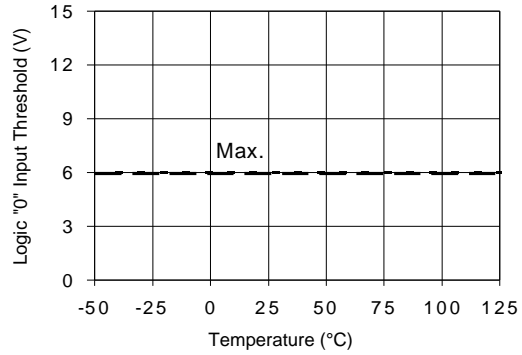


Figure 13A. Logic "0" Input Threshold vs. Temperature

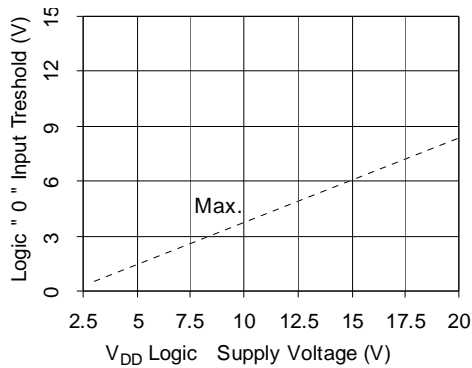


Figure 13B. Logic "0" Input Threshold vs. Voltage

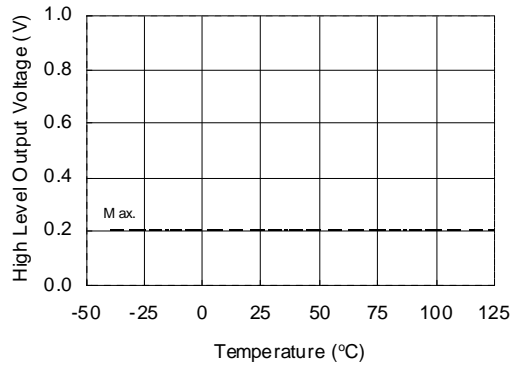
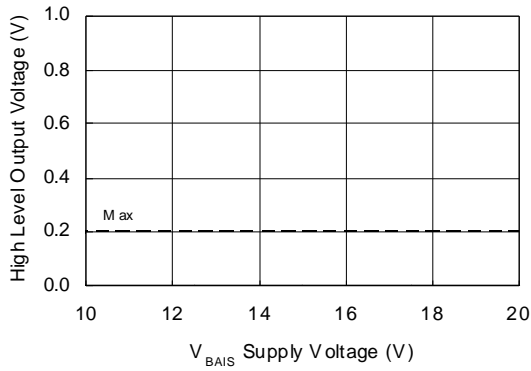
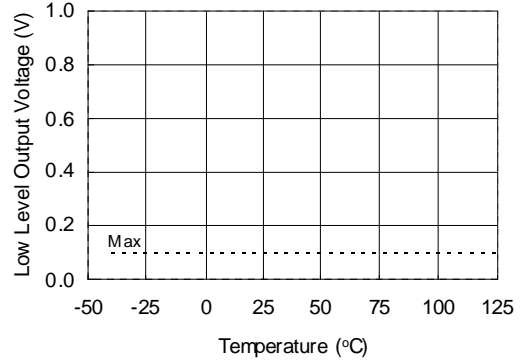


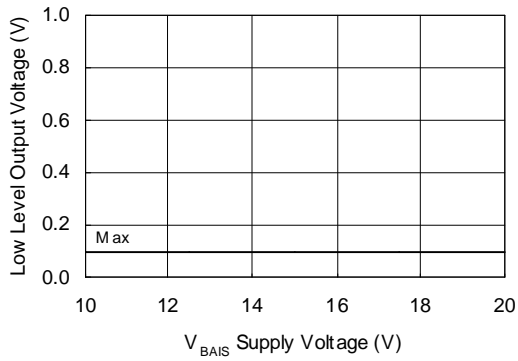
Figure 14A. High Level Output Voltage vs. Temperature (I<sub>O</sub> = 2 mA)



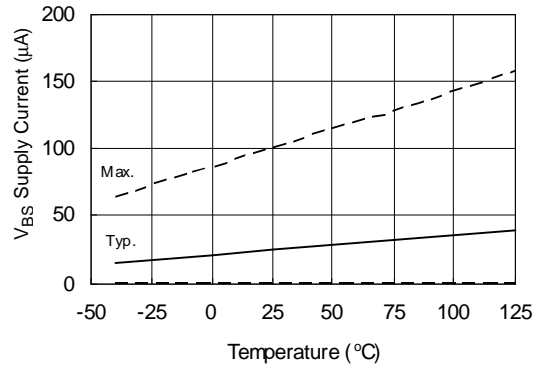
**Figure 14B. High Level Output Voltage vs. Supply Voltage ( $I_o = 2 \text{ mA}$ )**



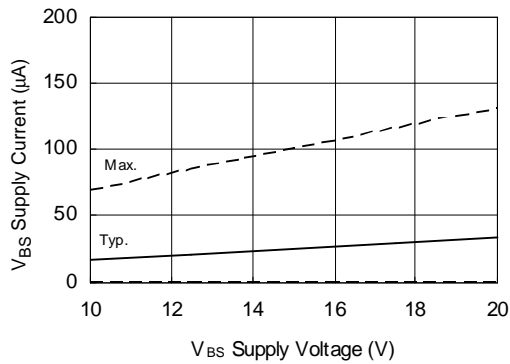
**Figure 15A. Low Level Output Voltage vs. Temperature ( $I_o = 2 \text{ mA}$ )**



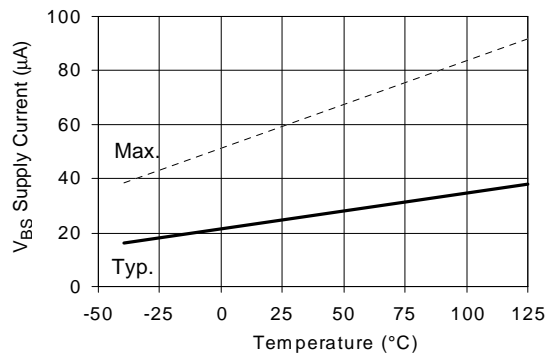
**Figure 15B. Low Level Output Voltage vs. Supply Voltage ( $I_o = 2 \text{ mA}$ )**



**Figure 16A.  $V_{BS}$  Supply Current vs. Temperature**



**Figure 16B.  $V_{BS}$  Supply Current vs. Voltage**



**Figure 17A.  $V_{BS}$  Supply Current vs. Temperature**

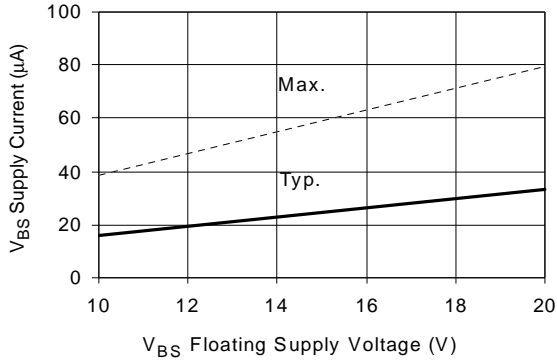


Figure 17B. V<sub>BS</sub> Supply Current vs. Voltage

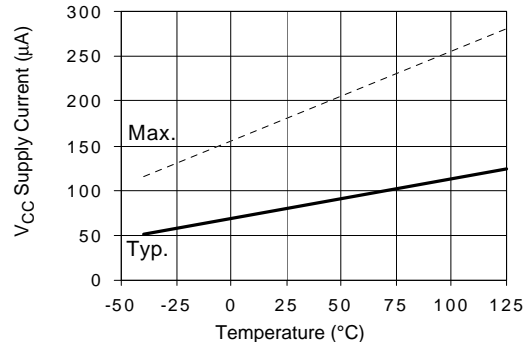


Figure 18A. V<sub>CC</sub> Supply Current vs. Temperature

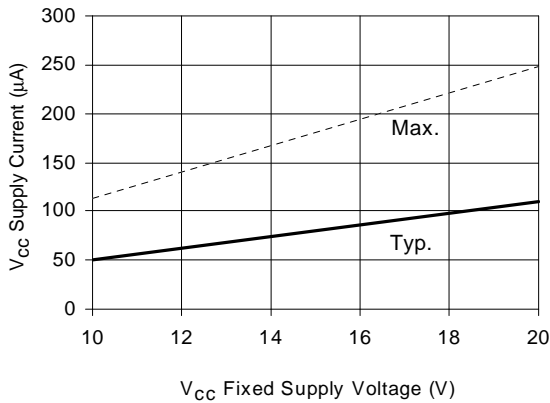


Figure 18B. V<sub>CC</sub> Supply Current vs. Voltage

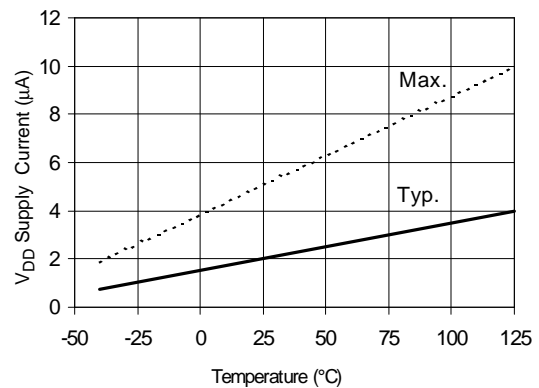


Figure 19A. V<sub>DD</sub> Supply Current vs. Temperature

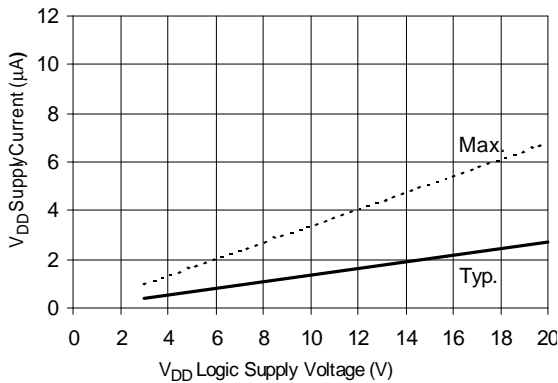


Figure 19B. V<sub>DD</sub> Supply Current vs. V<sub>DD</sub> Voltage

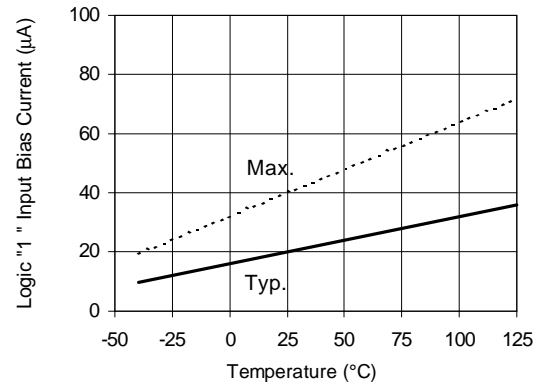
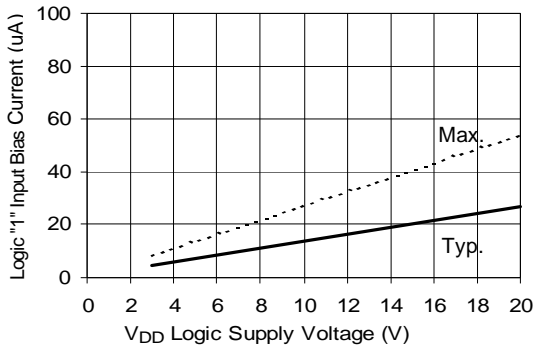
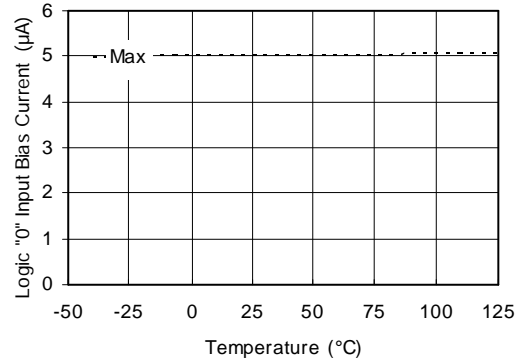


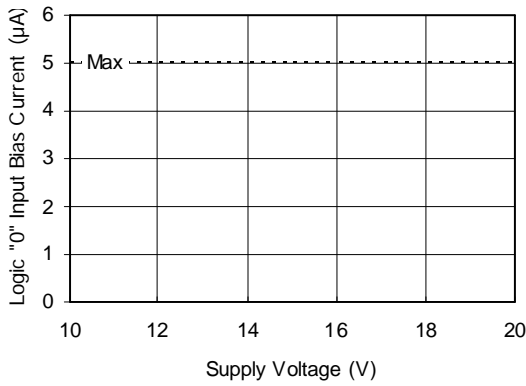
Figure 20A. Logic "1" Input Current vs. Temperature



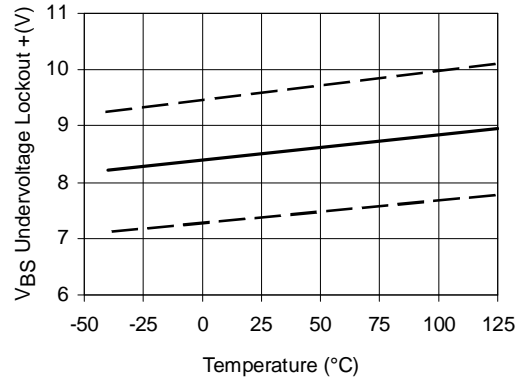
**Figure 20B. Logic "1" Input Current vs. V<sub>DD</sub> Voltage**



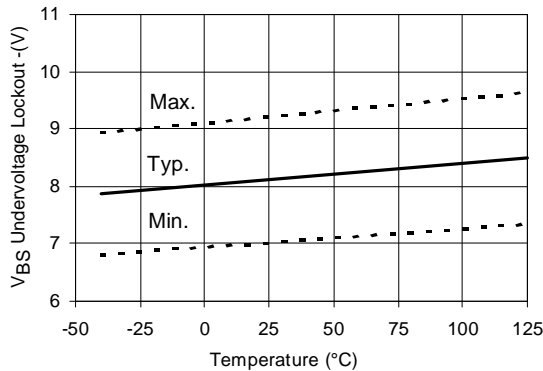
**Figure 21A. Logic "0" Input Bias Current vs. Temperature**



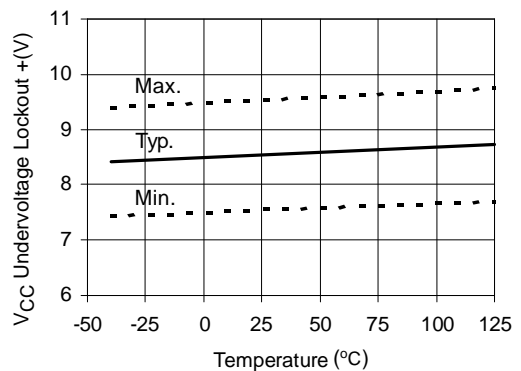
**Figure 21B. Logic "0" Input Bias Current vs. Voltage**



**Figure 22. V<sub>BS</sub> Undervoltage (+) vs. Temperature**



**Figure 23. V<sub>BS</sub> Undervoltage (-) vs. Temperature**



**Figure 24. V<sub>CC</sub> Undervoltage (-) vs. Temperature**

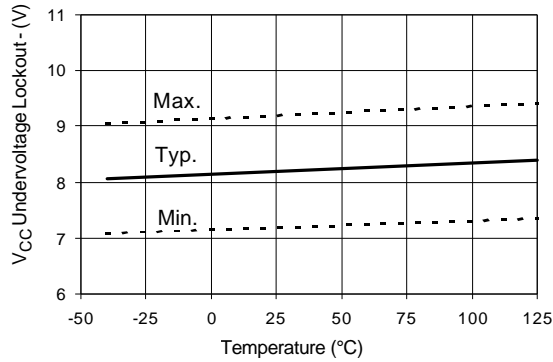


Figure 25. V<sub>CC</sub> Undervoltage (-) vs. Temperature

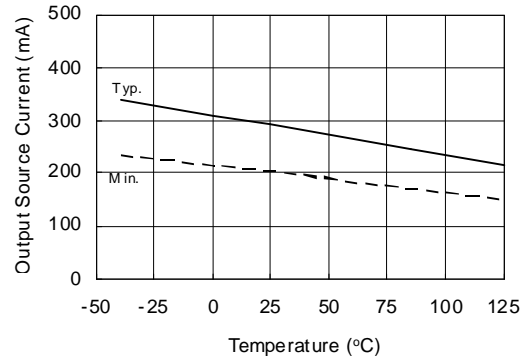


Figure 26A. Output Source Current vs. Temperature

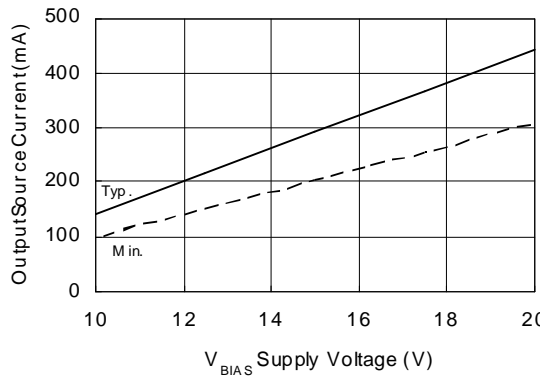


Figure 26B. Output Source Current vs. Supply Voltage

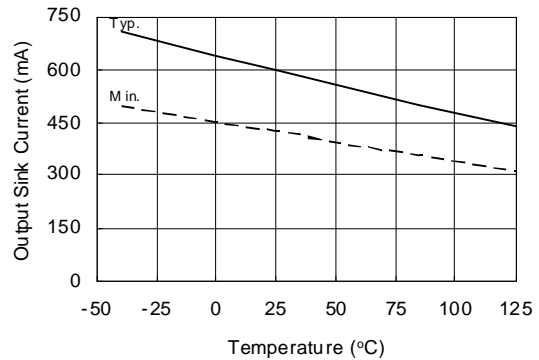


Figure 27A. Output Sink Current vs. Temperature

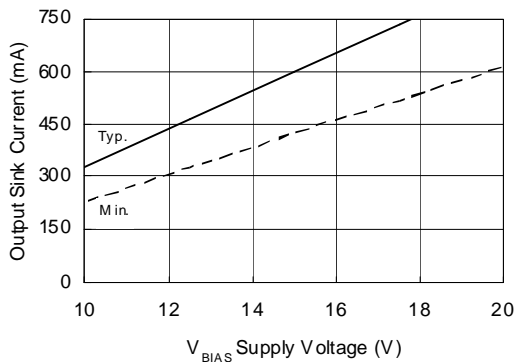
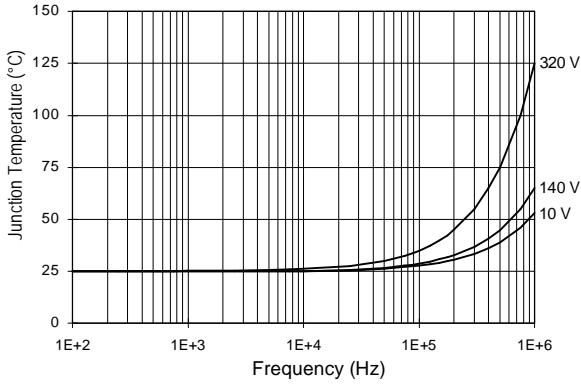
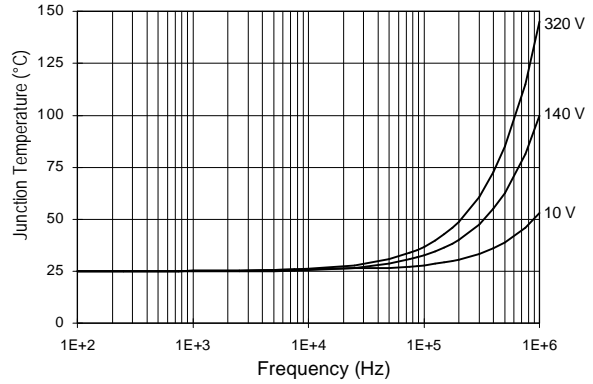


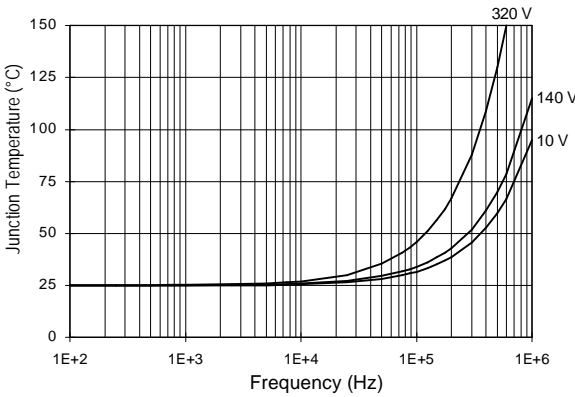
Figure 27B. Output Sink Current vs. Supply Voltage



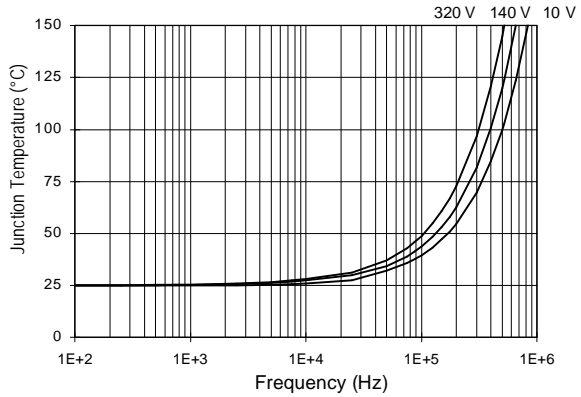
**Figure 28. IRS2112 T<sub>J</sub> vs. Frequency (IRFBC20)**  
R<sub>GATE</sub> = 33 W, V<sub>CC</sub> = 15 V



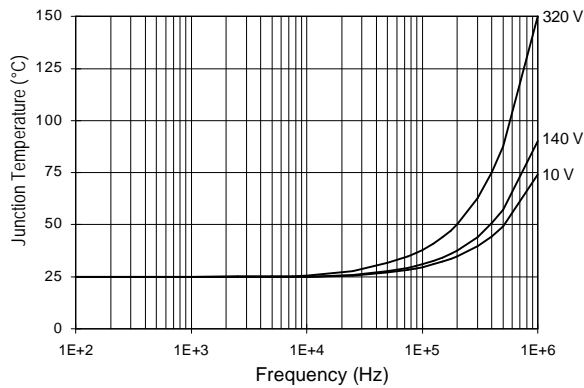
**Figure 29. IRS2112 T<sub>J</sub> vs. Frequency (IRFBC30)**  
R<sub>GATE</sub> = 22 W, V<sub>CC</sub> = 15 V



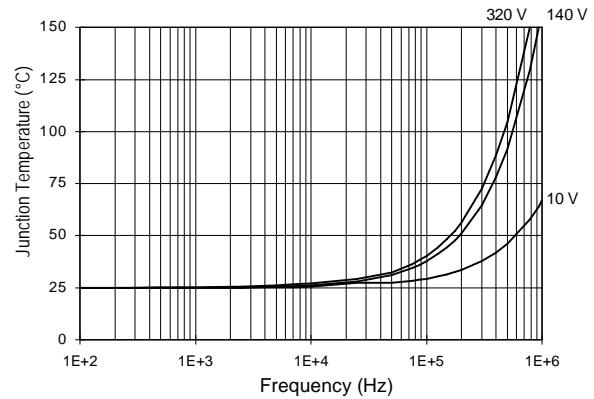
**Figure 30. IRS2112 T<sub>J</sub> vs. Frequency (IRFBC40)**  
R<sub>GATE</sub> = 15 W, V<sub>CC</sub> = 15 V



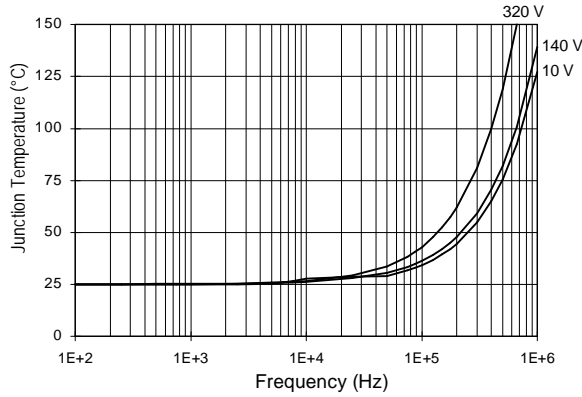
**Figure 31. IRS2112 T<sub>J</sub> vs. Frequency (IRFPE50)**  
R<sub>GATE</sub> = 10 W, V<sub>CC</sub> = 15 V



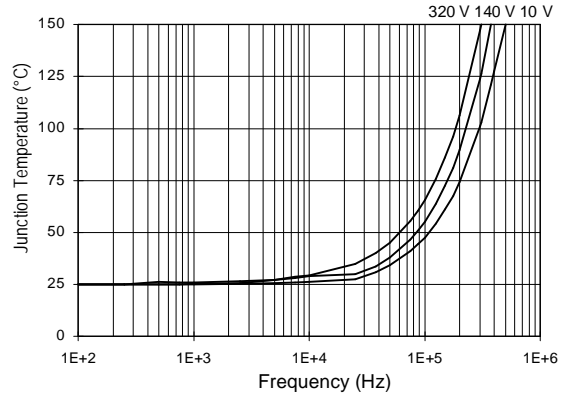
**Figure 32. IRS2112S T<sub>J</sub> vs. Frequency (IRFBC20)**  
R<sub>GATE</sub> = 33 W, V<sub>CC</sub> = 15 V



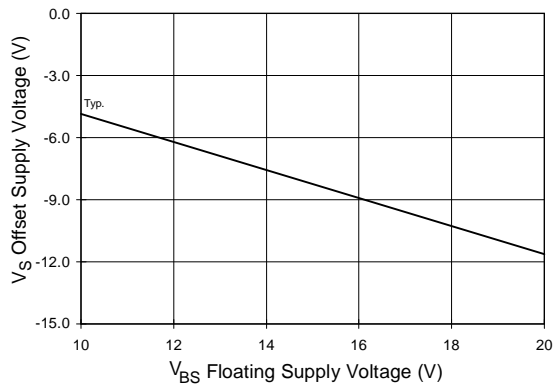
**Figure 33. IRS2112S T<sub>J</sub> vs. Frequency (IRFBC30)**  
R<sub>GATE</sub> = 22 W, V<sub>CC</sub> = 15 V



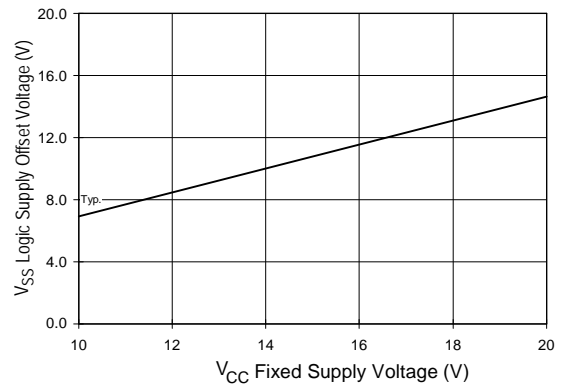
**Figure 34. IRS2112S  $T_J$  vs. Frequency (IRFBC40)**  
 $R_{GATE} = 15 W, V_{CC} = 15 V$



**Figure 35. IRS2112S  $T_J$  vs. Frequency (IRFPE50)**  
 $R_{GATE} = 10 W, V_{CC} = 15 V$

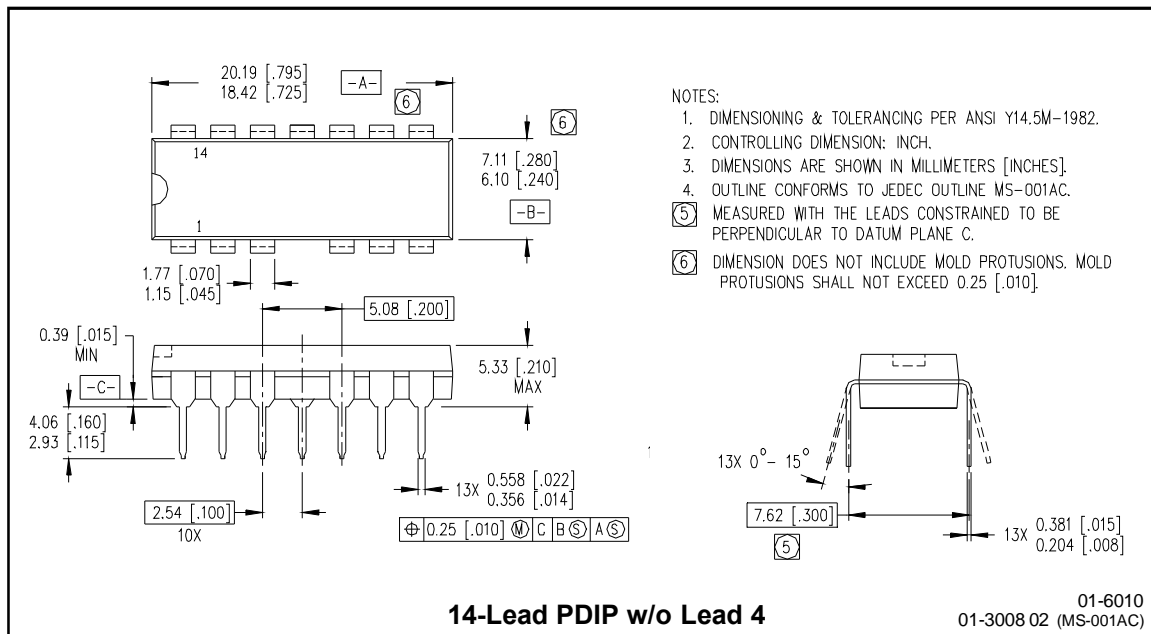
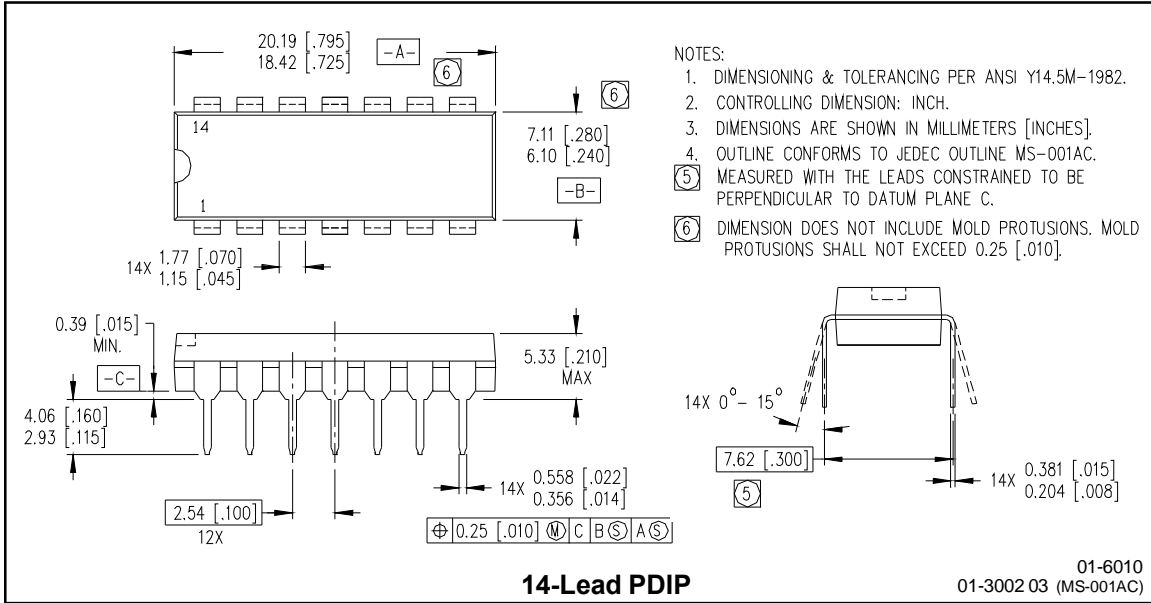


**Figure 36. Maximum  $V_S$  Negative Offset vs.  $V_{BS}$  Supply Voltage**

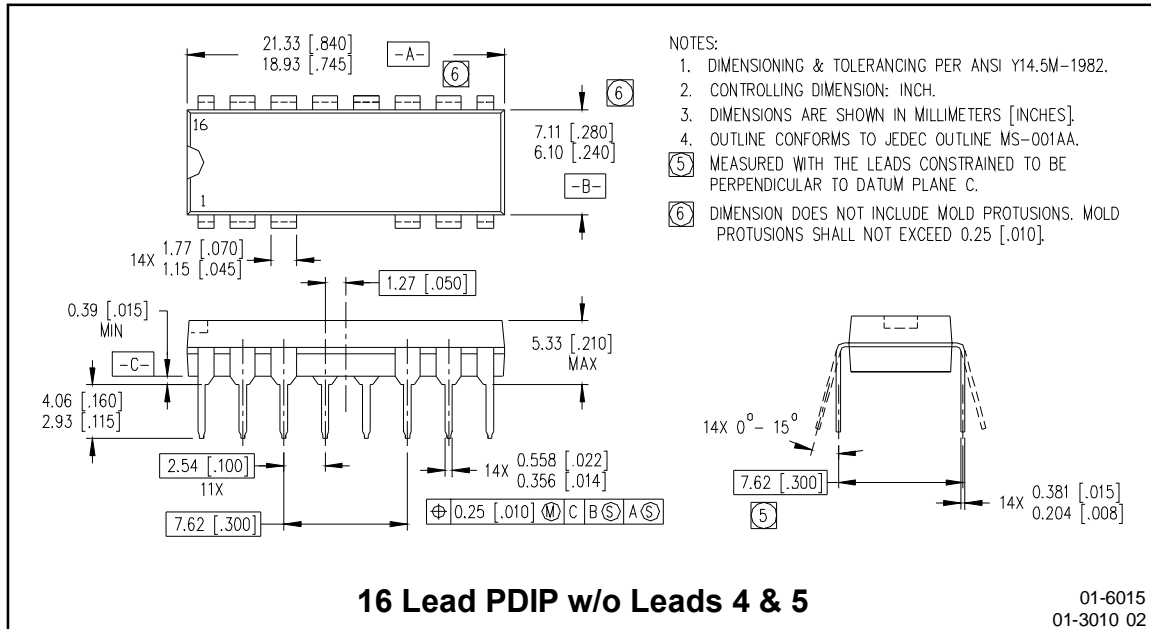


**Figure 37. Maximum  $V_{SS}$  Positive Offset vs.  $V_{CC}$  Supply Voltage**

## Case outline

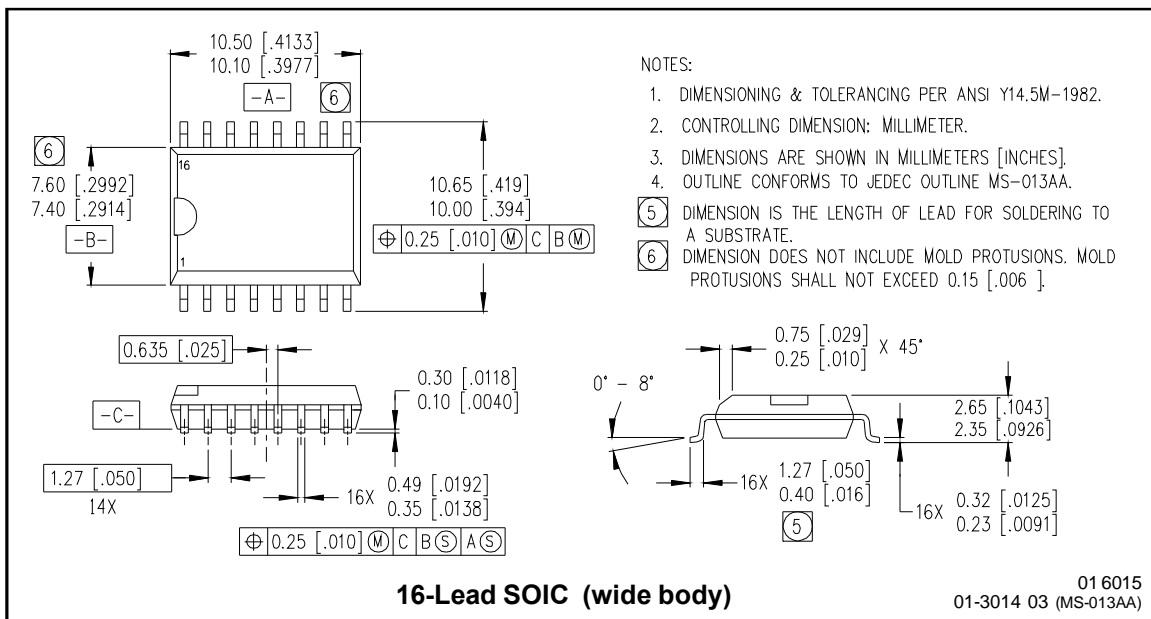






NOTES:

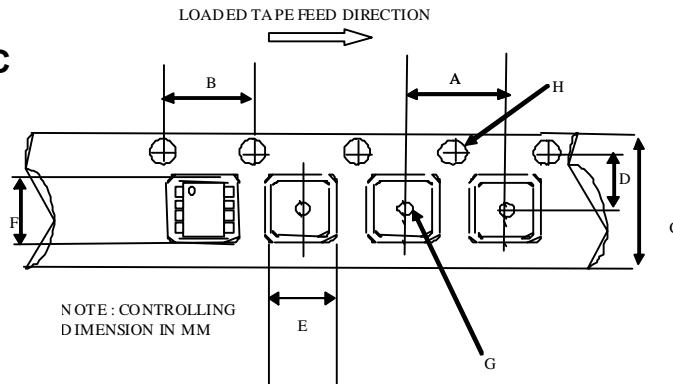
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AA.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



NOTES:

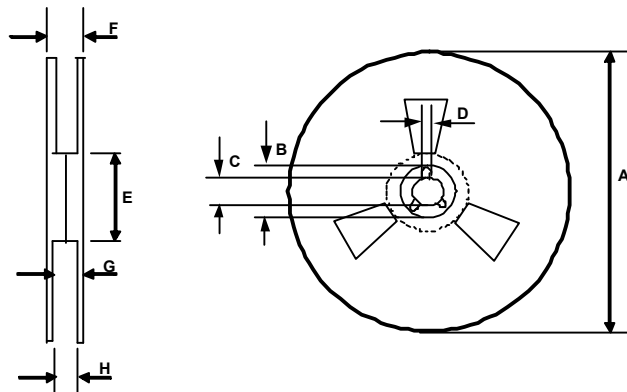
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-013AA.
5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].

## Tape & Reel 16-Lead SOIC



CARRIER TAPE DIMENSION FOR 16SOICW

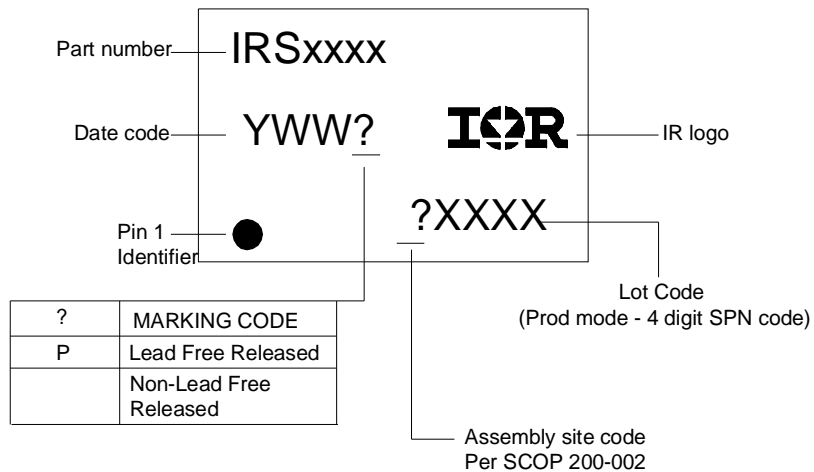
Code	Metric		Imperial	
	Min	Max	Min	Max
A	11.90	12.10	0.468	0.476
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	10.80	11.00	0.425	0.433
F	10.60	10.80	0.417	0.425
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 16SOICW

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

## LEADFREE PART MARKING INFORMATION



## ORDER INFORMATION

- 14-Lead PDIP IRS2112PbF
- 14-Lead PDIP IRS2112-1PbF
- 16-Lead PDIP IRS2112-2PbF
- 16-Lead SOIC IRS2112SPbF
- 16-Lead SOIC Tape & Reel IRS2112STRPbF