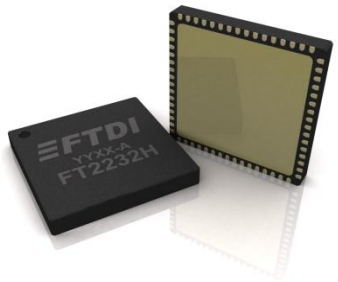
Future Technology Devices International Ltd

FT2232H Dual High Speed USB to Multipurpose UART/FIFO IC



The FT2232H is FTDI's 5th generation of USB devices. The FT2232H is a USB 2.0 High Speed (480Mb/s) to UART/FIFO IC. It has the capability of being configured in a variety of industry standard serial or parallel interfaces. The FT2232H has the following advanced features:

- Single chip USB to dual serial / parallel ports with a variety of configurations.
- Entire USB protocol handled on the chip. No USB specific firmware programming required.
- USB 2.0 High Speed (480Mbits/Second) and Full Speed (12Mbits/Second) compatible.
- Dual Multi-Protocol Synchronous Serial Engine (MPSSE) to simplify synchronous serial protocol (USB to JTAG, I^2C, SPI or bit-bang) design.
- Dual independent UART or FIFO ports configurable using MPSSEs.
- Independent Baud rate generators.
- RS232/RS422/RS485 UART Transfer Data Rate up to 12Mbaud. (RS232 Data Rate limited by external level shifter).
- USB to parallel FIFO transfer data rate up to 8 Mbyte/Sec.
- Single channel synchronous FIFO mode for transfers > 25 Mbytes/Sec
- CPU-style FIFO interface mode simplifies CPU interface design.
- MCU host bus emulation mode configuration option.
- Fast Opto-Isolated serial interface option.
- FTDI's royalty-free Virtual Com Port (VCP) and Direct (D2XX) drivers eliminate the requirement for USB driver development in most cases.
- Adjustable receive buffer timeout.
- Option for transmit and receive LED drive signals on each channel.
- Enhanced bit-bang Mode interface option with RD# and WR# strobes
- FT245B-style FIFO interface option with bi-directional data bus and simple 4 wire handshake interface.
- Highly integrated design includes +1.8V LDO regulator for VCORE, integrated POR function and on chip clock multiplier PLL (12MHz – 480MHz).
- Asynchronous serial UART interface option with full hardware handshaking and modem interface signals.
- Fully assisted hardware or X-On / X-Off software handshaking.
- UART Interface supports 7/8 bit data, 1/2 stop bits, and Odd/Even/Mark/Space/No Parity.
- Auto-transmit enable control for RS485 serial applications using TXDEN pin.
- Operational configuration mode and USB Description strings configurable in external EEPROM over the USB interface.
- Configurable I/O drive strength (4, 8, 12 or 16mA) and slew rate.
- Low operating and USB suspend current.
- Supports bus powered, self powered and high-power bus powered USB configurations.
- UHCI/OHCI/EHCI host controller compatible.
- USB Bulk data transfer mode (512 byte packets in High Speed mode).
- +1.8V (chip core) and +3.3V I/O interfacing (+5V Tolerant).
- Extended -40°C to 85°C industrial operating temperature range.
- Compact 64-LD Lead Free LQFP or QFN package
- +3.3V single supply operating voltage range.
- ESD protection for FT2232H IO's:
  Human Body Model (HBM) ±2kV,
  Machine Mode (MM) ±200V,
  Charge Device Model (CDM) ±500V,
  Latch-up free.

1 Typical Applications

- Single chip USB to dual channel UART (RS232, RS422 or RS485).
- Single chip USB to dual channel FIFO.
- Single chip USB to dual channel JTAG.
- Single chip USB to dual channel SPI.
- Single chip USB to dual channel I2C.
- Single chip USB to dual channel Bit-Bang.
- Single chip USB to dual combination of any of above interfaces.
- Single chip USB to Fast Serial Optic Interface.
- Single chip USB to CPU target interface (as memory), double and independent.
- Single chip USB to Host Bus Emulation (as CPU).
- PDA to USB data transfer
- USB Smart Card Readers
- USB Instrumentation
- USB Industrial Control
- USB MP3 Player Interface
- USB FLASH Card Reader / Writers
- Set Top Box PC - USB interface
- USB Digital Camera Interface
- USB Bar Code Readers

1.1 Driver Support

The FT2232H requires USB drivers (listed below) , available free from **http://www.ftdichip.com**, which are used to make the FT2232H appear as a virtual COM port (VCP). This allows the user to communicate with the USB interface via a standard PC serial emulation port (for example TTY). Another FTDI USB driver, the D2XX driver, can also be used with application software to directly access the FT2232H through a DLL.

Royalty free VIRTUAL COM PORT (VCP) DRIVERS for...

- Windows 2000, Server 2003, Server 2008
- Windows XP and XP 64-bit
- Windows Vista and Vista 64-bit
- Windows XP Embedded
- Windows CE 4.2, 5.0, 5.2 and 6.0
- Mac OS-X
- Linux (2.6.9 or later)
- Windows 7 and Windows 7 64-bit

Royalty free D2XX *Direct* Drivers (USB Drivers + DLL S/W Interface)

- Windows 2000, Server 2003, Server 2008
- Windows XP and XP 64-bit
- Windows Vista and Vista 64-bit
- Windows XP Embedded
- Windows CE 4.2, 5.0, 5.2 and 6.0
- Linux (2.4 or later) and Linux x86_64
- Windows 7 and Windows 7 64-bit

For driver installation, please refer to the application note:

- **AN_107, "Advanced Driver Options".**
- **AN_103, "FTDI Drivers Installation Guide for VISTA".**
- **AN_119, "FTDI Drivers Installation Guide for Windows7".**
- **AN_104, "FTDI Drivers Installation Guide for WindowsXP".**

The following additional installation guides application notes and technical notes are also available:

- **AN_113, "Interfacing FT2232H Hi-Speed Devices To I2C Bus".**
- **AN_109 – "Programming Guide for High Speed FTCI2C DLL"**
- **AN_110 – "Programming Guide for High Speed FTCJTAG DLL"**
- **AN_111 – "Programming Guide for High Speed FTCSPI DLL"**
- **AN 113 – "Interfacing FT2232H Hi-Speed Devices To I2C Bus"**
- **AN114 – "Interfacing FT2232H Hi-Speed Devices To SPI Bus"**
- **AN135 – MPSSE Basics**
- **AN108 - Command Processor For MPSSE and MCU Host Bus Emulation Modes**
- **TN_104, "Guide to Debugging Customers Failed Driver Installation"**

1.2 Part Numbers

Part Number	Package
FT2232HL-xxxx	64 Pin LQFP
FT2232HQ-xxxx	64 Pin QFN

Note: Packaging code for xxxx is:

- Reel: Taped and Reel (LQFP =1000 pcs per reel, QFN =4000 pcs per reel)

-Tray: Tray packing, (LQFP =160 pcs per tray, QFN =260 pcs per tray)

Please refer to section 8 for all package mechanical parameters.

1.3 USB Compliant

The FT2232H is fully compliant with the USB 2.0 specification and has been given the USB-IF Test-ID (TID) 40720019.

The timing of the rise/fall time of the USB signals is not only dependant on the USB signal drivers, it is also dependant system and is affected by factors such as PCB layout, external components and any transient protection present on the USB signals. For USB compliance these may require a slight adjustment. This timing can be modified through a programmable setting stored in the same external EEPROM that is used for the USB descriptors. Timing can also be changed by adding appropriate passive components to the USB signals.

2 FT2232H Block Diagram

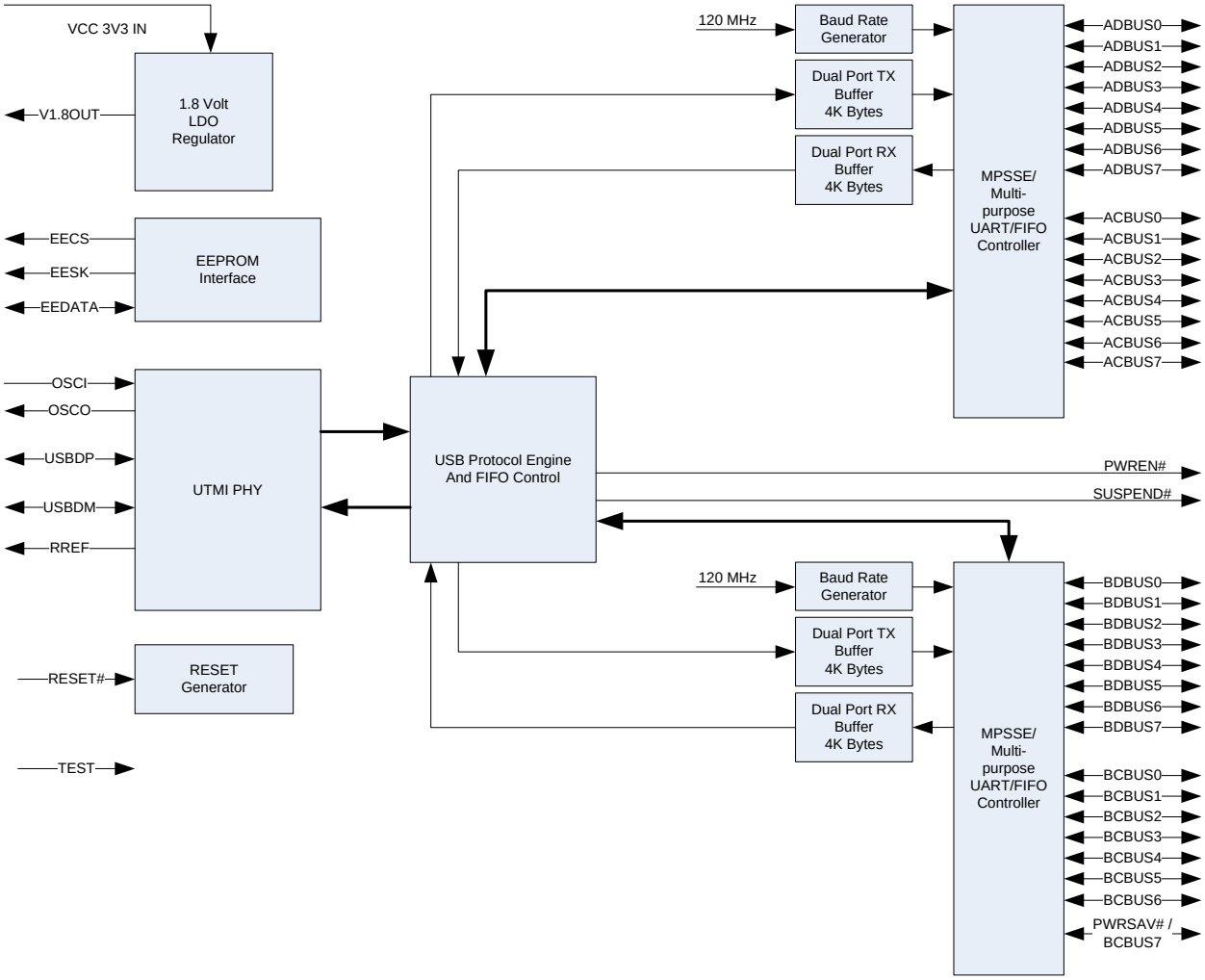


Figure 2.1 FT2232H Block Diagram

For a description of each function please refer to Section 4.

Table of Contents

3 Device Pin Out and Signal Description

The 64-pin LQFP and 64-pin QFN have the same pin numbering for specific functions. This pin numbering is illustrated in the schematic symbol shown in **Figure 3.1**.

3.1 64-Pin LQFP and 64-Pin QFN Package Schematic Symbol

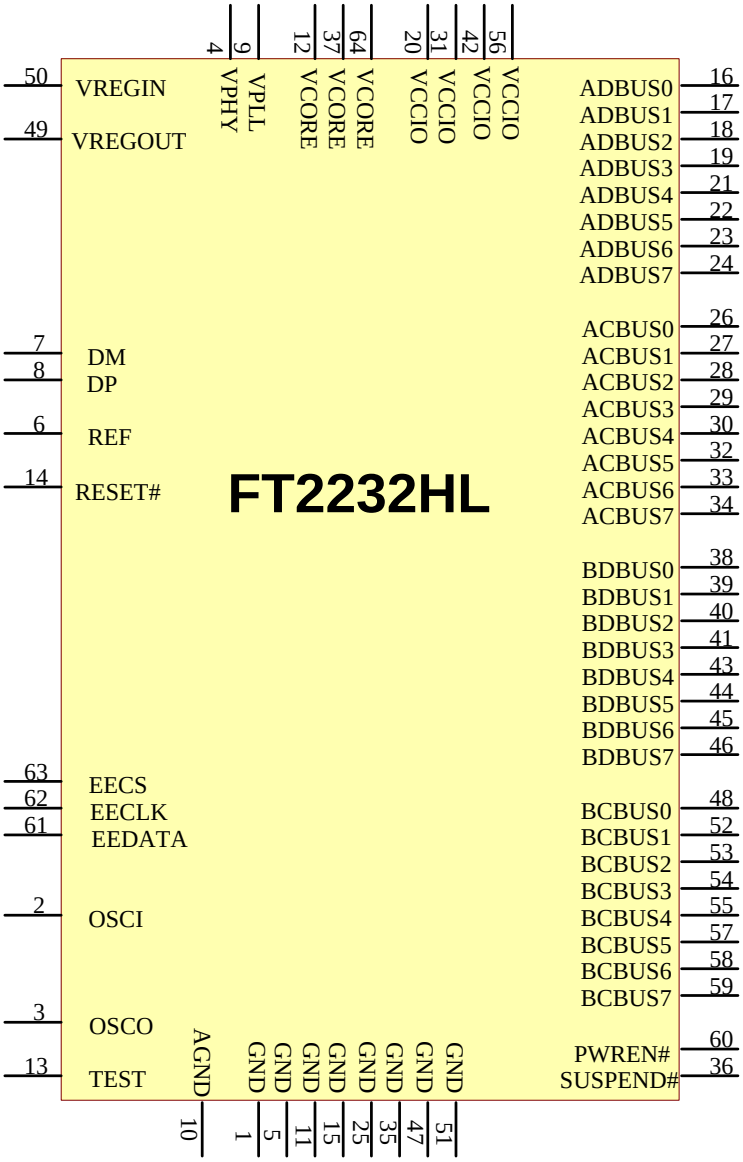


Figure 3.1 FT2232H Schematic Symbol

3.2 FT2232H Pin Descriptions

This section describes the operation of the FT2232H pins. Both the LQFP and the QFN packages have the same function on each pin. The function of many pins is determined by the configuration of the FT2232H. The following table details the function of each pin dependent on the configuration of the interface. Each of the functions are described in the following table (Note: The convention used throughout this document for active low signals is the signal name followed by a #).

Pins marked ** default to tri-stated inputs with an internal 75KΩ (approx) pull up resistor to VCCIO.

FT2232H										
Pin		Pin functions (depends on configuration)								
Pin #	Pin Name	ASYNC Serial (RS232)	245 FIFO SYNC	245 FIFO	ASYNC Bit-bang	SYNC Bit-bang	MPSSE	Fast Serial interface	CPU Style FIFO	Host Bus Emulation
		Channel A								
16	ADBUS0	TXD	D0	D0	D0	D0	TCK/SK	USES CHANNEL B	D0	AD0
17	ADBUS1	RXD	D1	D1	D1	D1	TDI/DO		D1	AD1
18	ADBUS2	RTS#	D2	D2	D2	D2	TDO/DI		D2	AD2
19	ADBUS3	CTS#	D3	D3	D3	D3	TMS/CS		D3	AD3
21	ADBUS4	DTR#	D4	D4	D4	D4	GPIOL0		D4	AD4
22	ADBUS5	DSR#	D5	D5	D5	D5	GPIOL1		D5	AD5
23	ADBUS6	DCD#	D6	D6	D6	D6	GPIOL2		D6	AD6
24	ADBUS7	RI#	D7	D7	D7	D7	GPIOL3		D7	AD7
26	ACBUS0	TXDEN	RXF#	RXF#	**	**	GPIOH0		CS#	A8
27	ACBUS1	**	TXE#	TXE#	WRSTB#	WRSTB#	GPIOH1		A0	A9
28	ACBUS2	**	RD#	RD#	RDSTB#	RDSTB#	GPIOH2		RD#	A10
29	ACBUS3	RXLED#	WR#	WR#	**	**	GPIOH3		WR#	A11
30	ACBUS4	TXLED#	SIWUA	SIWUA	SIWUA	SIWUA	GPIOH4		SIWUA	A12
32	ACBUS5	**	CLKOUT	**	**	**	GPIOH5		**	A13
33	ACBUS6	**	OE#	**	**	**	GPIOH6		**	A14
34	ACBUS7	**	**	**	**	**	GPIOH7		**	A15
		Channel B								
38	BDBUS0	TXD		D0	D0	D0	TCK/SK	FSDI	D0	CS#
39	BDBUS1	RXD		D1	D1	D1	TDI/DO	FSCLK	D1	ALE
40	BDBUS2	RTS#		D2	D2	D2	TDO/DI	FSDO	D2	RD#
41	BDBUS3	CTS#		D3	D3	D3	TMS/CS	FSCTS	D3	WR#
43	BDBUS4	DTR#		D4	D4	D4	GPIOL0		D4	IORDY
44	BDBUS5	DSR#		D5	D5	D5	GPIOL1		D5	CLKOUT
45	BDBUS6	DCD#		D6	D6	D6	GPIOL2		D6	I/O0
46	BDBUS7	RI#		D7	D7	D7	GPIOL3		D7	I/O1
48	BCBUS0	TXDEN		RXF#	**	**	GPIOH0		CS#	**
52	BCBUS1	**		TXE#	WRSTB#	WRSTB#	GPIOH1		A0	**
53	BCBUS2	**		RD#	RDSTB#	RDSTB#	GPIOH2		RD#	**
54	BCBUS3	RXLED#		WR#	**	**	GPIOH3		WR#	**
55	BCBUS4	TXLED#		SIWUB	SIWUB	SIWUB	GPIOH4	SIWUB	SIWUB	**
57	BCBUS5	**		**	**	**	GPIOH5		**	**
58	BCBUS6	**		**	**	**	GPIOH6		**	**
59	BCBUS7	PWRSAV#	PWRSAV#	PWRSAV#	PWRSAV#	PWRSAV#	GPIOH7	PWRSAV#	PWRSAV#	PWRSAV#
60	PWREN#	PWREN#	PWREN#	PWREN#	PWREN#	PWREN#	PWREN#	PWREN#	PWREN#	PWREN#
36	SUSPEND#	SUSPEND#	SUSPEND#	SUSPEND#	SUSPEND#	SUSPEND#	SUSPEND#	SUSPEND#	SUSPEND#	SUSPEND#
		Configuration memory interface								
63	EECS									

62	EECLK	
61	EEDATA	

3.3 Common Pins

The operation of the following FT2232H pins are the same regardless of the configured mode:-

Pin No.	Name	Type	Description
12,37,64	VCORE	POWER Input	+1.8V input. Core supply voltage input.
20,31,42,56	VCCIO	POWER Input	+3.3V input. I/O interface power supply input. Failure to connect all VCCIO pins will result in failure of the device.
9	VPLL	POWER Input	+3.3V input. Internal PHY PLL power supply input. It is recommended that this supply is filtered using an LC filter.
4	VPHY	POWER Input	+3.3V Input. Internal USB PHY power supply input. Note that this cannot be connected directly to the USB supply. A +3.3V regulator must be used. It is recommended that this supply is filtered using an LC filter.
50	VREGIN	POWER Input	+3.3V Input. Integrated 1.8V voltage regulator input.
49	VREGOUT	POWER Output	+1.8V Output. Integrated voltage regulator output. Connect to VCORE with 3.3uF filter capacitor.
10	AGND	POWER Input	0V Analog ground.
1,5,11,15, 25,35,47,51	GND	POWER Input	0V Ground input.

Table 3.1 Power and Ground

Pin No.	Name	Type	Description
2	OSCI	INPUT	Oscillator input.
3	OSCO	OUTPUT	Oscillator output.
6	REF	INPUT	Current reference – connect via a 12KΩ resistor @ 1% to GND.
7	DM	INPUT	USB Data Signal Minus.
8	DP	INPUT	USB Data Signal Plus.
13	TEST	INPUT	IC test pin – for normal operation should be connected to GND.
14	RESET#	INPUT	Reset input (active low).
60	PWREN#	OUTPUT	Active low power-enable output. PWREN# = 0: Normal operation. PWREN# =1 : USB SUSPEND mode or device has not been configured. This can be used by external circuitry to power down logic when device is in USB suspend or has not been configured.
36	SUSPEND#	OUTPUT	Active low when USB is in suspend mode.
59	PWRSAV#	INPUT	USB Power Save input. This is an EEPROM configurable option used when the FT2232H is used in a self powered mode and is used to prevent forcing current down the USB lines when the host or hub is powered off. PWRSAV# = 1 : Normal Operation PWRSAV# = 0 : FT2232H forced into SUSPEND mode. PWRSAV# can be connected to GND (via a 10KΩ resistor) and another resistor (e.g. 4K7) connected to the VBUS of the USB connector. When this input goes high, then it indicates to the FT2232H that it is connected to a host PC. When the host or hub is powered down then the FT2232H is held in SUSPEND mode.

Table 3.2 Common Function pins

Pin No.	Name	Type	Description
63	EECS	I/O	EEPROM – Chip Select. Tri-State during device reset.
62	EECLK	OUTPUT	Clock signal to EEPROM. Tri-State during device reset. When not in reset, this outputs the EEPROM clock.
61	EEDATA	I/O	EEPROM – Data I/O Connect directly to Data-In of the EEPROM and to Data-Out of the EEPROM via a 2.2K resistor. Also, pull Data-Out of the EEPROM to VCC via a 10K resistor for correct operation. Tri-State during device reset.

Table 3.3 EEPROM Interface Group

3.4 Configured Pins

The following sections describe the function of the configurable pins referred to in the table given in Section 3.2 which is determined by how the FT2232H is configured.

3.4.1 FT2232H pins used in an RS232 interface

The FT2232H channel A or channel B can be configured as an RS232 interface. When configured in this mode, the pins used and the descriptions of the signals are shown in Table 3.4.

Channel A Pin No.	Channel B Pin No.	Name	Type	RS232 Configuration Description
16	***38***	TXD	OUTPUT	TXD = transmitter output
17	***39***	RXD	INPUT	RXD = receiver input
18	***40***	RTS#	OUTPUT	RTS# = Ready To send handshake output
19	***41***	CTS#	INPUT	CTS# = Clear To Send handshake input
21	***43***	DTR#	OUTPUT	DTR# = Data Transmit Ready modem signaling line
22	***44***	DSR#	INPUT	DSR# = Data Set Ready modem signaling line
23	***45***	DCD#	INPUT	DCD# = Data Carrier Detect modem signaling line
24	***46***	RI#	INPUT	RI# = Ring Indicator Control Input. When the Remote Wake up option is enabled in the EEPROM, taking RI# low can be used to resume the PC USB Host controller from suspend. (Also see note 1, 2, 3 in section 4.12)
26	***48***	TXDEN	OUTPUT	TXDEN = (TTL level). For use with RS485 level converters.
29	***54***	RXLED#	OUTPUT	RXLED = Receive signaling output. Pulses low when receiving data (RXD) via USB. This should be connected to an LED.
30	***55***	TXLED#	OUTPUT	TXLED = Transmit signaling output. Pulses low when transmitting data (TXD) via USB. This should be connected to an LED.

Table 3.4 Channel A and Channel B RS232 Configured Pin Descriptions

3.4.2 FT2232H pins used in an FT245 Style Synchronous FIFO Interface

The FT2232H only channel A can be configured as a FT245 style synchronous FIFO interface. When configured in this mode, the pins used and the descriptions of the signals are shown in Table 3.5. To enter this mode the external EEPROM must be set to make port A 245 mode. A software command (Set Bit Mode option) is then sent by the application to the FTDI driver to tell the chip to enter single channel synchronous FIFO mode. In this mode the 'B' channel is not available as all resources have been switched onto channel A. In this mode, data is written or read on the rising edge of the CLKOUT.

Channel A Pin No.	Name	Type	FT245 Configuration Description
24,23,22,21, 19,18,17,16	ADBUS[7:0]	I/O	D7 to D0 bidirectional FIFO data. This bus is normally input unless OE# is low.
26	RXF#	OUTPUT	When high, do not read data from the FIFO. When low, there is data available in the FIFO which can be read by driving RD# low. When in synchronous mode, data is transferred on every clock that RXF# and RD# are both low. Note that the OE# pin must be driven low at least 1 clock period before asserting RD# low.
27	TXE#	OUTPUT	When high, do not write data into the FIFO. When low, data can be written into the FIFO by driving WR# low. When in synchronous mode, data is transferred on every clock that TXE# and WR# are both low.
28	RD#	INPUT	Enables the current FIFO data byte to be driven onto D0...D7 when RD# goes low. The next FIFO data byte (if available) is fetched from the receive FIFO buffer each CLKOUT cycle until RD# goes high.
29	WR#	INPUT	Enables the data byte on the D0...D7 pins to be written into the transmit FIFO buffer when WR# is low. The next FIFO data byte is written to the transmit FIFO buffer each CLKOUT cycle until WR# goes high.
32	CLKOUT	OUTPUT	60 MHz Clock driven from the chip. All signals should be synchronized to this clock.
33	OE#	INPUT	Output enable when low to drive data onto D0-7. This should be driven low at least 1 clock period before driving RD# low to allow for data buffer turn-around.
30	SIWU	INPUT	The Send Immediate / WakeUp signal combines two functions on a single pin. If USB is in suspend mode (PWREN# = 1) and remote wakeup is enabled in the EEPROM , strobing this pin low will cause the device to request a resume on the USB Bus. Normally, this can be used to wake up the Host PC. During normal operation (PWREN# = 0), if this pin is strobed low any data in the device TX buffer will be sent out over USB on the next Bulk-IN request from the drivers regardless of the pending packet size. This can be used to optimize USB transfer speed for some applications. Tie this pin to VCCIO if not used. (Also see note 1, 2, 3 in section 4.12)

Table 3.5 Channel A FT245 Style Synchronous FIFO Configured Pin Descriptions

For a functional description of this mode, please refer to section 4.4 FT245 Synchronous FIFO Interface Mode Description

3.4.3 FT2232H pins used in an FT245 Style Asynchronous FIFO Interface

The FT2232H channel A or channel B can be configured as a FT245 asynchronous FIFO interface. When configured in this mode, the pins used and the descriptions of the signals are shown in Table 3.6. To enter this mode the external EEPROM must be set to make port A or B or both 245 mode. In this mode, data is written or read on the falling edge of the RD# or WR# signals.

Channel A Pin No.	Channel B Pin No.	Name	Type	FT245 Configuration Description
24,23,22,21, 19,18,17,16	46,45,44,43, 41,40,39,38	Channel A = ADBUS[7:0] Channel B = BDBUS[7:0]	I/O	D7 to D0 bidirectional FIFO data. This bus is normally input unless RD# is low.
26	48	RXF#	OUTPUT	When high, do not read data from the FIFO. When low, there is data available in the FIFO which can be read by driving RD# low. When RD# goes high again RXF# will always go high and only become low again if there is another byte to read. During reset this signal pin is tri-state, but pulled up to VCCIO via an internal 200kΩ resistor.
27	52	TXE#	OUTPUT	When high, do not write data into the FIFO. When low, data can be written into the FIFO by strobing WR# high, then low. During reset this signal pin is tri-state, but pulled up to VCCIO via an internal 200kΩ resistor.
28	53	RD#	INPUT	Enables the current FIFO data byte to be driven onto D0...D7 when RD# goes low. Fetches the next FIFO data byte (if available) from the receive FIFO buffer when RD# goes high.
29	54	WR#	INPUT	Writes the data byte on the D0...D7 pins into the transmit FIFO buffer when WR# goes from high to low.
30	55	SIWU	INPUT	The Send Immediate / WakeUp signal combines two functions on a single pin. If USB is in suspend mode (PWREN# = 1) and remote wakeup is enabled in the EEPROM , strobing this pin low will cause the device to request a resume on the USB Bus. Normally, this can be used to wake up the Host PC. During normal operation (PWREN# = 0), if this pin is strobed low any data in the device TX buffer will be sent out over USB on the next Bulk-IN request from the drivers regardless of the pending packet size. This can be used to optimize USB transfer speed for some applications. Tie this pin to VCCIO if not used. (Also see note 1, 2, 3 in section 4.12)

Table 3.6 Channel A and Channel B FT245 Style Asynchronous FIFO Configured Pin Descriptions

3.4.4 FT2232H pins used in a Synchronous or Asynchronous Bit-Bang Interface

The FT2232H channel A or channel B can be configured as a synchronous or asynchronous bit-bang interface. Bit-bang mode is a special FTDI FT2232H device mode that changes the 8 IO lines on either (or both) channels into an 8 bit bi-directional data bus. There are two types of bit-bang modes: synchronous and asynchronous.

When configured in any bit-bang mode, the pins used and the descriptions of the signals are shown in **Table 3.7**

Channel A Pin No.	Channel B Pin No.	Name	Type	Configuration Description
24,23,22,21 , 19,18,17,16	**46,45,44,43, 41,40,39,38**	**Channel A = ADBUS[7:0]** **Channel B = BDBUS[7:0]**	I/O	D7 to D0 bidirectional Bit-Bang parallel I/O data pins
27	**52**	**WRSTB#**	OUTPUT	Write strobe, active low output indicates when new data has been written to the I/O pins from the Host PC (via the USB interface).
28	**53**	**RDSTB#**	OUTPUT	Read strobe, this output rising edge indicates when data has been read from the parallel I/O pins and sent to the Host PC (via the USB interface).
30	**55**	**SIWU**	INPUT	The Send Immediate / WakeUp signal combines two functions on a single pin. If USB is in suspend mode (PWREN# = 1) and remote wakeup is enabled in the EEPROM , strobing this pin low will cause the device to request a resume on the USB Bus. Normally, this can be used to wake up the Host PC. During normal operation (PWREN# = 0), if this pin is strobed low any data in the device TX buffer will be sent out over USB on the next Bulk-IN request from the drivers regardless of the pending packet size. This can be used to optimize USB transfer speed for some applications. Tie this pin to VCCIO if not used. (Also see note 1, 2, 3 in section 4.12)

Table 3.7 Channel A and Channel B Synchronous or Asynchronous Bit-Bang Configured Pin Descriptions

For a functional description of this mode, please refer to section 4.10 Synchronous and Asynchronous Bit-Bang Interface Mode Description.

3.4.5 FT2232H pins used in an MPSSE

The FT2232H channel A and channel B each have a Multi-Protocol Synchronous Serial Engine (MPSSE). Each MPSSE can be independently configured to a number of industry standard serial interface protocols such as JTAG, I2C or SPI, or it can be used to implement a proprietary bus protocol. For example, it is possible to use one of the FT2232H's channels to connect to an SRAM configurable FPGA such as supplied by Altera or Xilinx. The FPGA device would normally be un-configured (i.e. have no defined function) at power-up. Application software on the PC could use the MPSSE to download configuration data to the FPGA over USB. This data would define the hardware function on power up. The other FT2232H channel would be available for another function. Alternatively each MPSSE can be used to control a number of GPIO pins. When configured in this mode, the pins used and the descriptions of the signals are shown Table 3.6

Channel A Pin No.	Channel B Pin No.	Name	Type	MPSSE Configuration Description
16	38	TCK/SK	OUTPUT	Clock Signal Output. For example: JTAG – TCK, Test interface clock SPI – SK, Serial Clock
17	39	TDI/DO	OUTPUT	Serial Data Output. For example: JTAG – TDI, Test Data Input SPI – DO
18	40	TDO/DI	INPUT	Serial Data Input. For example: JTAG – TDO, Test Data output SPI – DI, Serial Data Input
19	41	TMS/CS	OUTPUT	Output Signal Select. For example: JTAG – TMS, Test Mode Select SPI – CS, Serial Chip Select
21	43	GPIOL0	I/O	General Purpose input/output
22	44	GPIOL1	I/O	General Purpose input/output
23	45	GPIOL2	I/O	General Purpose input/output
24	46	GPIOL3	I/O	General Purpose input/output
26	48	GPIOH0	I/O	General Purpose input/output
27	52	GPIOH1	I/O	General Purpose input/output
28	53	GPIOH2	I/O	General Purpose input/output
29	54	GPIOH3	I/O	General Purpose input/output
30	55	GPIOH4	I/O	General Purpose input/output
32	57	GPIOH5	I/O	General Purpose input/output
33	58	GPIOH6	I/O	General Purpose input/output
34	59	GPIOH7	I/O	General Purpose input/output

Table 3.8 Channel A and Channel B MPSSE Configured Pin Descriptions

For a functional description of this mode, please refer to section 4.6 MPSSE Interface Mode Description.

3.4.6 FT2232H Pins used as a Fast Serial Interface

The FT2232H channel B can be configured for use with high-speed optical bi-directional isolated serial data transfer: Fast Serial Interface. (Not available on channel A). A proprietary FTDI protocol designed to allow galvanic isolated devices to communicate synchronously with the FT2232H using just 4 signal wires (over two dual opto-isolators), and two power lines. The peripheral circuitry controls the data transfer rate in both directions, whilst maintaining full data integrity. Maximum USB full speed data rates can be achieved. Both 'A' and 'B' channels can communicate over the same 4 wire interface if desired.

When configured in this mode, the pins used and the descriptions of the signals are shown in **Table 3.9**.

Channel B Pin No.	Name	Type	Fast Serial Interface Configuration Description
38	FSDI	INPUT	Fast serial data input.
39	FSCLK	INPUT	Fast serial clock input. Clock input to FT2232H chip to clock data in or out.
40	FSDO	OUTPUT	Fast serial data output.
41	FSCTS	OUTPUT	Fast serial Clear To Send signal output. Driven low to indicate that the chip is ready to send data

Table 3.9 Channel B Fast Serial Interface Configured Pin Descriptions

For a functional description of this mode, please refer to section 4.8 Fast Opto-Isolated Serial Interface Mode Description

3.4.7 FT2232H Pins Configured as a CPU-style FIFO Interface

The FT2232H channel A or channel B can be configured in a CPU-style FIFO interface mode which allows a CPU to interface to USB via the FT2232H. This mode is enabled in the external EEPROM.

When configured in this mode, the pins used and the descriptions of the signals are shown in **Table 3.10**

Channel A Pin No.	Channel B Pin No.	Name	Type	Fast Serial Interface Configuration Description
24,23,22,21 **,** ***19,18,17,16***	**46,45,44,43 , 41,40,39,38**	**Channel A = ADBUS[7:0]** **Channel B = BDBUS[7:0]**	I/O	D7 to D0 bidirectional data bus
26	48	CS#	INPUT	Active low chip select input
27	52	A0	INPUT	Address bit A0
28	53	RD#	INPUT	Active Low FIFO Read input
29	54	WR#	INPUT	Active Low FIFO Write input

Table 3.10 Channel A and Channel B CPU-style FIFO Interface Configured Pin Descriptions

For a functional description of this mode, please refer to section 4.9 CPU-style FIFO Interface Mode Description

3.4.8 FT2232H Pins Configured as a Host Bus Emulation Interface

The FT2232H can be used to combine channel A and channel B to be configured as a host bus emulation interface mode which emulates a standard 8048 or 8051 MCU host.

When configured in this mode, the pins used and the descriptions of the signals are shown in **Table 3.11**

Pin No.	Name	Type	Fast Serial Interface Configuration Description
24,23,22,21, 19,18,17,16	ADBUS[7:0]	I/O	Multiplexed bidirectional Address/Data bus AD7 to AD0
34,33,32,30, 29,28,27,26	A[15:8]	OUTPUT	Extended Address A15 to A8
38	CS#	OUTPUT	Active low chip select device during Read or Write.
39	ALE	OUTPUT	Positive pulse to latch the address
40	RD#	OUTPUT	Active low read output.
41	WR#	OUTPUT	Active low write output. (Data is setup before WR# goes low, and is held after WR# goes high)
43	IORDY	INPUT	Extends the time taken to perform a Read or Write operation if driven low. Pull up to VCORE if not being used.
44	CLKOUT	OUTPUT	Master clock. Outputs the clock signal being used by the configured interface.
45	I/O0	I/O	MPSSE mode instructions to set / clear or read the high byte of data can be used with this pin. Please refer to Application Note **AN_108** for operation of these instructions.
46	I/O1	I/O	MPSSE mode instructions to set / clear or read the high byte of data can be used with this pin. In addition this pin has instructions which will make the controller wait until it is high, or wait until it is low. This can be used to connect to an IRQ pin of a peripheral chip. The FT2232H will wait for the interrupt, and then read the device, and pass the answer back to the host PC. I/O1 must be held in input mode if this option is used. Please refer to Application Note **AN_108** for operation of these instructions.

Table 3.11 Channel A and Channel B Host Bus Emulation Interface Configured Pin Descriptions

For a functional description of this mode, please refer to section 4.7 MCU Host Bus Emulation Mode

4 Function Description

The FT2232H USB 2.0 High Speed (480Mb/s) to UART/FIFO is one of FTDI's 5th generation of Ics. It has the capability of being configured in a variety of industry standard serial or parallel interfaces.

The FT2232H has two independent configurable interfaces. Each interface can be configured as UART, FIFO, JTAG, SPI, I2C or bit-bang mode with independent baud rate generators. In addition to these, the FT2232H supports a host bus emulation mode, a CPU-Style FIFO mode and a fast opto-isolated serial interface mode.

4.1 Key Features

USB High Speed to Dual Interface. The FT2232H is a USB 2.0 High Speed (480Mbits/s) to dual independent flexible and configurable parallel/serial interfaces.

Functional Integration. The FT2232H integrates a USB protocol engine which controls the physical Universal Transceiver Macrocell Interface (UTMI) and handles all aspects of the USB 2.0 High Speed interface. The FT222H includes an integrated +1.8V Low Drop-Out (LDO) regulator and 12MHz to 480MHz PLL. It also includes 4kbytes Tx and Rx data buffers per interface. The FT2232H effectively integrates the entire USB protocol on a chip with no firmware required.

MPSSE.Multi-Purpose Synchronous Serial Engines (MPSSE), capable of speeds up to 30 Mbits/s, provides flexible synchronous interface configurations.

Data Transfer rate. The FT2232H supports a data transfer rate up to 12 Mbaud when configured as an RS232/RS422/RS485 UART interface or greater than 25 Mbytes/second over a synchronous parallel FIFO interface. Please note the FT2232H does not support the baud rates of 7 Mbaud 9 Mbaud, 10 Mbaud and 11 Mbaud.

Latency Timer. This is really a feature of the driver and is used to as a timeout to flush short packets of data back to the PC. The default is 16ms, but it can be altered between 0ms and 256ms. At 0ms latency you get a packet transfer on every high speed microframe.

4.2 Functional Block Descriptions

Dual Multi-Purpose UART/FIFO Controllers. The FT2232H has two independent UART/FIFO Controllers. These control the UART data, 245 fifo data, opto isolation (Fast Serial) or control the Bit-Bang mode if selected by SETUP command. Each Multi-Purpose UART/FIFO Controller also contain an MPSSE (Multi Protocol Synchronous Serial Engine) which can be used independently of each other. Using this MPSSE, the Multi-Purpose UART/FIFO Controller can be configured, under software command, to have 1 MPSSE + 1 UART / 245 FIFO (each UART / 245 can be set to Bit Bang mode to gain extra I/O if required) or 2 MPSSE.

USB Protocol Engine and FIFO control. The USB Protocol Engine controls and manages the interface between the UTMI PHY and the FIFOs of the chip. It also handles power management and the USB protocol specification.

Dual Port FIFO TX Buffer (4Kbytes per interface). Data from the Host PC is stored in these buffers to be used by the Multi-purpose UART/FIFO controllers. This is controlled by the USB Protocol Engine and FIFO control block.

Dual Port FIFO RX Buffer (4Kbytes per interface). Data from the Multi-purpose UART/FIFO controllers is stored in these blocks to be sent back to the the Host PC when requested. This is controlled by the USB Protocol Engine and FIFO control block.

RESET Generator – The integrated Reset Generator Cell provides a reliable power-on reset to the device internal circuitry at power up. The RESET# input pin allows an external device to reset the FT2232H. RESET# should be tied to VCCIO (+3.3v) if not being used.

Independent Baud Rate Generators – The Baud Rate Generators provides a x16 or a x10 clock input to the UART's from a 120MHz reference clock and consists of a 14 bit pre-scaler and 4 register bits which provide fine tuning of the baud rate (used to divide by a number plus a fraction). This determines the Baud Rate of the UART which is programmable from 183 baud to 12 million baud. The FT2232H does not support the baud rates of 7 Mbaud 9 Mbaud, 10 Mbaud and 11 Mbaud.

See FTDI application note AN232B-05 on the FTDI website (www.ftdichip.com) for more details.

+1.8V LDO Regulator. The +1.8V LDO regulator generates the +1.8 volts for the core and the USB transceiver cell. Its input (VREGIN) must be connected to a +3.3V external power source. It is also recommended to add an external filtering capacitor to the VREGIN. There is no direct connection from the +1.8V output (VREGOUT) and the internal functions of the FT2232H. The PCB must be routed to connect VREGOUT to the pins that require the +1.8V including VREGIN.

UTMI PHY. The Universal Transceiver Macrocell Interface (UTMI) physical interface cell. This block handles the Full speed / High Speed SERDES (serialise – deserialise) function for the USB TX/RX data. It also provides the clocks for the rest of the chip. A 12 MHz crystal should be connected to the OSCI and OSCO pins. A 12K Ohm resistor should be connected between REF and GND on the PCB.

The UTMI PHY functions include:

- Supports 480 Mbit/s "High Speed" (HS)/ 12 Mbit/s "Full Speed" (FS), FS Only and "Low Speed" (LS)
- SYNC/EOP generation and checking
- Data and clock recovery from serial stream on the USB.
- Bit-stuffing/unstuffing; bit stuff error detection.
- Manages USB Resume, Wake Up and Suspend functions.
- Single parallel data clock output with on-chip PLL to generate higher speed serial data clocks.

EEPROM Interface. When used without an external EEPROM the FT2232H defaults to a USB to dual asynchronous serial port device. Adding an external 93C46 (93C56 or 93C66) EEPROM allows each of the chip's channels to be independently configured as a serial UART (RS232 mode), parallel FIFO (245) mode or fast serial (opto isolation). The external EEPROM can also be used to customise the USB VID, PID, Serial Number, Product Description Strings and Power Descriptor value of the FT2232H for OEM applications. Other parameters controlled by the EEPROM include Remote Wake Up, Soft Pull Down on Power-Off and I/O pin drive strength.

The EEPROM should be a 16 bit wide configuration such as a Microchip 93LC46B or equivalent capable of a 1Mbit/s clock rate at VCC = +3.00V to 3.6V. The EEPROM is programmable in-circuit over USB using a utility program called MPROG available from FTDI's web site (**www.ftdichip.com**). This allows a blank part to be soldered onto the PCB and programmed as part of the manufacturing and test process.

If no EEPROM is connected (or the EEPROM is blank), the FT2232H will default to dual serial ports. The device uses its built-in default VID (0403) , PID (6010) Product Description and Power Descriptor Value. In this case, the device will not have a serial number as part of the USB descriptor.

4.3 Dual Port FT232 UART Interface Mode Description

The FT2232H can be configured in similar UART modes as the FTDI FT232 devices. The following examples illustrate how to configure the FT2232H with an RS232, RS422 or RS485 interface. The FT2232 can be configured as a mixture of these interfaces.

4.3.1 Dual Port RS232 Configuration

Figure 4.1 illustrates how the FT2232H can be configured with an RS232 UART interface. This can be repeated for channel B to provide a dual RS232, but has been omitted for clarity.

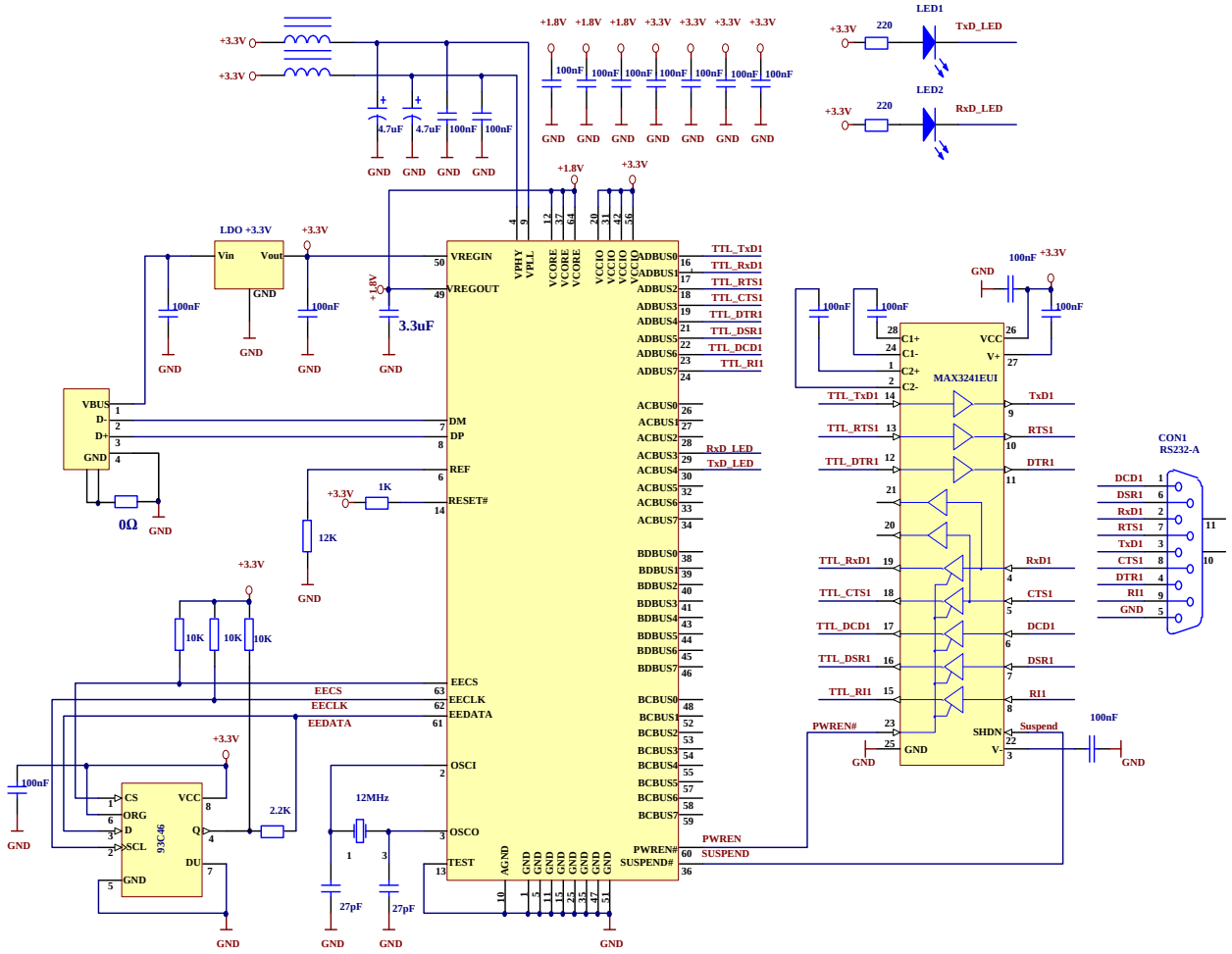


Figure 4.1 RS232 Configuration

4.3.2 Dual Port RS422 Configuration

Figure 4.2 illustrates how the FT2232H can be configured as a dual RS422 interface.

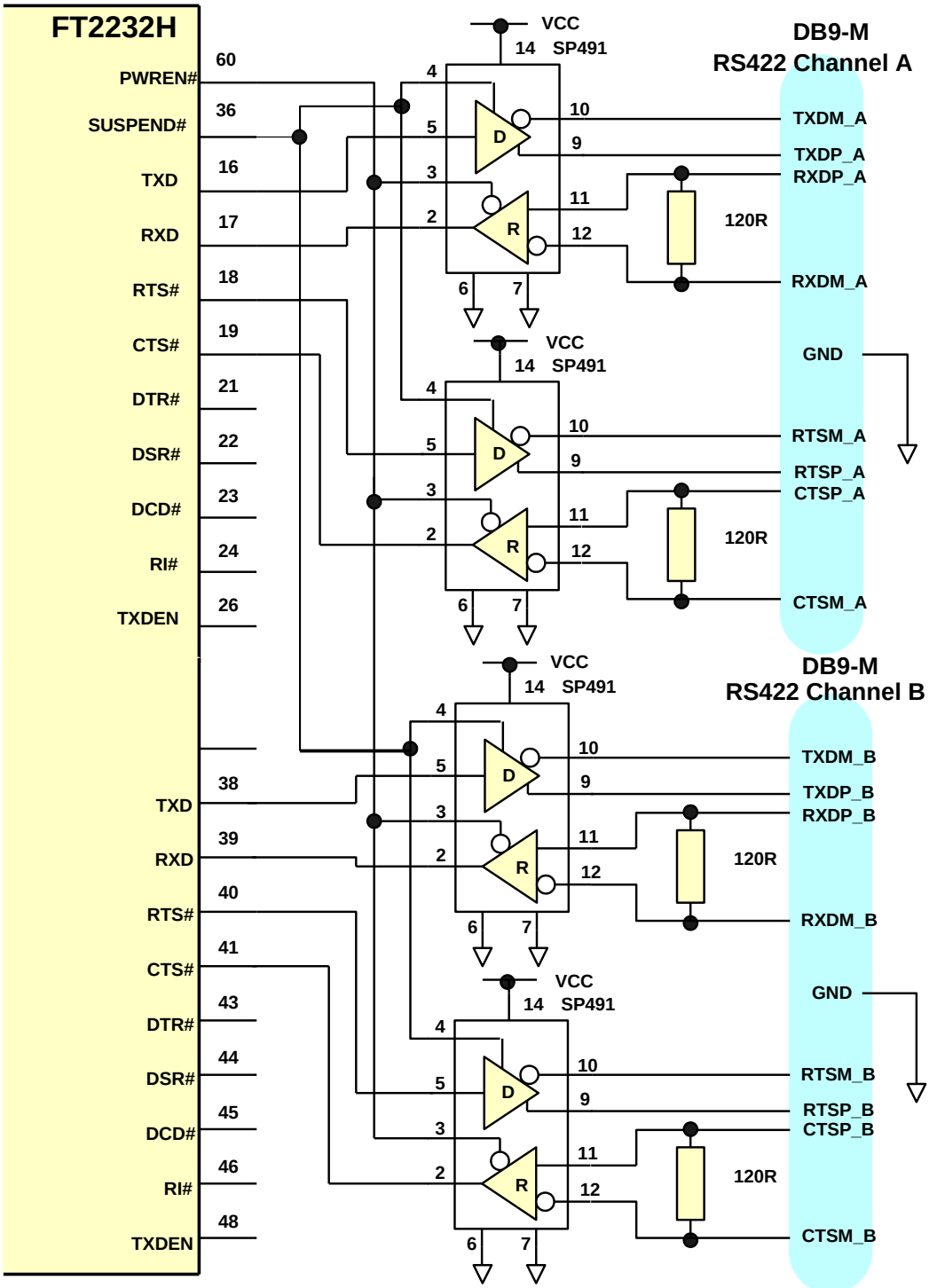


Figure 4.2 Dual RS422 Configuration

In this case both channel A and channel B are configured as UART operating at TTL levels. The Sipex SP491 is used as a level converter to convert the TTL level signals from the FT2232H to RS422 levels. The PWREN# signal is used to power down the level shifters such that they operate in a low quiescent current when the USB interface is in suspend mode.

4.3.3 Dual Port RS485 Configuration

Figure 4.3 illustrates how the FT2232H can be configured as a dual RS485 interface.

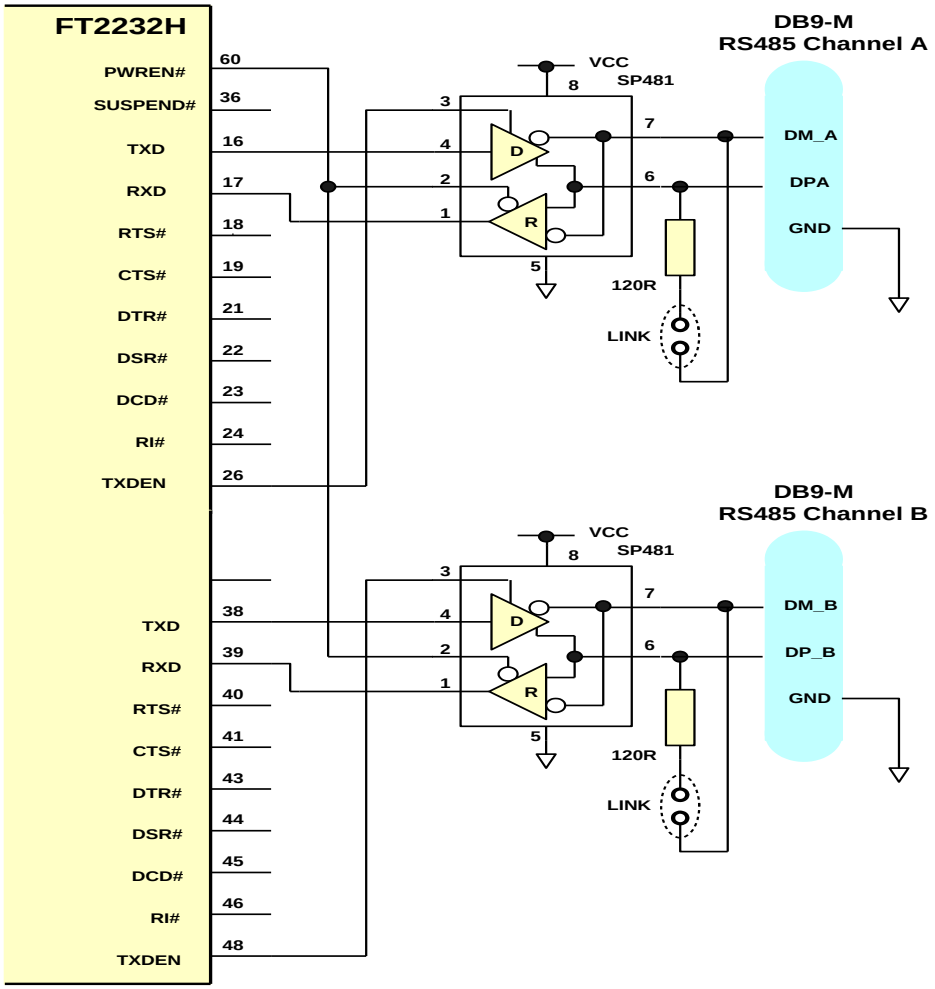


Figure 4.3 Dual RS485 Configuration

In this case both channel A and channel B are configured as RS485 operating at TTL levels. This example uses two Sipex SP491 devices but there are similar parts available from Maxim and Analog Devices amongst others. The SP491 is a RS485 device in a compact 8 pin SOP package. It has separate enables on both the transmitter and receiver. With RS485, the transmitter is only enabled when a character is being transmitted from the UART. The TXDEN pins on the FT2232H are provided for exactly that purpose, and so the transmitter enables are wired to the TXDEN's. The receiver enable is active low, so it is wired to the PWREN# pin to disable the receiver when in USB suspend mode.

RS485 is a multi-drop network – i.e. many devices can communicate with each other over a single two wire cable connection. The RS485 cable requires to be terminated at each end of the cable. Links are provided to allow the cable to be terminated if the device is physically positioned at either end of the cable.

In this example the data transmitted by the FT2232H is also received by the device that is transmitting. This is a common feature of RS485 and requires the application software to remove the transmitted data from the received data stream. With the FT2232H it is possible to do this entirely in hardware – simply modify the schematic so that RXD of the FT2232H is the logical OR of the SP481 receiver output with TXDEN using an HC32 or similar logic gate.

4.4 FT245 Synchronous FIFO Interface Mode Description

When channel A is configured in an FT245 Synchronous FIFO interface mode the IO timing of the signals used are shown in Figure 4.4, which shows details for read and write accesses. The timings are shown in Table 4.1. Note that only a read or a write cycle can be performed at any one time. Data is read or written on the rising edge of the CLKOUT clock.

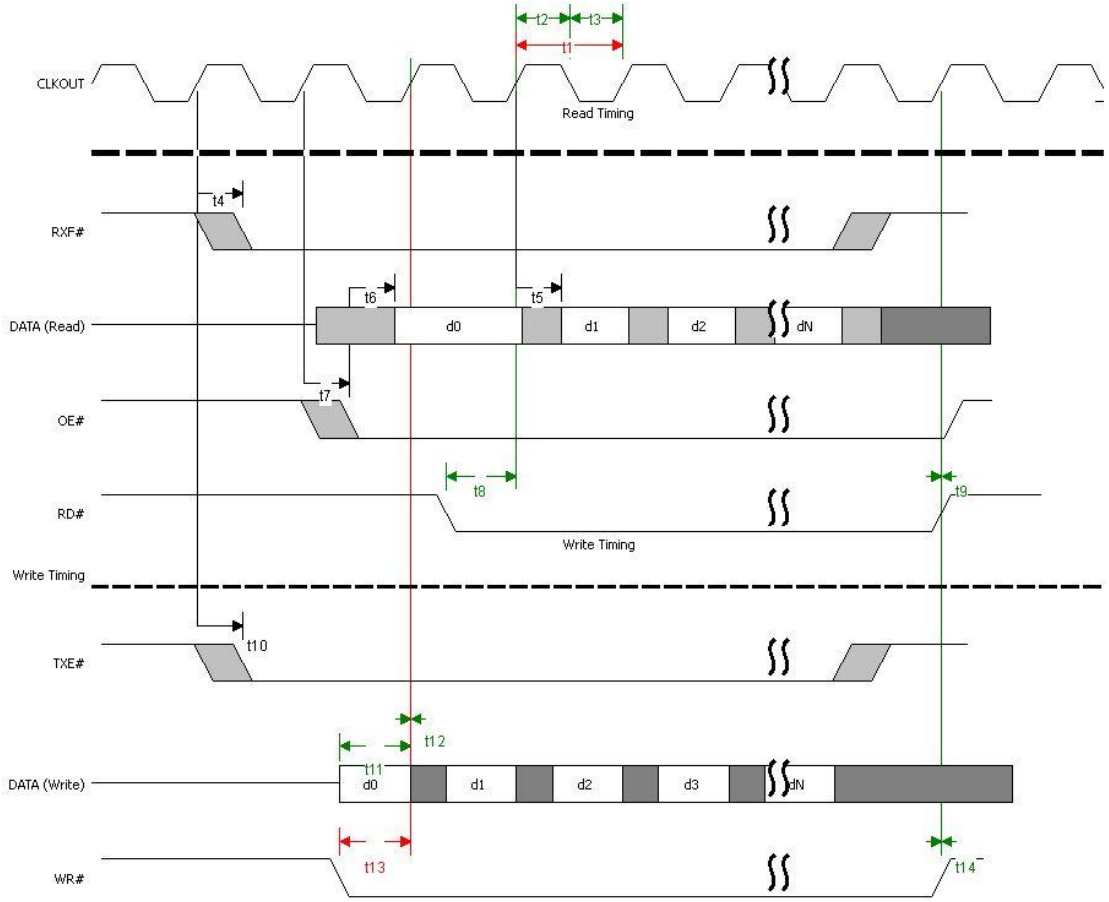


Figure 4.4 FT245 Synchronous FIFO Interface Signal Waveforms

NAME	MIN	NOM	MAX	Units	COMMENT
t1		16.67		ns	CLKOUT period
t2	7.5	8.33		ns	CLKOUT high period
t3	7.5	8.33		ns	CLKOUT low period
t4	1		7.15	ns	CLKOUT to RXF#
t5	1		7.15	ns	CLKOUT to read DATA valid
t6	1		7.15	ns	OE# to read DATA valid
t7	1		7.15	ns	CLKOUT to OE#
t8	11			ns	RD# setup time to CLKOUT (RD# low afterOE# low)
t9	0			ns	RD# hold time
t10	1		7.15	ns	CLKOUT TO TXE#
t11	11			ns	Write DATA setup time
t12	0			ns	Write DATA hold time
t13	11			ns	WR# setup time to CLKOUT (WR# low after TXE# low)
t14	0			ns	WR# hold time

Table 4.1 FT245 Synchronous FIFO Interface Signal Timings

This single channel mode uses a synchronous interface to get high data transfer speeds. The chip drives a 60 MHz CLKOUT clock for the external system to use.

Note that Asynchronous FIFO mode must be selected on both channels before selecting the Synchronous FIFO mode in software.

4.4.1 FT245 Synchronous FIFO Read Operation

A read operation is started when the chip drives RXF# low. The external system can then drive OE# low to turn around the data bus drivers before acknowledging the data with the RD# signal going low. The first data byte is on the bus after OE# is low. The external system can burst the data out of the chip by keeping RD# low or it can insert wait states in the RD# signal. If there is more data to be read it will change on the clock following RD# sampled low. Once all the data has been consumed, the chip will drive RXF# high. Any data that appears on the data bus, after RXF# is high, is invalid and should be ignored.

4.4.2 FT245 Synchronous FIFO Write Operation

A write operation can be started when TXE# is low. WR# is brought low when the data is valid. A burst operation can be done on every clock providing TXE# is still low. The external system must monitor TXE# and its own WR# to check that data has been accepted. Both TXE# and WR# must be low for data to be accepted.

4.5 FT245 Asynchronous FIFO Interface Mode Description

The FT2232H can be configured as a dual channel asynchronous FIFO interface. This mode is similar to the synchronous FIFO interface with the exception that the data is written to or read from the FIFO on the falling edge of the WR# or RD# signals.

This mode does not provide a CLKOUT signal and it does not expect an OE# input signal. The following diagrams illustrate the asynchronous FIFO mode timing.

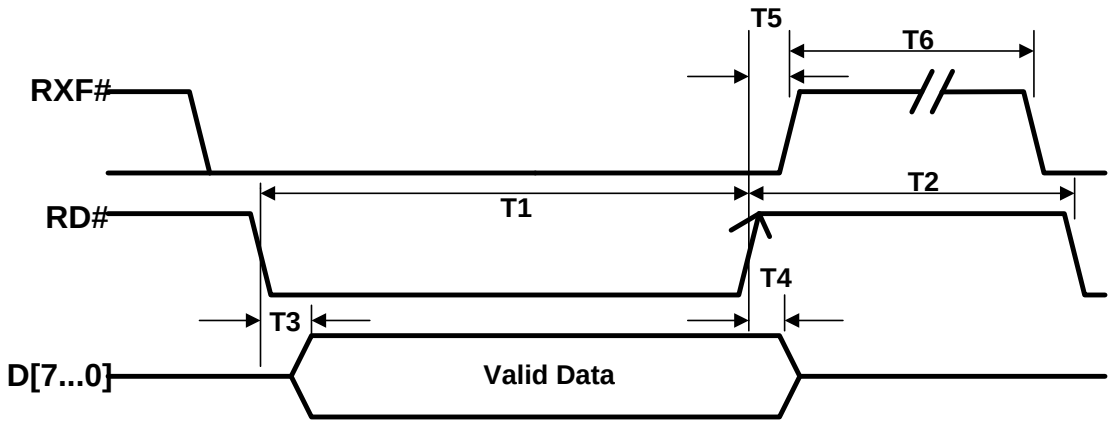


Figure 4.5 FT245 asynchronous FIFO Interface READ Signal Waveforms

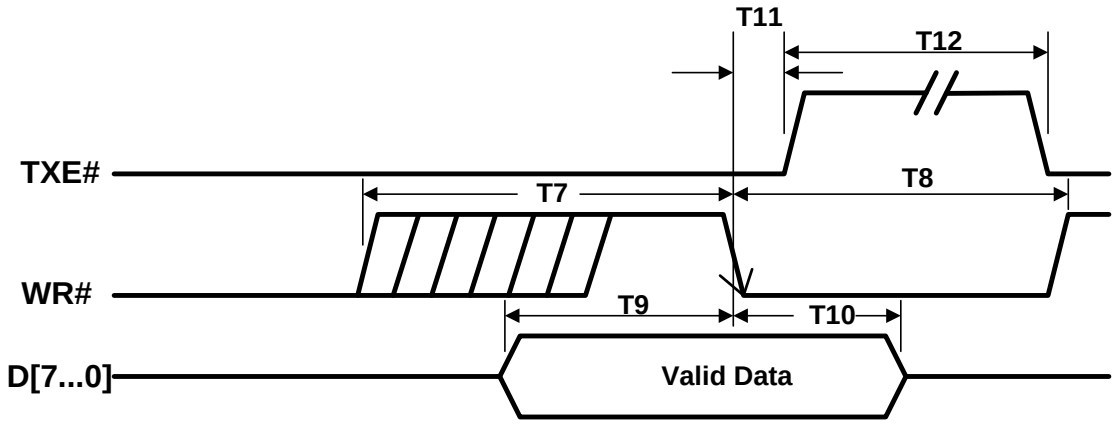


Figure 4.6 FT245 asynchronous FIFO Interface WRITE Signal Waveforms

Time	Description	Min	Max	Units
T1	RD# input pulse width	**50**		ns
T2	RD# to RD pre-charge	T5 +T6		ns
T3	RD# input active to data output valid	20	50	ns
T4	Valid data hold time after RD# input rising edge	0		ns
T5	RD# inactive to RXF# output inactive	0	25	ns
T6	RXF# output inactive after RD# cycle	33	67	ns
T7	WR# active pulse width	10		ns
T8	WR# to WR# pre-charge time	50		ns

T9	Data setup time before WR# input falling edge	20		ns
T10	Data hold time from WR# input falling edge	10		ns
T11	WR# inactive to TXE# output active	10	25	ns
T12	TXE# input inactive after WR# cycle	49	84	ns

Table 4.2 Asynchronous FIFO Timings (based on standard drive level outputs)

4.6 MPSSE Interface Mode Description.

MPSSE Mode is designed to allow the FT2232H to interface efficiently with synchronous serial protocols such as JTAG, I2C and SPI Bus. It can also be used to program SRAM based FPGA's over USB. The MPSSE interface is designed to be flexible so that it can be configured to allow any synchronous serial protocol (industry standard or proprietary) to be implemented using the FT2232H. MPSSE is available on channel A and channel B.

MPSSE is fully configurable, and is programmed by sending commands down the data stream. These can be sent individually or more efficiently in packets. MPSSE is capable of a maximum sustained data rate of 30 Mbits/s.

When a channel is configured in MPSSE mode, the IO timing and signals used are shown in Figure 4.7 and Table 4.3 These show timings for CLKOUT=30MHz. CLKOUT can be divided internally to be provide a slower clock.

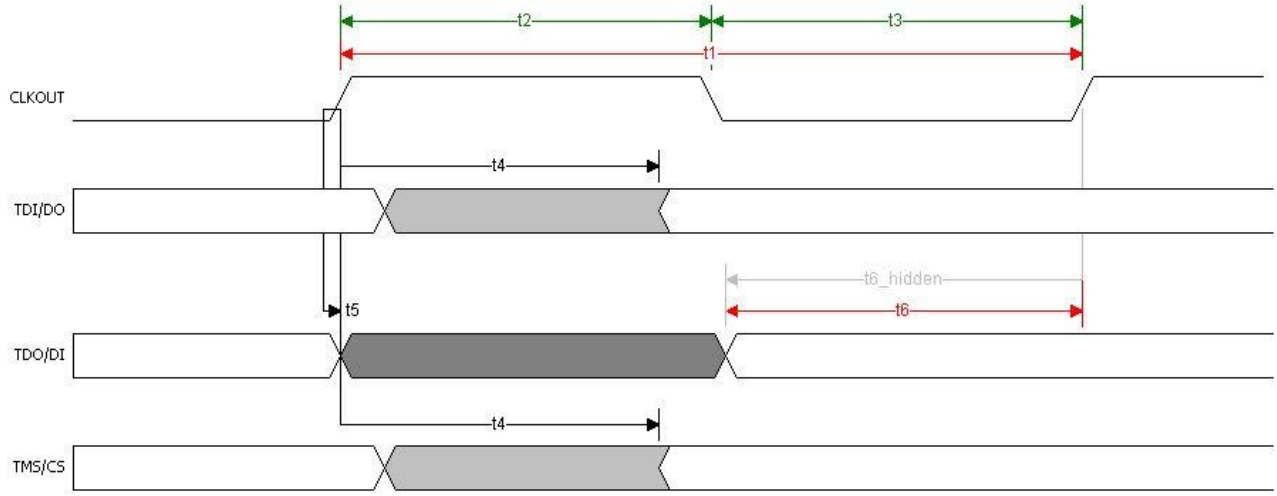


Figure 4.7 MPSSE Signal Waveforms

NAME	MIN	NOM	MAX	Units	COMMENT
t1		33.33		ns	CLKOUT period
t2	15	16.67		ns	CLKOUT high period
t3	15	16.67		ns	CLKOUT low period
t4	1		7.15	ns	CLKOUT to TDI/DO delay
t5	0			ns	TDO/DI hold time
t6	11				TDO/DI setup time

Table 4.3 MPSSE Signal Timings

MPSSE mode is enabled using Set Bit Bang Mode driver command. A hex value of 2 will enable it, and a hex value of 0 will reset the device. See application note **AN2232L-02, "Bit Mode Functions for the FT2232D"** for more details and examples.

The MPSSE command set is fully described in application note **AN_108 – "Command Processor For MPSSE and MCU Host Bus Emulation Modes"**.

The following additional application notes are available for configuring the MPSSE :

- **AN_109 – "Programming Guide for High Speed FTCI2C DLL"**
- **AN_110 – "Programming Guide for High Speed FTCJTAG DLL"**
- **AN_111 – "Programming Guide for High Speed FTCSPI DLL"**

4.6.1 MPSSE Adaptive Clocking

Adaptive clocking is a new MPSSE feature added to the FT2232H MPSSE engine.

The mode is effectively handshaking the CLK signal with a return clock RTCK. This is a technique used by ARM processors.

The FT2232H will assert the CLK line and wait for the RTCK to be returned from the target device to GPIOL3 line before changing the TDO (data out line).

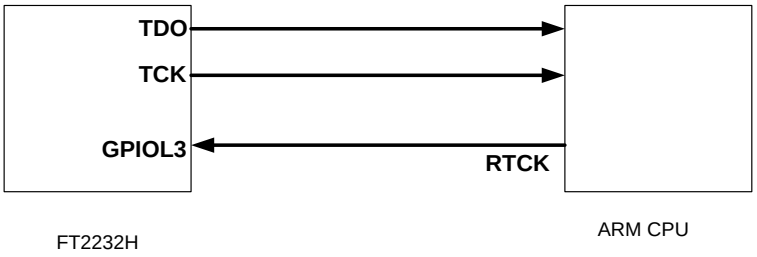


Figure 4.8 Adaptive Clocking Interconnect

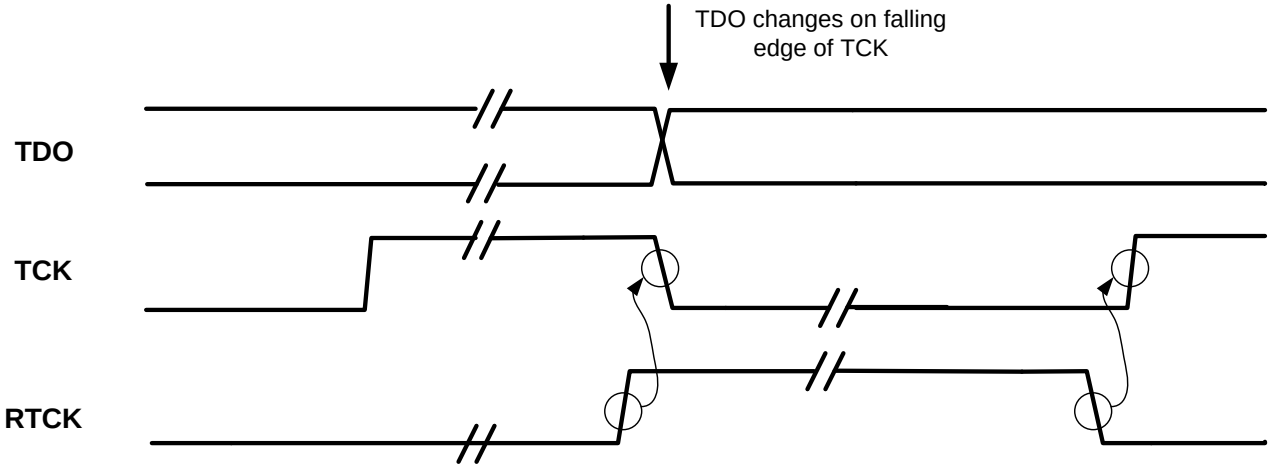


Figure 4.9: Adaptive Clocking waveform.

Adaptive clocking is not enabled by default.

See: AN_108 Command Processor for MPSSE and MCU Host Bus Emulation Modes.

4.7 MCU Host Bus Emulation Mode

MCU host bus emulation mode uses both of the FT2232H's A and B channel interfaces to make the chip emulate a standard 8048/8051 MCU host bus. This allows peripheral devices for these MCU families to be directly connected to USB via the FT2232H.

The lower 8 bits (AD7 to AD0) is a multiplexed Address / Data bus. A15 to A18 provide upper (extended) addresses. There are 4 basic operations:-

1) Read (does not change A15 to A8)

2) Read Extended (changes A15 to A8)

3) Write (does not change A15 to A8)

4) Write Extended (changes A15 to A8)

MCU Host Bus Emulation mode is enabled using Set Bit Bang Mode driver command. A hex value of 8 will enable it, and a hex value of 0 will reset the device. The FT2232H operates in the same way as the FT2232D. See application note **AN2232-02, "Bit Mode Functions for the FT2232D"** for more details and examples.

The MCU Host Bus Emulation Mode command set is fully described in application note **AN_108 – "Command Processor For MPSSE and MCU Host Bus Emulation Modes"**.

When MCU Host Bus Emulation mode is enabled the IO signal lines on both channels work together and the pins are configured as described in **Table 3.11**. The following sections give some details of the read and write cycle waveforms and timings. The CLKOUT output clock can operate up to 60MHz.

In Host Bus Emulation mode the clock divisor has no effect. The clock divisor is used for serial data and is a different part of the MPSSE block. In host bus emulation the 60MHz clock is always output and doesn't change with any commands.

4.7.1 MCU Host Bus Emulation Mode Signal Timing – Write Cycle

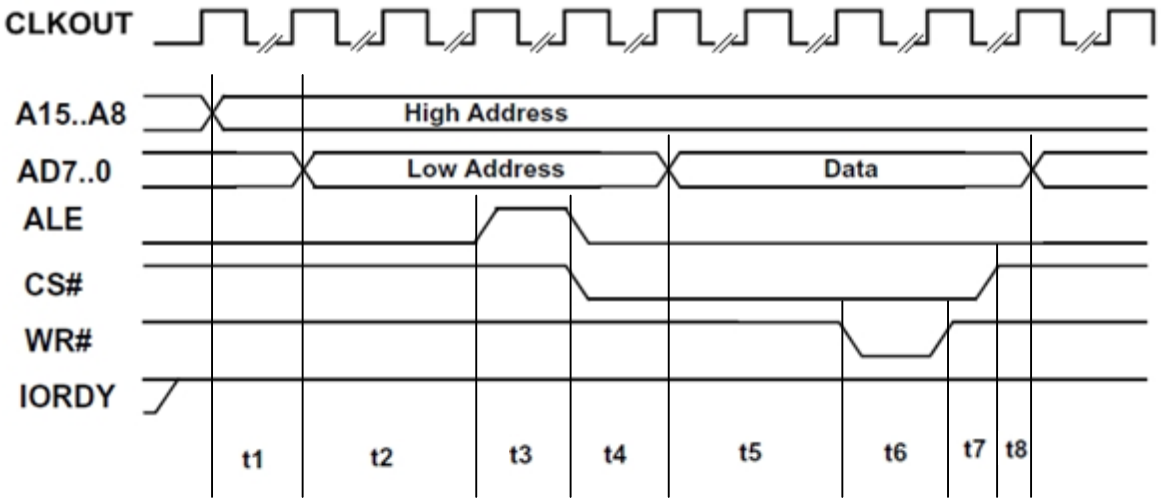


Figure 4.10 MCU Host Bus Emulation Mode Signal Waveforms – write cycle

	Number of clock cycles For Write				
Div By 5	On		Off		
IORDY	Low	High	Low	High	
t1	6	6	2	2	A15-8 to AD7-0
t2	3	3	1	1	AD7-0 to ALE
t3	10	5	2	1	ALE width
t4	2	2	2	2	ALE to Address not Valid
t5	13	3	1	1	AD7-0 Data Valid to WRn
t6	10	5	6	1	WRn width
t7	1	1	1	1	WRn inactive to CSn inactive
t8	1	1	1	1	CSn inactive to AD7-0 not valid

Table 4.4 MCU Host Bus Emulation Mode Signal Timings – write cycle

When Div By 5 is on the device will return 2 bytes when doing a read. When it is off the device will return 1 byte when doing a read. The clock period is 16.67 nS so most devices would need the Div By 5 to be set on. IORDY can be held low permanently to extend all cycles.

4.7.2 MCU Host Bus Emulation Mode Signal Timing – Read Cycle

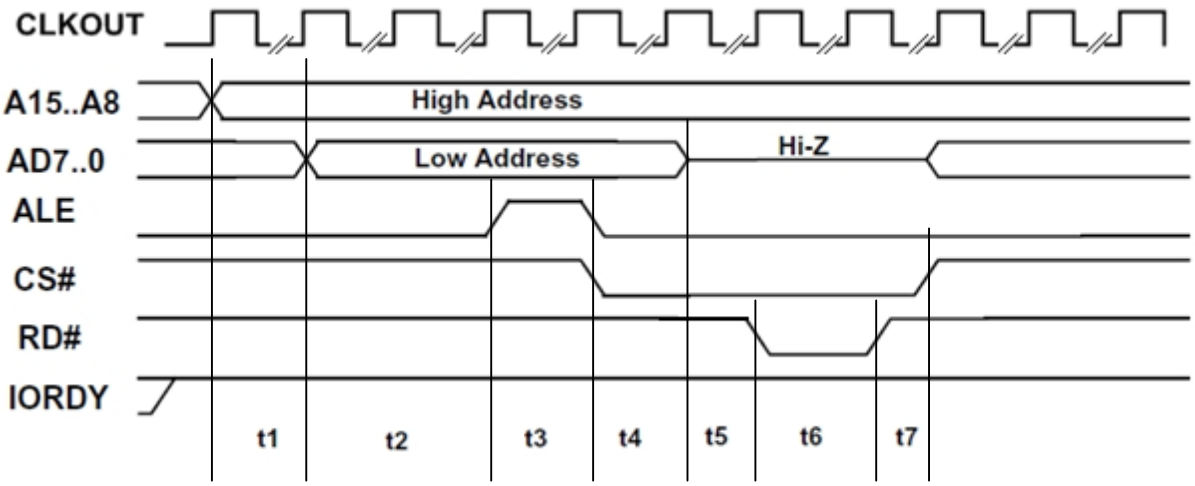


Figure 4.11 MCU Host Bus Emulation Mode Signal Waveforms – read cycle

	Number of clock cycles For Read				
Div By 5	On		Off		
IORDY	Low	High	Low	High	
t1	6	6	2	2	A15-8 to AD7-0
t2	3	3	1	1	AD7-0 to ALE
t3	10	5	2	1	ALE width
t4	2	5	2	1	ALE to Address not Valid
t5	13	0	1	0	Address not Valid to RDn active
t6	10	10	6	2	RDn active
t7	1	1	1	1	RDn inactive to CSn inactive

Table 4.5 MCU Host Bus Emulation Mode Signal Timings– read cycle

When Div By 5 is on the device will return 2 bytes when doing a read. When it is off the device will return 1 byte when doing a read. The clock period is 16.67 nS so most devices would need the Div By 5 to be set on. IORDY can be held low permanently to extend all cycles.

An example of the MCU Host Emulation Interface enabling a USB interface to CAN Bus using a CANBus Controller is shown in Figure 4.12

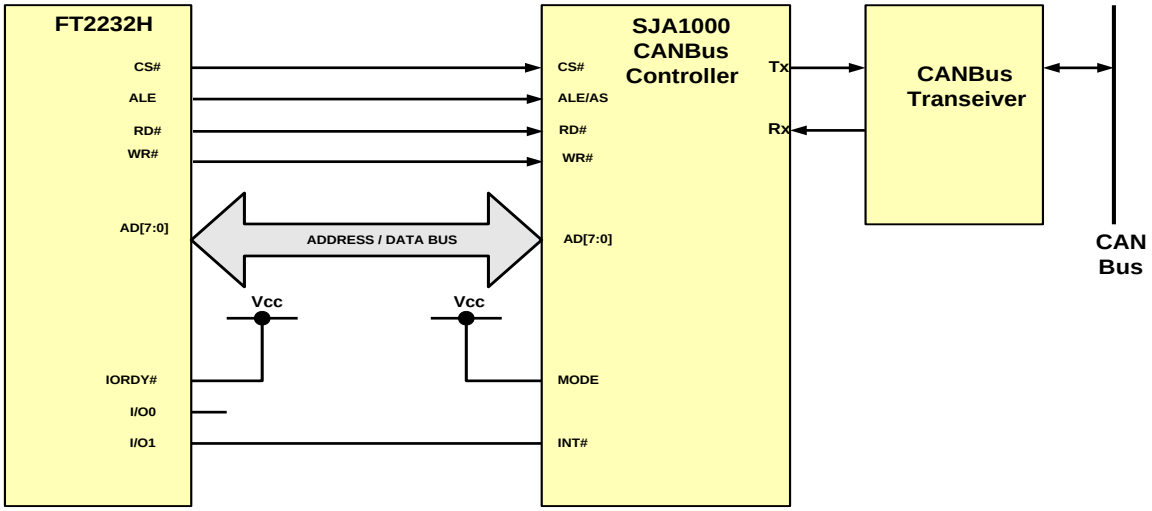


Figure 4.12 MCU Host Emulation Example using a CANBus Controller

4.8 Fast Opto-Isolated Serial Interface Mode Description

Fast Opto-Isolated Serial Interface Mode provides a method of communicating with an external device over USB using 4 wires that can have opto-isolators in their path, thus providing galvanic isolation between systems. If either channel A or channel B is enabled in Fast Opto-Isolated Serial mode then the pins on channel B are switched to the fast serial interface configuration. The I/O interface for fast serial mode is always on channel B, even if both channels are being used in this mode. An address bit is used to determine the source or destination channel of the data. It therefore makes sense to always use at least channel B or both for fast serial mode, but not A own its own.

Fast serial mode is enabled by setting the appropriate bits in the external EEPROM. The fast serial mode can be held in reset by setting a bit value of 10 using the Set Bit Bang Mode command. While this bit is set the device is held reset – data can be sent to the device, but it will not be sent out by the device until the device is enabled again. This is done by sending a bit value of 0 using the set bit mode command. See application note **AN2232L-02, "Bit Mode Functions for the FT2232D"** for more details and examples.

When either Channel B or both Channel A and B are configured in Fast Opto-Isolated Serial Interface mode the IO timing of the signals used are shown in Figure 4.13 and the timings are shown in Table 4.6

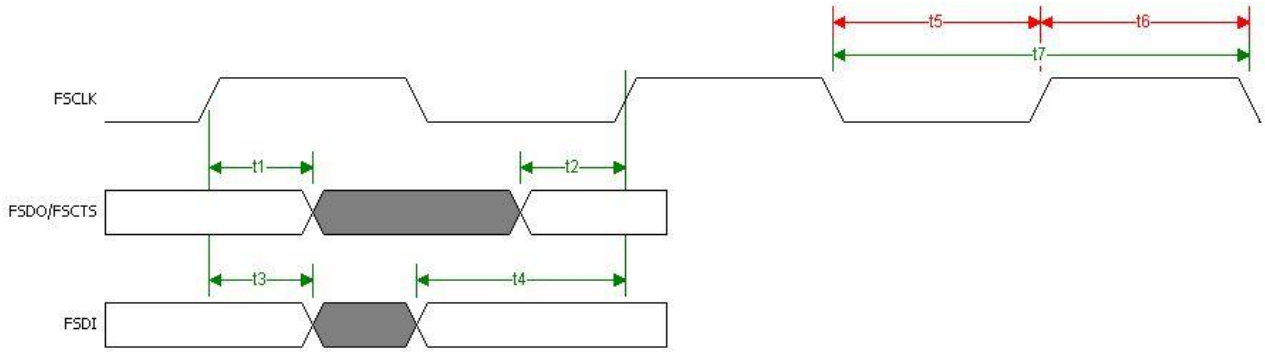


Figure 4.13 Fast Opto-Isolated Serial Interface Signal Waveforms

NAME	MIN	NOM	MAX	Units	COMMENT
t1	5			ns	FSDO/FSCTS hold time
t2	5			ns	FSDO/FSCTS setup time
t3	5			ns	FSDI hold time
t4	10			ns	FSDI Setup Time
t5	10			ns	FSCLK low
t6	10			ns	FSCLK high
t7	20			ns	FSCLK Period

Table 4.6 Fast Opto-Isolated Serial Interface Signal Timings

4.8.1 Outgoing Fast Serial Data

To send fast serial data out of the FT2232H, the external device must drive the FSCLK clock. If the FT2232H has data ready to send, it will drive FSDO output low to indicate the start bit. It will not do this if it is currently receiving data from the external device. This is illustrated in Figure 4.14.

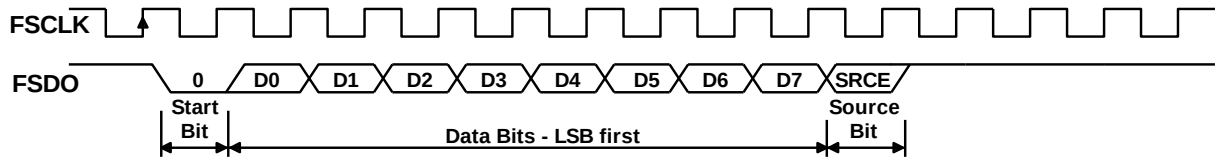


Figure 4.14 Fast Opto-Isolated Serial Interface Output Data

Notes :-

1. The first bit output (Start bit) is always 0.
2. FSDO is always sent LSB first.
3. The last serial bit output is the source bit (SRCE). It indicates which channel the data has come from. A '0' means that it has come from Channel A, a '1' means that it has come from Channel B.
4. If the target device is unable to accept the data when it detects the START bit, it should stop the FSCLK until it can accept the data.

4.8.2 Incoming Fast Serial Data

An external device is allowed to send data into the FT2232H if FSCTS is high. On receipt of a zero START bit on FSDI, the FT2232H will drop FSCTS on the next positive clock edge. The data from bits 0 to 7 are then clocked in (LSB first). The last bit (DEST) determines where the data will be written to. The data can be sent to either channel A or to channel B. If DEST= '0', the data is sent to channel A, (assuming channel A is enabled for fast serial mode, otherwise the data is sent to channel B). If DEST= '1' the data is sent to channel B, (assuming channel B is enabled for fast serial mode, otherwise the data will go to channel A. (Either channel A, channel B or both channels must be enabled as fast serial mode or the function is disabled). This is illustrated in Figure 4.15.

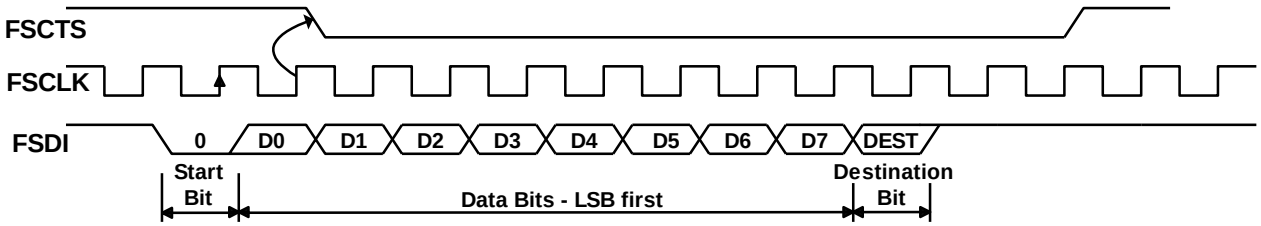


Figure 4.15 Fast Opto-Isolated Serial Interface Input Data

Notes :-

1. The first bit input (Start bit) is always 0.
2. FSDI is always received LSB first.
3. The last received serial bit is the destination bit (DEST).It indicates which channel the data should go to. A '0' means that it should go to channel A, a '1' means that it should go to channel B.
4. The target device should ensure that CTS is high before it sends data. CTS goes low after data bit 0 (D0) and stays low until the chip can accept more data.

4.8.3 Fast Opto-Isolated Serial Data Interface Example

The following example,Figure 4.16 , shows two Agilent HCPL-2430 (see the semiconductor section at **www.agilent.com**) high speed opto-couplers used to optically isolate an external device which interfaced to USB using the FT2232H. In this example VCC5V is the USB VBUS supply and VCCE is the supply to the external device.

Care must be taken with the voltage used to power the photo-LED's. It must be the same voltage as that the FT2232H I/Os are driving to, or the LED's may be permanently on. Limiting resistors should be fitted in the lines that drive the diodes. The outputs of the opto-couplers are open-collector and require a pull-up resistor.

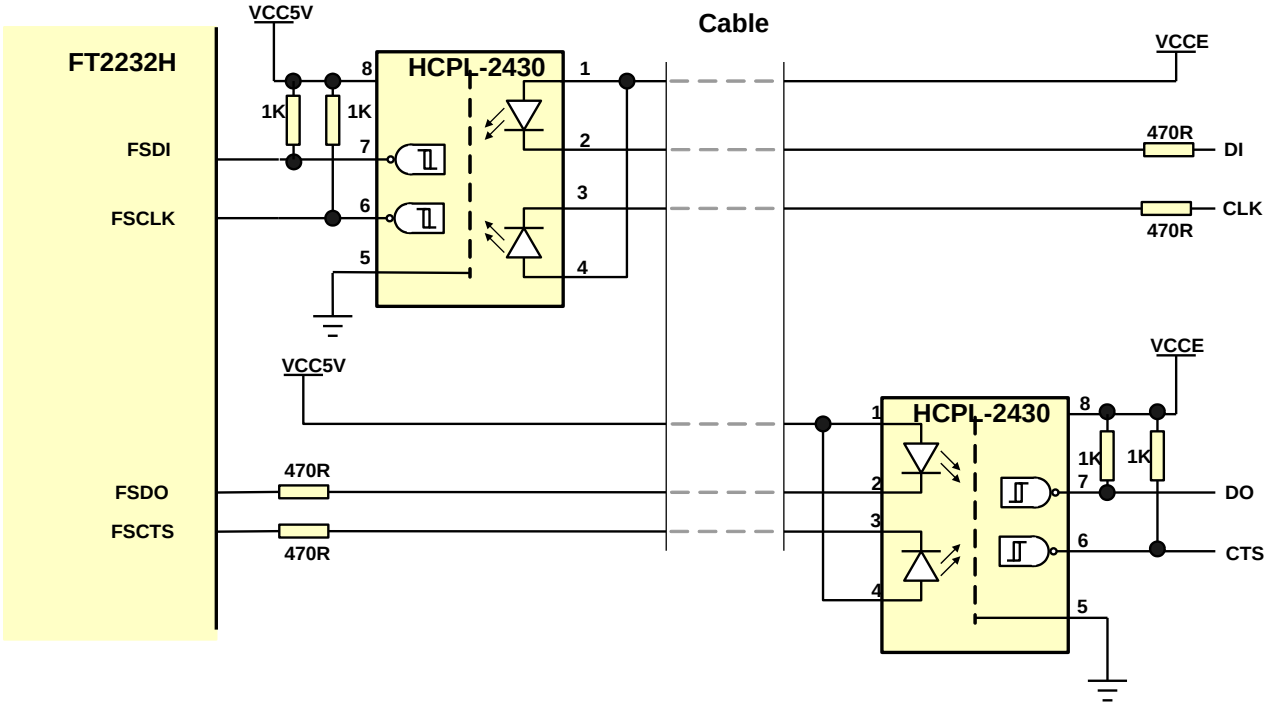


Figure 4.16 Fast Opto-Isolated Serial Interface Example

4.9 CPU-style FIFO Interface Mode Description

CPU-style FIFO interface mode is designed to allow a CPU to interface to USB via the FT2232H. This mode is enabled in the external EEPROM. The interface is achieved using a chip select bit (CS#) and address bit (A0). When either Channel A or Channel B are in CPU-style Interface mode the IO signal lines are configured as given in **Table 3.10**.

This mode uses a combination of CS# and A0 to determine the operation to be carried out. The following truth-table, **Table 4.7**, gives the decode values for particular operations.

CS#	A0	RD#	WR#
1	X	X	X
0	0	Read Data Pipe	Write Data Pipe
0	1	Read Status	Send Immediate

Table 4.7 CPU-Style FIFO Interface Operation Select

The Status read is shown in **Table 4.8**

Data Bit	Data	Status
bit 0	1	Data available (=RXF)
bit 1	1	Space available (=TXE)
bit 2	1	Suspend
bit 3	1	Configured
bit 4	X	X
bit 5	X	X
bit 6	X	X
bit 7	X	X

Table 4.8 CPU-Style FIFO Interface Operation Read Status Description

Note that bits 7 to 4 can be arbitrary values and that X= not used.

The timing of reading and writing in this mode is shown in **Figure 4.17** and **Table 4.9**.

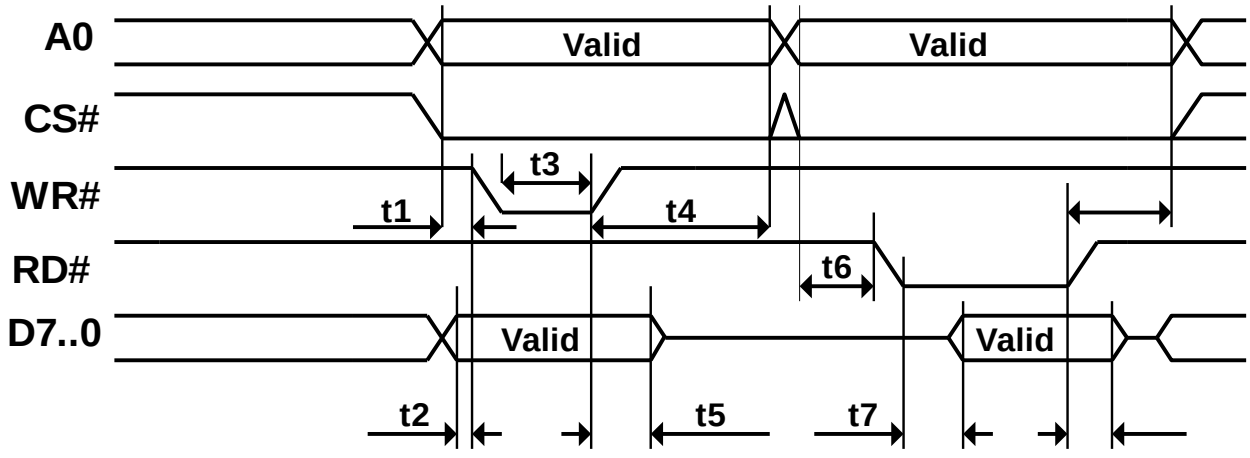


Figure 4.17 CPU-Style FIFO Interface Operation Signal Waveforms.

NAME	MIN	NOM	MAX	Units	COMMENT
t1	15			ns	A0 / CS Setup to WR#
t2	15			ns	Data setup to WR#
t3	20			ns	WR# Pulse width
t4	5			ns	A0/CS Hold from WR#
t5	5			ns	Data hold from WR#
t6	15			ns	A0/CS Setup to RD#
t7	15		50	ns	Data delay from RD#
t8	5			ns	A0/CS hold from RD#
t9	0		30	ns	Data hold time from RD#

Table 4.9 CPU-Style FIFO Interface Operation Signal Timing.

An example of the CPU-style FIFO interface connection is shown in Figure 4.18

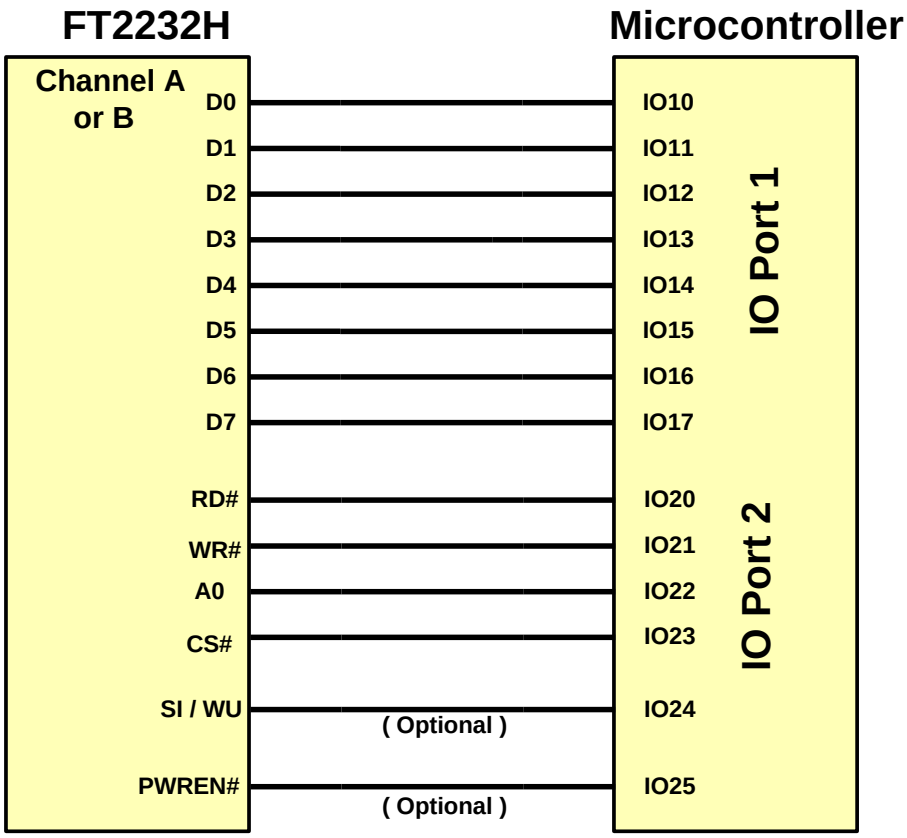


Figure 4.18 CPU-Style FIFO Interface Example

4.10 Synchronous and Asynchronous Bit-Bang Interface Mode

Description

The FT2232H channel A or channel B can be configured as a bit-bang interface. There are two types of bit-bang modes: synchronous and asynchronous.

Asynchronous Bit-Bang Mode

Asynchronous Bit-Bang mode is the same as BM-style Bit-Bang mode, except that the internal RD# and WR# strobes (RDSTB# and WRSTB#) are now brought out of the device to allow external logic to be clocked by accesses to the bit-bang IO bus.
On either or both channels any data written to the device in the normal manner will be self clocked onto the data pins (those which have been configured as outputs). Each pin can be independently set as an input or an output. The rate that the data is clocked out at is controlled by the baud rate generator.

For the data to change there has to be new data written, and the baud rate clock has to tick. If no new data is written to the channel, the pins will hold the last value written.

Synchronous Bit-Bang Mode

The synchronous Bit-Bang mode will only update the output parallel port pins whenever data is sent from the USB interface to the parallel interface. When this is done, the WRSTB# will activate to indicate that the data has been read from the USB Rx FIFO buffer and written out on the pins. Data can only be received from the parallel pins (to the USB Tx FIFO interface) when the parallel interface has been written to.

With Synchronous Bit-Bang mode data will only be sent out by the FT2232H if there is space in the FT2232H USB TXFIFO for data to be read from the parallel interface pins. This Synchronous Bit-Bang mode will read the data bus parallel I/O pins first, before it transmits data from the USB RxFIFO. It is therefore 1 byte behind the output, and so to read the inputs for the byte that you have just sent, another byte must be sent.

For example :-

(1) Pins start at 0xFF
Send 0x55,0xAA
Pins go to 0x55 and then to 0xAA
Data read = 0xFF,0x55

(2) Pins start at 0xFF
Send 0x55,0xAA,0xAA
(repeat the last byte sent)
Pins go to 0x55 and then to 0xAA

Data read = 0xFF,0x55,0xAA

Synchronous Bit-Bang Mode differs from Asynchronous Bit-Bang mode in that the device parallel output is only read when the parallel output is written to by the USB interface. This makes it easier for the controlling program to measure the response to a USB output stimulus as the data returned to the USB interface is synchronous to the output data.

Asynchronous Bit-Bang mode is enabled using Set Bit Bang Mode driver command. A hex value of 1 will enable Asynchronous Bit-Bang mode.

Synchronous Bit-Bang mode is enabled using Set Bit Bang Mode driver command. A hex value of 4 will enable Synchronous Bit-Bang mode.

See application note **AN2232-02, "Bit Mode Functions for the FT2232"** for more details and examples of using the bit-bang modes.

An example of the synchronous bi-bang mode timing is shown in Figure 4.19

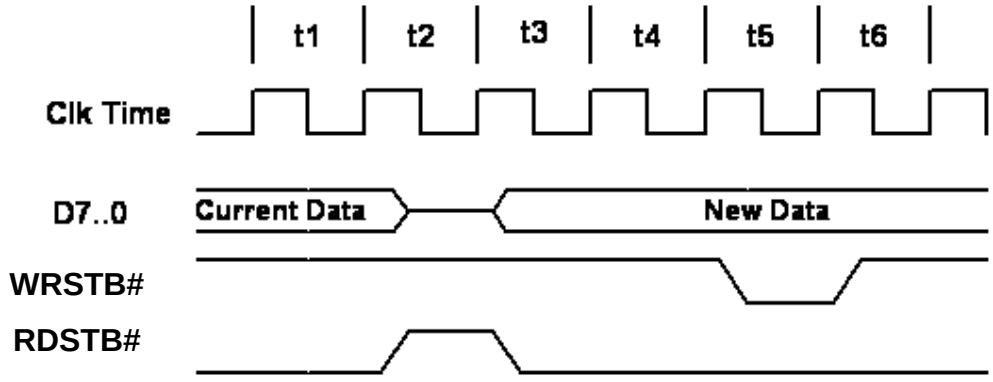


Figure 4.19 Synchronous Bit-Bang Mode Timing Interface Example

NAME	Description
t1	Current pin state is read
t2	RDSTB# is set inactive and data on the paralle I/O pins is read and sent to the USB host.
t3	RDSTB# is set active again, and any pins that are output will change to their new data
t4	1 clock cycle to allow for data setup
t5	WRSTB# goes active. This indicates that the host PC has written new data to the I/O parallel data pins
t6	WRSTB# goes inactive

Table 4.10 Synchronous Bit-Bang Mode Timing Interface Example Timings

WRSTB# = this output indicates when new data has been written to the I/O pins from the Host PC (via the USB interface).

RDSTB# = this output rising edge indicates when data has been read from the I/O pins and sent to the Host PC (via the USB interface).

The WRSTB# goes active in t4. The WRSTB# goes active when data is read from the USB RXFIFO (i.e. sent from the PC). The RDSTB# goes inactive when data is sampled from the pins and written to the USB TXFIFO (i.e. sent to the PC). The SETUP command to the FT2232H is used to setup the bit-mode. This command also contains a byte wide data mask to set the direction of each bit. The direction on each pin doesn't change unless a new SETUP command is used to modify the direction.

The WRSTB# and RDSTB# strobes are only a guide to what may be happening depending on the direction of the bus. For example if all pins are configured as inputs, it is still necessary to write to these pins in order to get the FT2232H to read those pins even though the data written will never appear on the pins.

Signals and data-flow are illustrated in **Figure 4.20**

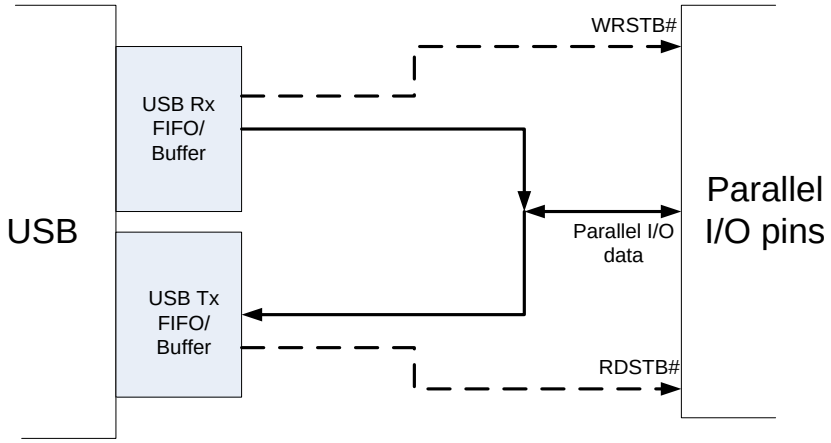


Figure 4.20 Bit-bang Mode Dataflow Illustration Diagram.

4.11 RS232 UART Mode LED Interface Description

When configured in UART mode the FT2232H has two IO pins on each channel dedicated to controlling LED status indicators, one for transmitted data the other for received data. When data is being transmitted / received the respective pins drive from tri-state to low in order to provide indication on the LED's of data transfer. A digital one-shot timer is used so that even a small percentage of data transfer is visible to the end user.

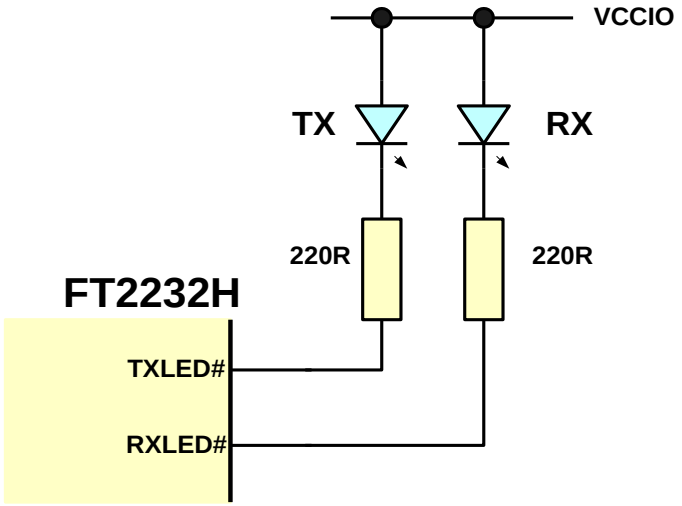


Figure 4.21 Dual LED UART Configuration

Figure 4.21 shows a configuration using two individual LED's – one for transmitted data the other for received data.

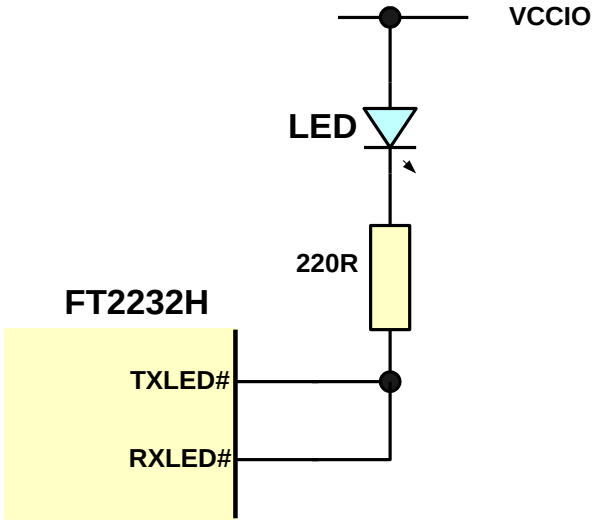


Figure 4.22 Single LED UART Configuration

In **Figure 4.22** the transmit and receive LED indicators are wire-OR'ed together to give a single LED indicator which indicates any transmit or receive data activity.

Note that the LED's are connected to the same supply as VCCIO.

4.12 Send Immediate / Wake Up (SIWU#)

The SIWU# function is available in the FIFO modes and in bitbang mode.

The Send Immediate portion is used to flush data from the chip back to the PC. This can be used to get short packets of data back to the PC without waiting for the latency timer to expire.

This mechanism should only be used when you have stopped sending data to the chip to avoid overrun.

The data transfer is flagged to the USB host by the falling edge of the signal.

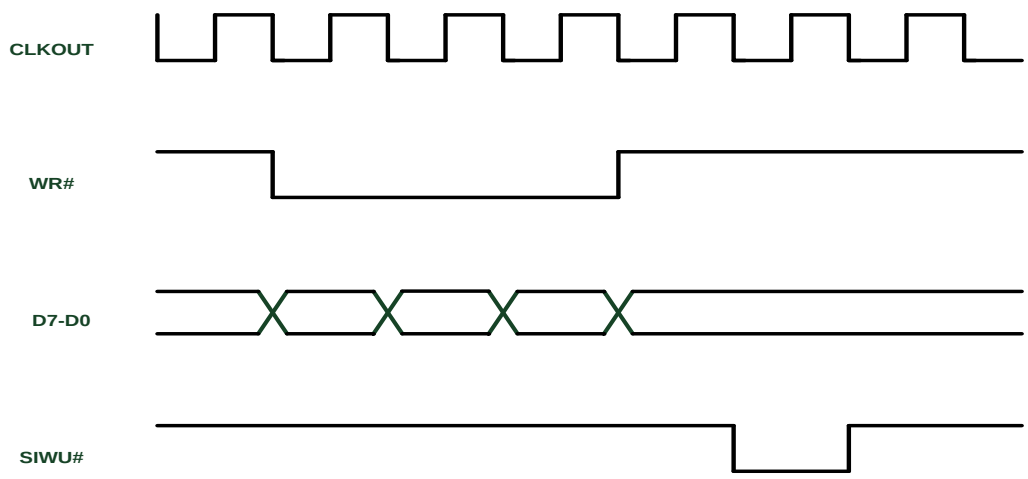


Figure 4.23: Using SIWU#

When the pin is being used for a Wake Up function to wake up a sleeping PC a 20ms negative pulse on this pin is required.

Notes

1. When using remote wake-up, ensure the resistors are pulled-up in suspend. Also ensure peripheral designs do not allow any current sink paths that may partially power the peripheral.
2. If remote wake-up is enabled, a peripheral is allowed to draw up to 2.5mA in suspend. If remote wake-up is disabled, the peripheral must draw no more than 500uA in suspend.
3. If a Pull-down is enabled, the FT2232H will not wake up from suspend.

FT2232H Mode Selection

The 2 channels of the FT2232H reset to 2 asynchronous serial interfaces.

Following a reset the required mode of each channel is determined by the contents of the EEPROM (programmed using MPROG V3.4a or later).

The EEPROM contents determine if the 2 channels have been configured as FT232 asynchronous serial interface, FT245 FIFO interface, CPU-style FIFO interface or Fast Serial Interface.

Following a reset, the EEPROM is read to determine which mode is configured. After device enumeration, an ***FT_SetBitMode*** command (refer to *D2XX_Programmers_Guide*) can be sent to the USB driver to switch the selected interface into the required mode – asynchronous bit-bang, synchronous bit-bang or MPSSE.

When in FT245 FIFO mode, the ***FT_SetBitMode*** command can be used to select either Synchronous FIFO (***FT_SetBitMode*** = 0x40) or Asynchronous FIFO mode. (Note that Asynchronous FIFO mode must be selected on both channels before selecting the Synchronous FIFO mode. This means that an EEPROM is needed to initially configure Asynchronous FIFO mode before software configures the Synchronous FIFO mode).

When Synchronous FIFO mode selected, channel A uses all the memory resources of channel B. As such channel B is then not available. In this case the state of the channel B pins is determined when the configuration is switched to Asynchronous FIFO mode. If channel B had not been used for any data transfer before configuration of Asynchronous FIFO mode, then the channel B pins will remain in their default mode (D7:0=tri-stated but pulled high trough 75K resistor, TXE# =low, RXF# =high. RD# and WR# are inputs and should be pulled high). An MPSSE command, ***set_data_bits*** can be used to configure the channel B pins as inputs before configuring channel A as Synchronous FIFO. This avoids the channel B pins driving against any interfaces (such as SPI) which may have been configured previous to any switching of channel A to Synchronous FIFO mode. Refer to http://www.ftdichip.com/Documents/AppNotes/AN2232C-01_MPSSE_Cmnd.pdf for the ***set_data_bits*** command and further information on the MPSSE used in MCU Host BUS Emulation mode.

The MPSSE can be configured directly using the D2XX commands. The *D2XX_Programmers_Guide* is available from the FTDI website at http://www.ftdichip.com/Documents/ProgramGuides/D2XX_Programmer's_Guide(FT_000071).pdf

The application note **AN_108 – "Command Processor For MPSSE and MCU Host Bus Emulation Modes"** gives further explanation and examples for the MPSSE.

4.12.1 Do I need an EEPROM?

The following table **Table 4.11**summarises what modes are configurable using the EEPROM or the application software.

	ASYNC Serial UART	ASYNC 245 FIFO	SYNC 245 FIFO	ASYNC Bit-bang	SYNC Bit-bang	MPSSE	Fast Serial interface	CPU-Style FIFO	Host Bus Emulation
EEPROM configured	YES	YES	YES				YES	YES	
Application Software configured			YES	YES	YES	YES			YES

Table 4.11 Configuration Using EEPROM and Application Software

5 Devices Characteristics and Ratings

5.1 Absolute Maximum Ratings

The absolute maximum ratings for the FT2232H devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these values may cause permanent damage to the device.

Parameter	Value	Unit
Storage Temperature	-65°C to 150°C	Degrees C
Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity)	168 Hours (IPC/JEDEC J-STD-033A MSL Level 3 Compliant)*	Hours
Ambient Operating Temperature (Power Applied)	-40°C to 85°C	Degrees C
MTTF FT2232HL	TBD	hours
MTTF FT2232HQ	TBD	hours
VCORE Supply Voltage	-0.3 to +2.0	V
VCCIO IO Voltage	-0.3 to +4.0	V
DC Input Voltage – USBDP and USBDM	-0.5 to +3.63	V
DC Input Voltage – High Impedance Bi-directionals (powered from VCCIO)	-0.3 to +5.8	V
DC Input Voltage – All Other Inputs such as PWREN#, SUSPEND#, RESET#, EECS, EECLK, EEDATA	-0.5 to + (VCCIO +0.5)	V
DC Output Current – Outputs	16	mA

Table 5.1 Absolute Maximum Ratings

* If devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of +125°C and baked for up to 17 hours.

5.2 DC Characteristics

The I/O pins are +3.3v cells, which are +5V tolerant (except the USB PHY pins).

DC Characteristics (Ambient Temperature = -40°C to +85°C)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
VCORE	VCC Core Operating Supply Voltage	1.62	1.80	1.98	V	
VCCIO*	VCCIO Operating Supply Voltage	2.97	3.30	3.63	V	Cells are 5V tolerant
VREGIN	VREGIN Voltage regulator Input	3.00	3.30	3.60	V	
VREGOUT	Voltage regulator Output	1.71	1.80	1.89	V	
Ireg	Regulator Current			150	mA	VREGIN +3.3V
Icc1	Core Operating Supply Current	---	70	---	mA	VCORE = +1.8V Normal Operation
Icc1r	Core Reset Supply Current	---	5	---	mA	VCORE = +1.8V Device in reset state
Icc1s	Core Suspend Supply Current		500		µA	VCORE = +1.8V USB Suspend

Table 5.2 Operating Voltage and Current (except PHY)

*NOTE: Failure to connect all VCCIO pins will result in failure of the device.

The I/O pins are +3.3v cells, which are +5V tolerant (except the USB PHY pins).

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.40	3.14		V	Ioh = +/-2mA I/O Drive strength* = 4mA
			3.20		V	I/O Drive strength* = 8mA
			3.22		V	I/O Drive strength* = 12mA
			3.22		V	I/O Drive strength* = 16mA
Vol	Output Voltage Low		0.18	0.40	V	Iol = +/-2mA I/O Drive strength* = 4mA
			0.12		V	I/O Drive strength* = 8mA
			0.08		V	I/O Drive strength* = 12mA
			0.07		V	I/O Drive strength* = 16mA
Vil	Input low Switching Threshold		-	0.80	V	LVTTL
Vih	Input High Switching Threshold	2.00	-		V	LVTTL
Vt	Switching Threshold		1.50		V	LVTTL
Vt-	Schmitt trigger negative going threshold voltage	0.80	1.10	-	V	
Vt+	Schmitt trigger positive going threshold voltage		1.60	2.00	V	
Rpu	Input pull-up resistance	40	75	190	KΩ	Vin = 0
Rpd	Input pull-down resistance	40	75	190	KΩ	Vin =VCCIO
Iin	Input Leakage Current	15	45	85	µA	Vin = 0
Ioz	Tri-state output leakage current		+/-10		µA	Vin = 5.5V or 0

Table 5.3 I/O Pin Characteristics VCCIO = +3.3V (except USB PHY pins)

* The I/O drive strength and slow slew-rate are configurable in the EEPROM.

DC Characteristics (Ambient Temperature = -40°C to +85°C)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
VPHY, VPLL	PHY Operating Supply Voltage	3.0	3.3	3.6	V	3.3V I/O
Iccphy	PHY Operating Supply Current	---	30	60	mA	High-speed operation at 480 MHz
Iccphy (susp)	PHY Operating Supply Current	---	10	50	µA	USB Suspend

Table 5.4 PHY Operating Voltage and Current

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	VCORE-0.2			V	
Vol	Output Voltage Low			0.2	V	
Vil	Input low Switching Threshold		-	0.8	V	
Vih	Input High Switching Threshold	2.0	-		V	

Table 5.5 PHY I/O Pin Characteristics

5.3 ESD Tolerance

ESD protection for FT2232H IO's

Parameter	Reference	Minimum	Typical	Maximum	Units
Human Body Model (HBM)	JEDEC EIA/JESD22-A114-B, Class 2		±2kV		kV
Machine Mode (MM)	JEDEC EIA/JESD22-A115-A, Class B		±200V		V
Charge Device Model (CDM)	JEDEC EIA/ JESD22-C101-D, Class-III		±500V		V
Latch-up	JESD78, Trigger Class-II		±200mA		mA

Table 5.6 ESD Tolerance

6 FT2232H Configurations

The following sections illustrate possible USB power configurations for the FT2232H.

All USB power configurations illustrated apply to both package options for the FT2232H device

6.1 USB Bus Powered Configuration

Bus Powered Application example 1: Bus powered configuration

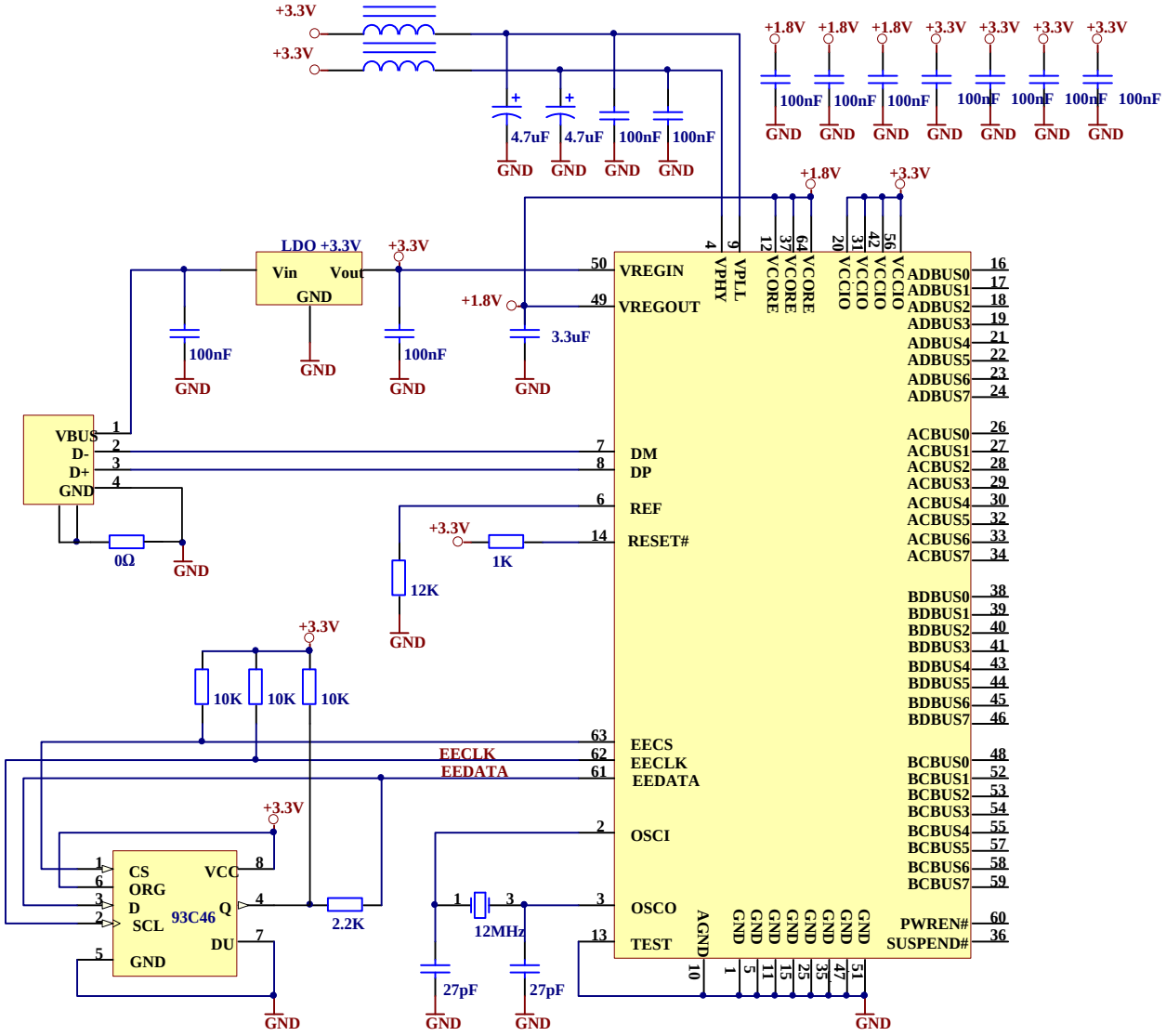


Figure 6.1 Bus Powered Configuration Example 1

Figure 6.1 illustrates the FT2232H in a typical USB bus powered design configuration. A USB bus powered device gets its power from the USB bus. In this application, the FT2232H requires that the VBUS (USB +5V) is regulated down to +3.3V (using an LDO) to supply the VCCIO, VPLL, VPHY and VREGIN.

VREGIN is the +3.3V input to the on chip +1.8V regulator. The output of the on chip LDO regulator (+1.8V) drives the FT2232H core supply (VCORE). This requires a minimum of a 3.3uF filter capacitor.

Bus Powered Application example 2: Bus powered configuration (with additional 1.8V LDO voltage regulator for VCORE)

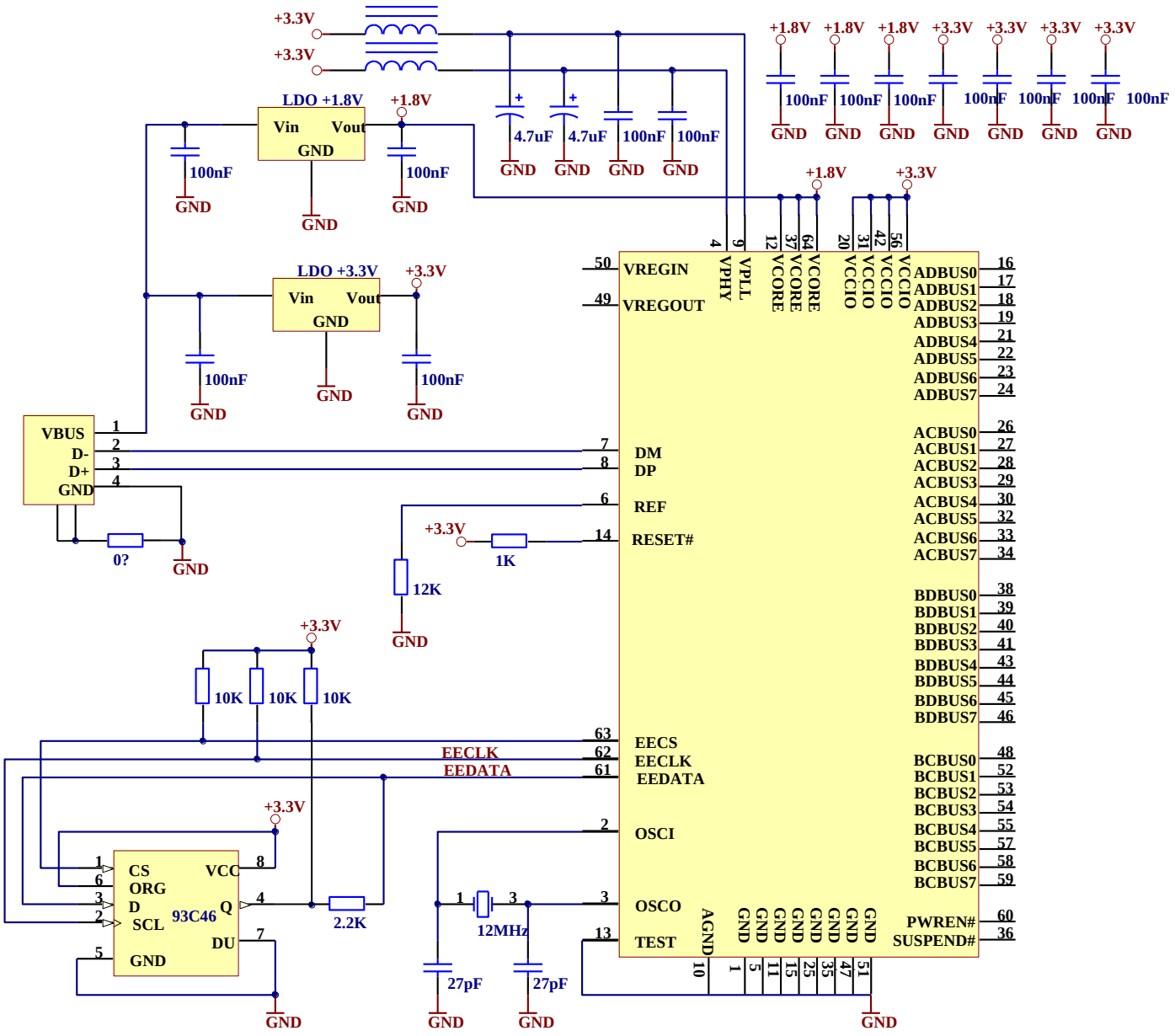


Figure 6.2 Bus Powered Configuration Example 2

Figure 6.3 illustrates the FT2232H in a typical USB bus powered configuration similar to Figure 6.1. The difference here is that the +1.8V for the FT2232H core (VCORE) has been regulated from the VBUS as well as the +3.3V supply to the VPLL, VPHY, VCCIO and VREGIN.

6.2 USB Self Powered Configuration

Self Powered application example 1: Self powered configuration

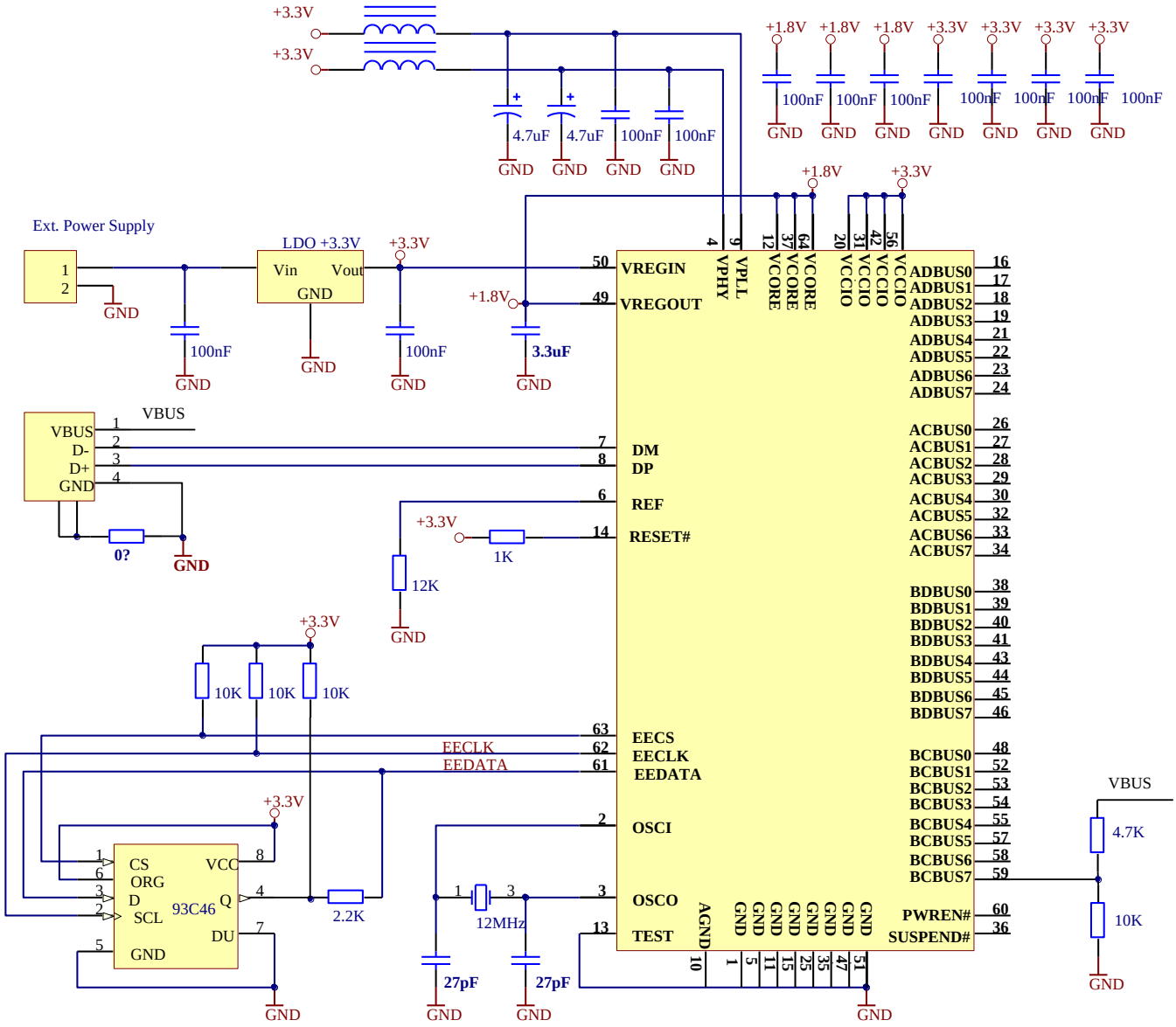


Figure 6.3 Self Powered Configuration Example 1

Figure 6.3 illustrates the FT2232H in a typical USB self powered configuration. A USB self powered device gets its power from its own power supply and does not draw current from the USB bus. In this example an external power supply is used. This external supply is regulated to +3.3V.

Note that in this set-up, the EEPROM should be configured for self-powered operation and the option "suspend on DBUS7 low" selected in MPROG. Also this configuration uses the pin BCBUS7, so this assumes that MPSSE mode is not selected.

Self Powered application example 2: Self powered configuration (with additional 1.8V LDO voltage regulator for VCORE)

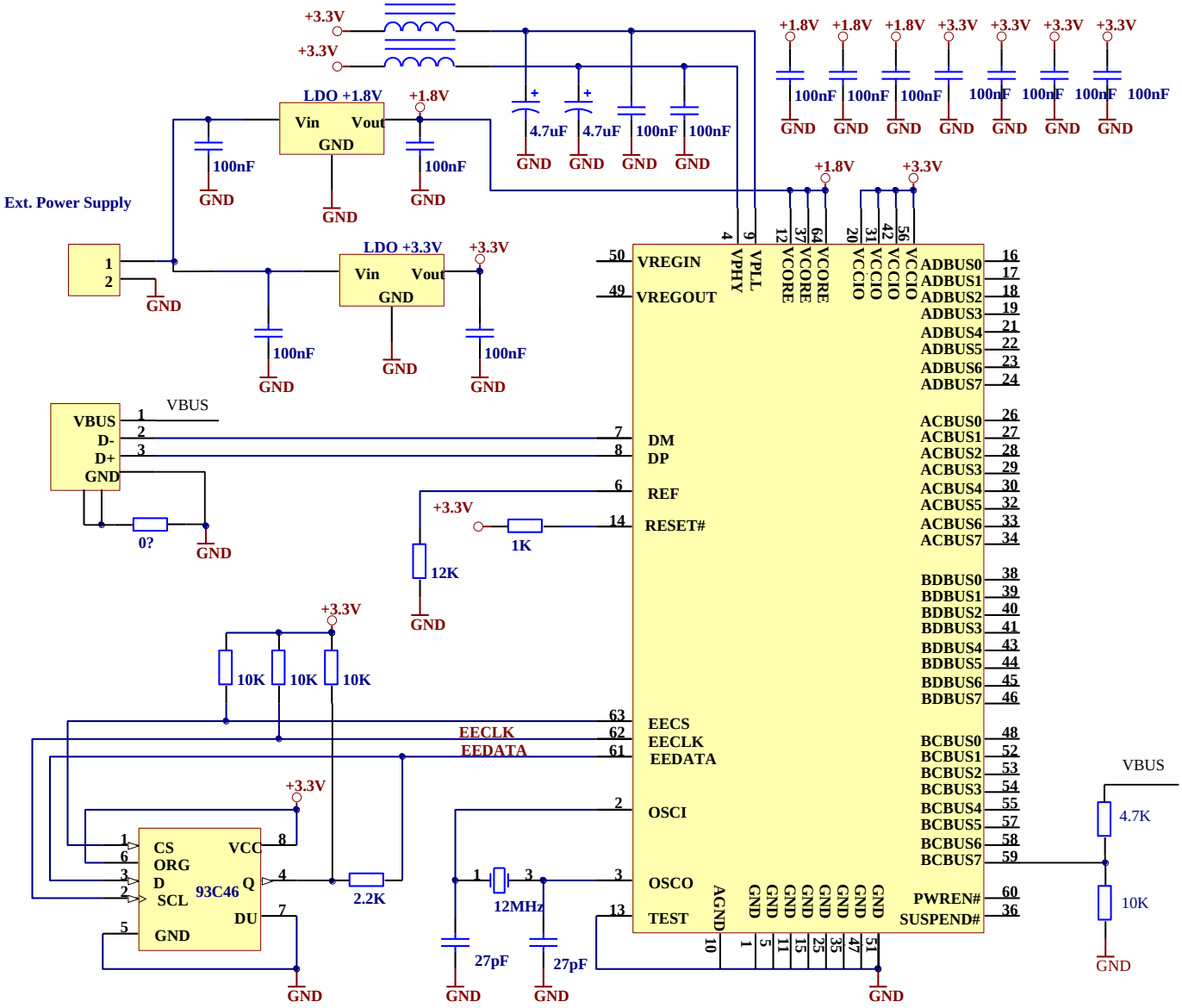


Figure 6.4 Self Powered Configuration Example 2

Figure 6.4 illustrates the FT2232H in a typical USB self powered configuration similar to Figure 6.3. The difference here is that the +1.8V for the FT2232H core has been regulated from the external power supply.

Note that in this set-up, the EEPROM should be configured for self-powered operation and the option "suspend on DBUS7 low" selected in MPROG. Also this configuration uses the pin BCBUS7, so this assumes that MPSSE mode is not selected.

6.3 Oscillator Configuration

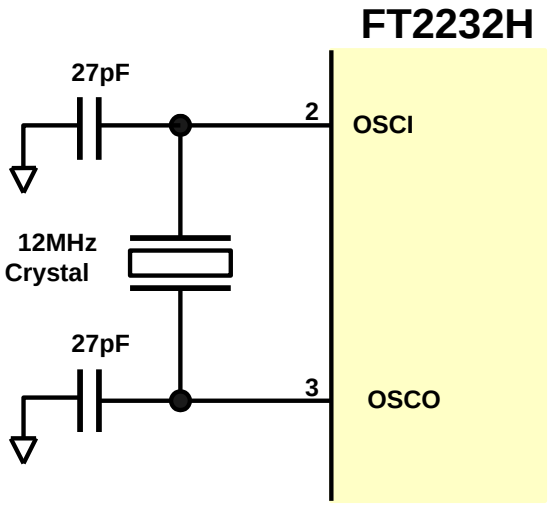


Figure 6.5 Recommended FT2232H Crystal Oscillator Configuration.

Figure 6.5 illustrates how to connect the FT2232H with a 12MHz ± 0.003% crystal. In this case loading capacitors should to be added between OSCI, OSCO and GND as shown. A value of 27pF is shown as the capacitor in the example – this will be good for many crystals but it is recommended to select the loading capacitor value based on the manufacturer's recommendations wherever possible. It is recommended to use a parallel cut type crystal.

It is also possible to use a 12 MHz Oscillator with the FT2232H. In this case the output of the oscillator would drive OSCI, and OSCO should be left unconnected. The oscillator must have a CMOS output drive capability.

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
OSCI Vin	Input Voltage	2.97	3.30	3.63	V	
FIn	Input Frequency		12		MHz	+/- 30ppm
Ji	Cycle to cycle jitter		< 150		pS	

Table 6.1 OSCI Input characteristics

7 EEPROM Configuration

If an external EEPROM is fitted (93LC46/56/66) it can be programmed over USB using MPROG V3.4a or later. The EEPROM must be 16 bits wide and capable or working at a VCC supply of +3.0 to +3.6 volts.

8 Package Parameters

The FT2232H is available in two different packages. The FT2232HL is the LQFP-64 option and the FT2232HQ is the QFN-64 package option. The solder reflow profile for both packages is described in Section 8.3

8.1 FT2232HQ, QFN-64 Package Dimensions

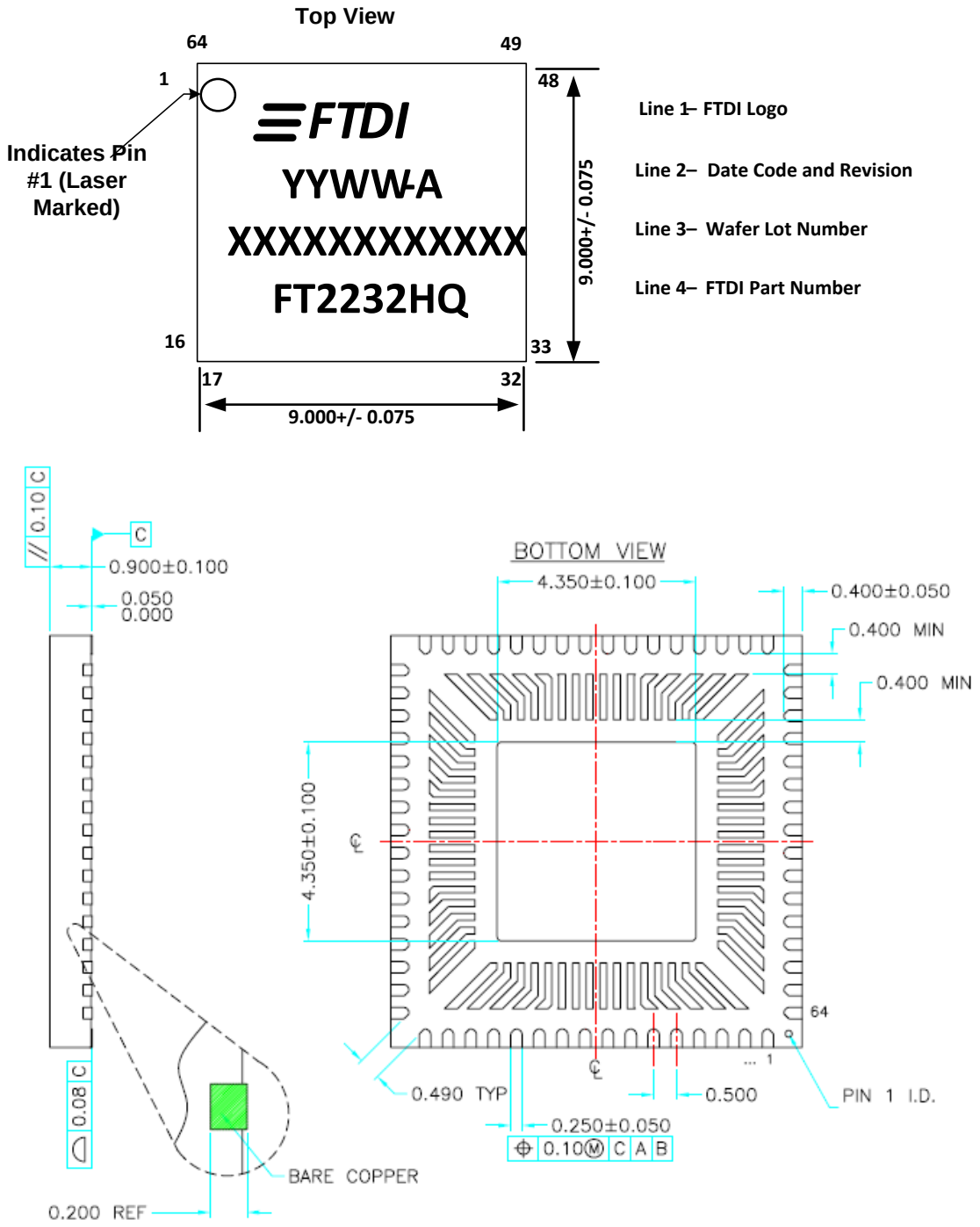
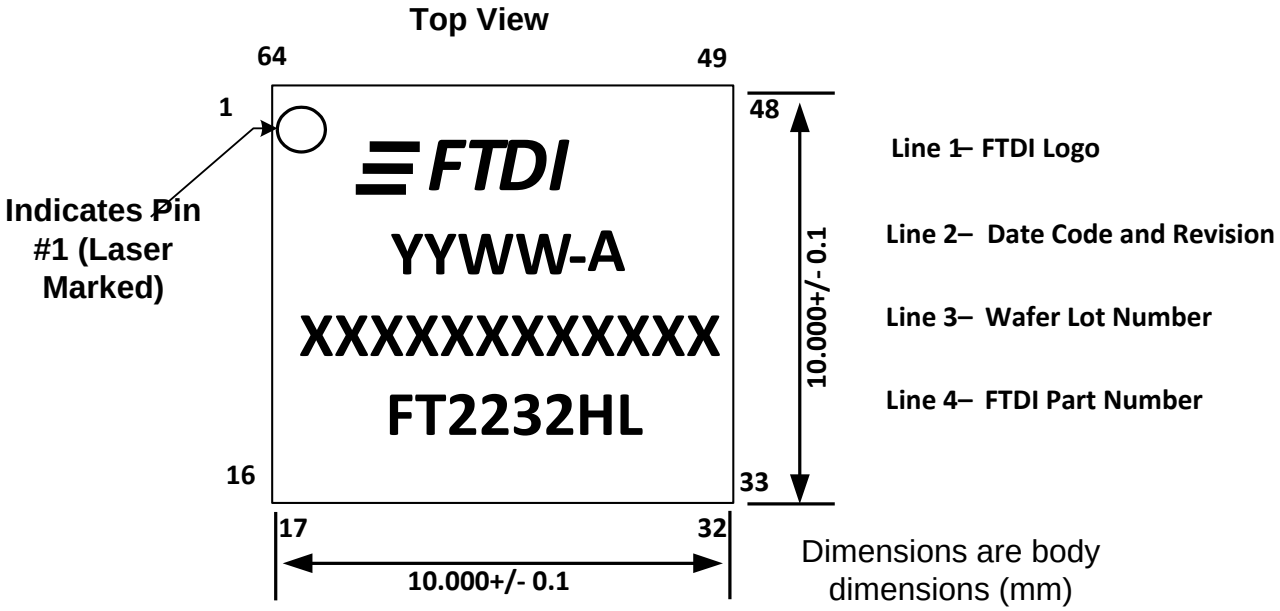


Figure 8.1 64 pin QFN Package Details

Notes
1. All dimensions are in mm.
2. Pin 1 ID can be combination of DOT AND/OR Chamfer.
3. Pin 1 ID is NOT connected to the internal ground of the device. It is internally connected to the bottom side central solder pad, which is 4.35 x 4.35mm.
4. Pin 1 ID can be connected to system ground, but it is not recommended using this as a ground point for the device.
5. Optional Chamfer on corner leads.

8.2 FT2232HL, LQFP-64 Package Dimensions



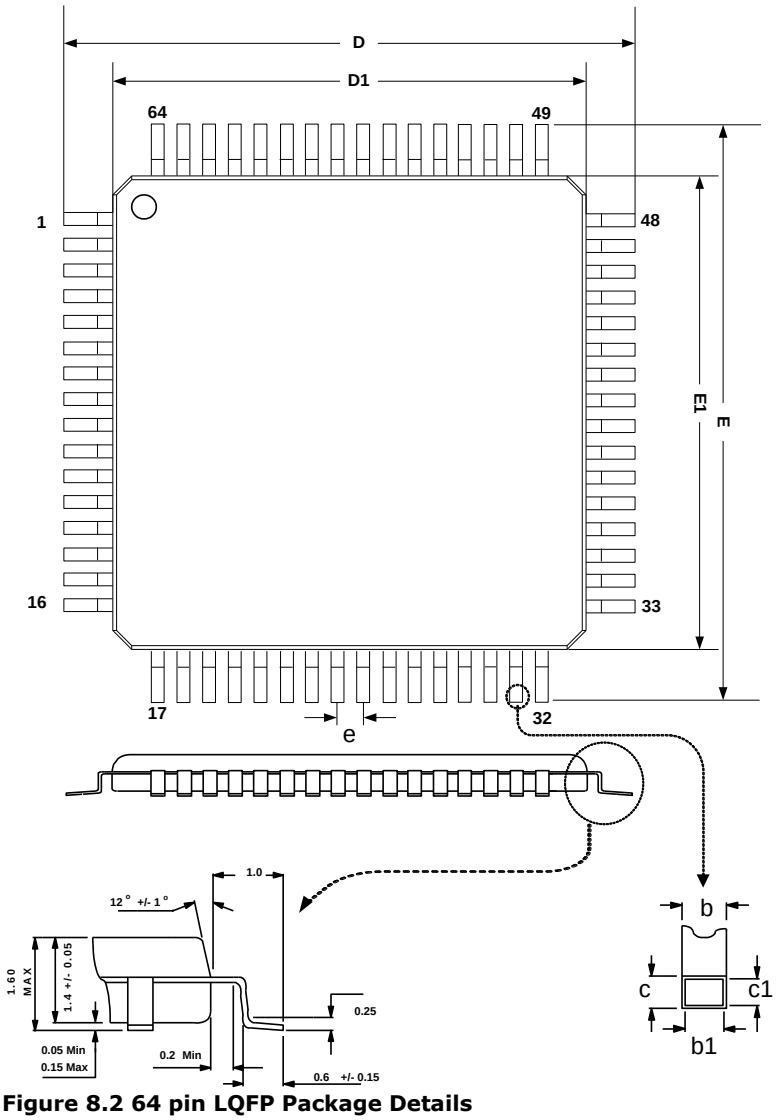


Figure 8.2 64 pin LQFP Package Details

SYMBOL	MIN	NOM	MAX
D	11.8	12	12.2
D1	9.9	10	10.1
E	11.8	12	12.2
E1	9.9	10	10.1
b	0.17	0.22	0.27
c	0.09		0.2
b1	0.17	0.2	0.23
c1	0.09		0.16
e		0.5 BSC	

Table 8.1 64 pin LQFP Package Details – dimensions (in mm)

8.3 Solder Reflow Profile

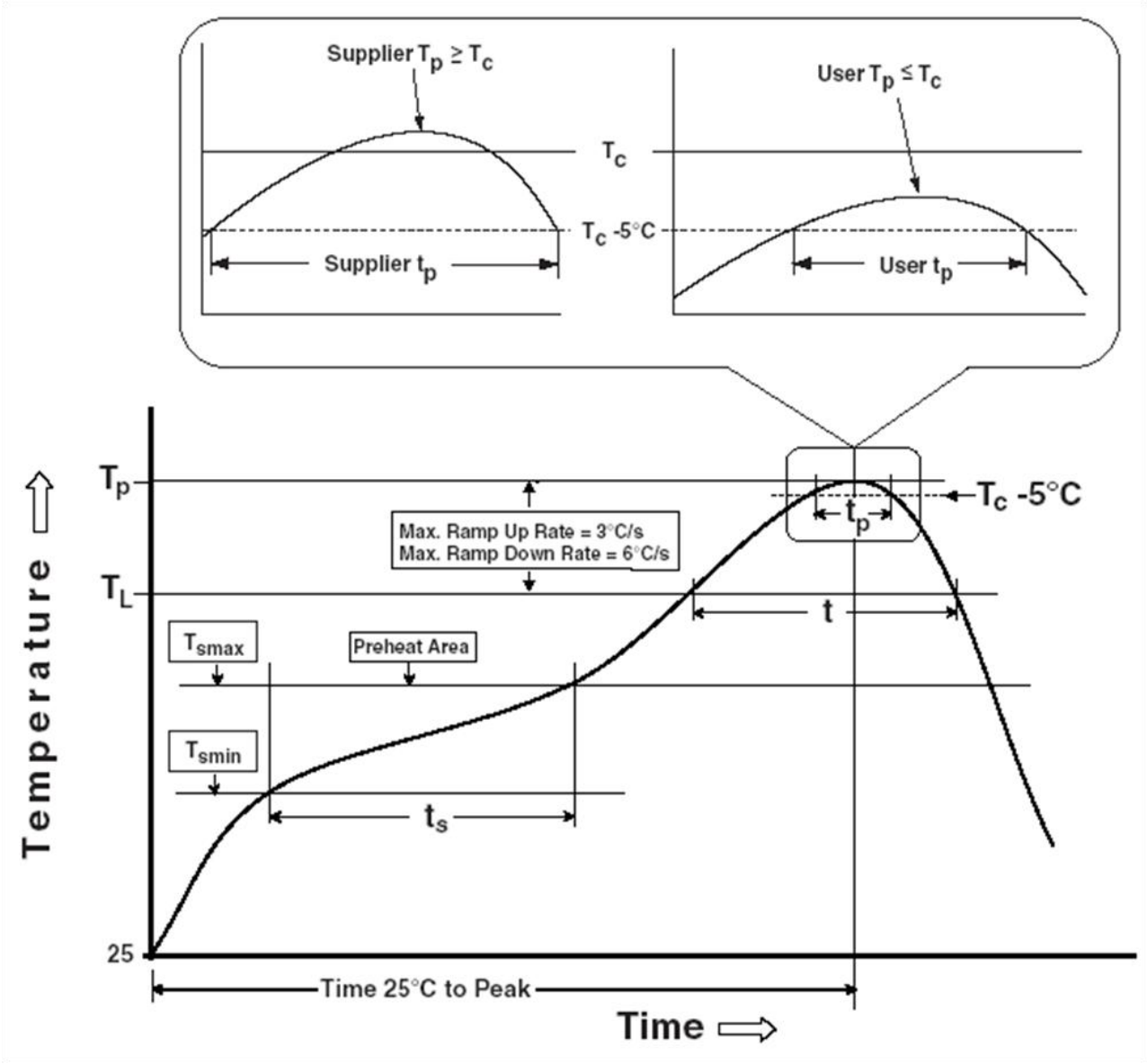


Figure 8.3 64 pin LQFP and QFN Reflow Solder Profile

Profile Feature	Pb Free Solder Process (green material)	SnPb Eutectic and Pb free (non green material) Solder Process
Average Ramp Up Rate (T_s to T_p)	3°C / second Max.	3°C / Second Max.
Preheat - Temperature Min (T_s Min.) - Temperature Max (T_s Max.) - Time (t_s Min to t_s Max)	 150°C 200°C 60 to 120 seconds	 100°C 150°C 60 to 120 seconds
Time Maintained Above Critical Temperature T_L: - Temperature (T_L) - Time (t_L)	 217°C 60 to 150 seconds	 183°C 60 to 150 seconds
Peak Temperature (T_p)	260°C	see Table 8.3
Time within 5°C of actual Peak Temperature (t_p)	30 to 40 seconds	20 to 40 seconds
Ramp Down Rate	6°C / second Max.	6°C / second Max.
Time for T= 25°C to Peak Temperature, T_p	8 minutes Max.	6 minutes Max.

Table 8.2 Reflow Profile Parameter Values

SnPb Eutectic and Pb free (non green material)		
Package Thickness	Volume mm3 < 350	Volume mm3 >=350
< 2.5 mm	235 +5/-0 deg C	220 +5/-0 deg C
≥ 2.5 mm	220 +5/-0 deg C	220 +5/-0 deg C
Pb Free (green material) = 260 +5/-0 deg C		

Table 8.3 Package Reflow Peak Temperature

9 Contact Information

Head Office – Glasgow, UK

Future Technology Devices International Limited
Unit 1, 2 Seaward Place,
Glasgow G41 1HH
United Kingdom
Tel: +44 (0) 141 429 2777
Fax: +44 (0) 141 429 2758

E-mail (Sales) sales1@ftdichip.com
E-mail (Support) support1@ftdichip.com
E-mail (General Enquiries) admin1@ftdichip.com
Web Site URL http://www.ftdichip.com
Web Shop URL http://www.ftdichip.com

Branch Office – Taipei, Taiwan

Future Technology Devices International Limited (Taiwan)
2F, No. 516, Sec. 1, NeiHu Road
Taipei 114
Taiwan , R.O.C.
Tel: +886 (0) 2 8797 1330
Fax: +886 (0) 2 8751 9737

E-mail (Sales) tw.sales1@ftdichip.com
E-mail (Support) tw.support1@ftdichip.com
E-mail (General Enquiries) tw.admin1@ftdichip.com
Web Site URL http://www.ftdichip.com

Branch Office – Hillsboro, Oregon, USA

Future Technology Devices International Limited (USA)
7235 NW Evergreen Parkway, Suite 600
Hillsboro, OR 97123-5803
USA
Tel: +1 (503) 547 0988
Fax: +1 (503) 547 0987

E-Mail (Sales) us.sales@ftdichip.com
E-Mail (Support) us.support@ftdichip.com
E-Mail (General Enquiries) us.admin@ftdichip.com
Web Site URL http://www.ftdichip.com

Branch Office – Shanghai, China

Future Technology Devices International Limited (China)
Room 408, 317 Xianxia Road,
ChangNing District,
ShangHai, China

Tel: +86 (21) 62351596
Fax: +86(21) 62351595

E-Mail (Sales): cn.sales@ftdichip.com
E-Mail (Support): cn.support@ftdichip.com
E-Mail (General Enquiries): cn.admin1@ftdichip.com
Web Site URL: http://www.ftdichip.com

Distributor and Sales Representatives

Please visit the Sales Network page of the FTDI Web site for the contact details of our distributor(s) and sales representative(s) in your country.

Appendix A – List of Figures and Tables

List of Tables

List of Figures

Appendix B – Revision History

Revision History		
Version draft	Initial Datasheet Created	October 2008
Version Preliminary	Preliminary Datasheet Released	23rd October 2008
Version 1.00	Datasheet Released	4th November 2008
Version 1.10	QFN Package updated	November 2008
Version 2.00	Various Updates	January 2009
Version 2.01	Corrections made to table 3.6, 3.7, table on page 8. Changed description of WRSTRB# and RDSTRB# Added note that HBE mode only operates at 60MHz	February 2009
Version 2.02	Corrections made to tray QFN 160 changed to 260 Correction made to 3.4.2, falling changed to rising	March 2009
Version 2.03	Corrections made to TxLED and RxLED pin connections Corrected signals in Figure 4.16. Corrected signal names in Fig 2.1 Added reference to AN_108, AN_109, AN_110, AN_111 and AN_113.	19th May 2009
Version 2.04	Added paragraph on latency timer to section 4.1	3rd June 2009
Version 2.05	Corrected Figures 6.2, 6.3 an 6.4 – missing regulators and better way of holding self powered designs in reset if not connected to USB. Corrected Max DC inputs on "DC Input Voltage – "All Other Inputs" pins from VCORE+0.5V to VCCIO+0.5V	17th June 2009
Version 2.06	Added explanation of SIWU (4.12) Added explanation of MPSSE Adaptive clocking (4.6.1). Corrected 12MHz crystal specification. Added # to TXLED, RXLED on table 3.4. Corrected TX_LED and RX_LED connections on Fig 4.1	21st Sept 2009
Version 2.07	Edited Table 3.11, references AN2232L-1 to AN_108 Updated and formatted contact information. Corrected TOC.	12 March 2010
Version 2.08	Added TID number (Section 1.3) Added ESD specifications	24th May 2010
Version 2.09	Corrected 'WR' to 'WR#' throughtout the datasheet Edited table 4.1 (T8 and T13 Comments) Edited section 4.7.1 and 4.7.2 Section 4.12, added clarifications about Wake up Clarified unsupported baud rates of 7,9,10 and 11 Mbaud.	2nd Sept 2010