21V, 5A, 500KHz Synchronous PWM-Buck DC/DC Converter

Description

FR9809 is a high-efficiency synchronous step-down DC/DC converter that employs a special process technique to obtain very low R_{DS}(ON) for the internal metal–oxide–semiconductor field-effect transistor (MOSFET). The input operation voltage is in a wide range from 4.75V to 21V, and continuous load current capability is 5A. Control circuit is designed by a particular current mode which provides fast transient response and eases loop stabilization.

This product has a very low standby current less than 1μA in shutdown mode. When the $\overline{\text{SHDN}}$/S pin voltage is less than 0.4V, FR9809 will turn off. Fault protection includes over current protection (OCP), under voltage lockout protection (UVLO) and over temperature protection (OTP) function.

This high-efficiency current mode step-down “Green Power Converter” offers the standard SOP-8 package with an exposed pad.

Features

- High Efficiency up to 90%
- Internal MOSFET R_{DS}(ON): 110mΩ/20mΩ
- Internal Compensation
- Input Operation Voltage Range: 4.75V to 21V
- 5A Continuous Output Current
- Output Voltage down to 0.805V
- 500KHz Oscillation Frequency
- Sync to External Clock from 300KHz to 800KHz
- Cycle-by-Cycle Current Limit
- Under Voltage Lockout
- Over-Temperature Protection with Auto Recovery
- <1μA Shutdown Current
- Thermal Enhanced SOP-8 (Exposed Pad) Package
- RoHS Compliant

Applications

- Networking Equipment
- OLPC, Netbook
- Distributed Power System
- LCD Monitor, TV, STB
- External HDD
- Security System

Pin Assignments

SP Package (SOP-8 Exposed Pad)

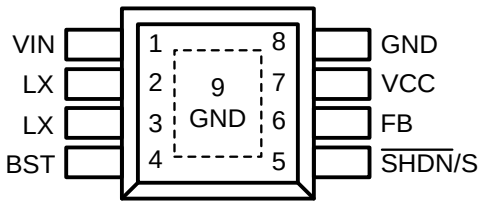
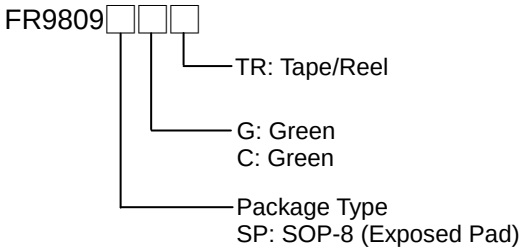


Figure 1. Pin Assignment of FR9809

Ordering Information



Typical Application Circuit

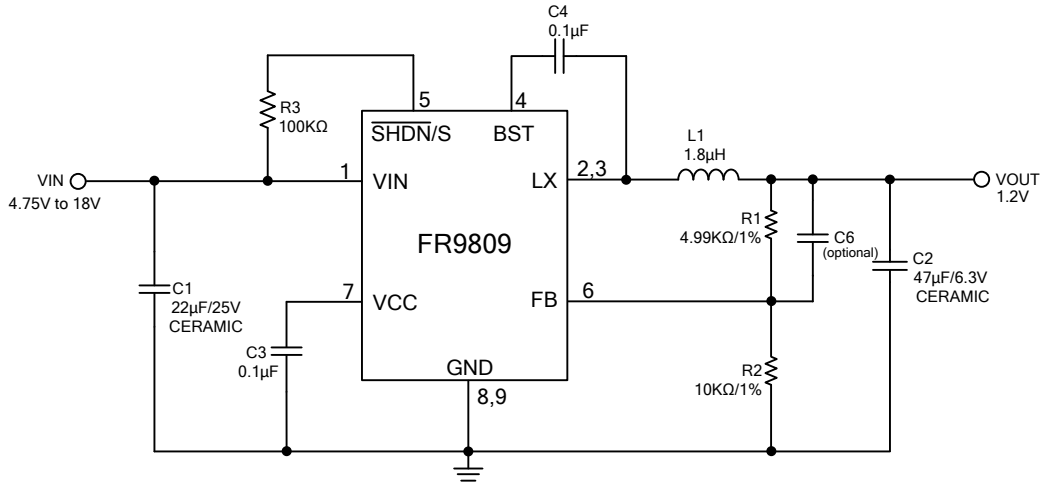


Figure 2. Output 1.2V Application Circuit

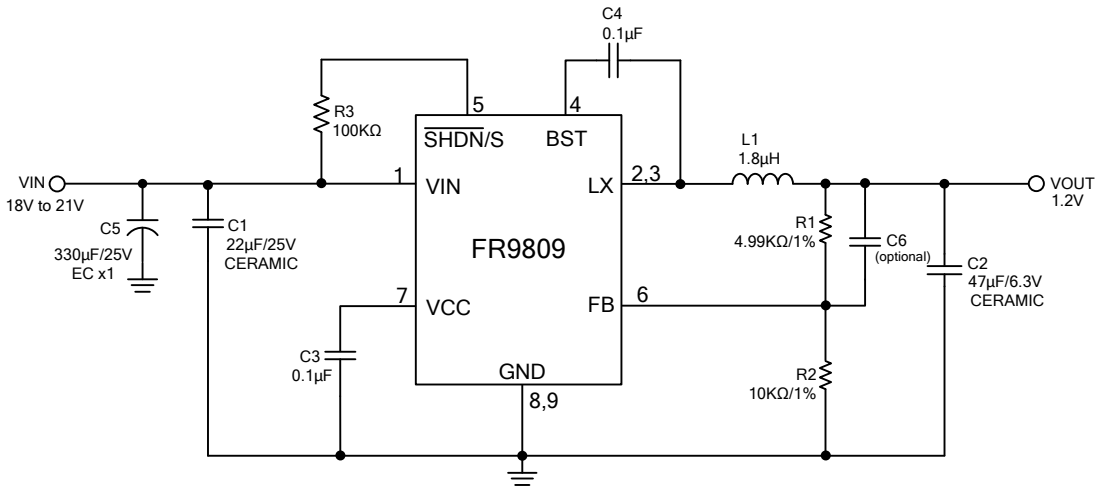


Figure 3. High Input Voltage Application Circuit

Functional Pin Description

I/O	Pin Name	Pin No.	Pin Function
I	FB	6	Voltage Feedback Input Pin. FB and VOUT are connected by a resistive voltage divider. This IC senses feedback voltage via FB and regulates it at 805mV.
I	VIN	1	Power Supply Input Pin. Drive 4.75V~21V voltage to this pin to power on this chip. A 22µF ceramic bypass capacitor is connected between VIN and GND to eliminate noise.
O	VCC	7	Bias Supply Output Pin. A 0.1µF capacitor must be connected from this pin to GND.
I	$\overline{\text{SHDN}}$/S	5	This pin provides a digital control to turn the converter on or off. For automatic start-up, connect the $\overline{\text{SHDN}}$/S pin to VIN pin with a 100KΩ resistor. An external clock from 300KHz to 800KHz can be applied to the $\overline{\text{SHDN}}$/S pin to change oscillation frequency.
O	LX	2,3	Power Switching Output Pin. This is the output pin that internal high-side NMOS switches to supply power.
O	BST	4	High-Side Gate-Drive BST Input. A 0.1µF capacitor is connected from this pin to LX. It can boost the gate drive to fully turn on the internal high-side NMOS.
I	GND	8	Ground Pin. This pin is connected to the exposed pad with copper.
I	Exposed Pad	9	Ground Pin. The exposed pad must be soldered to a large PCB area and connected to GND for maximum power dissipation.

Block Diagram

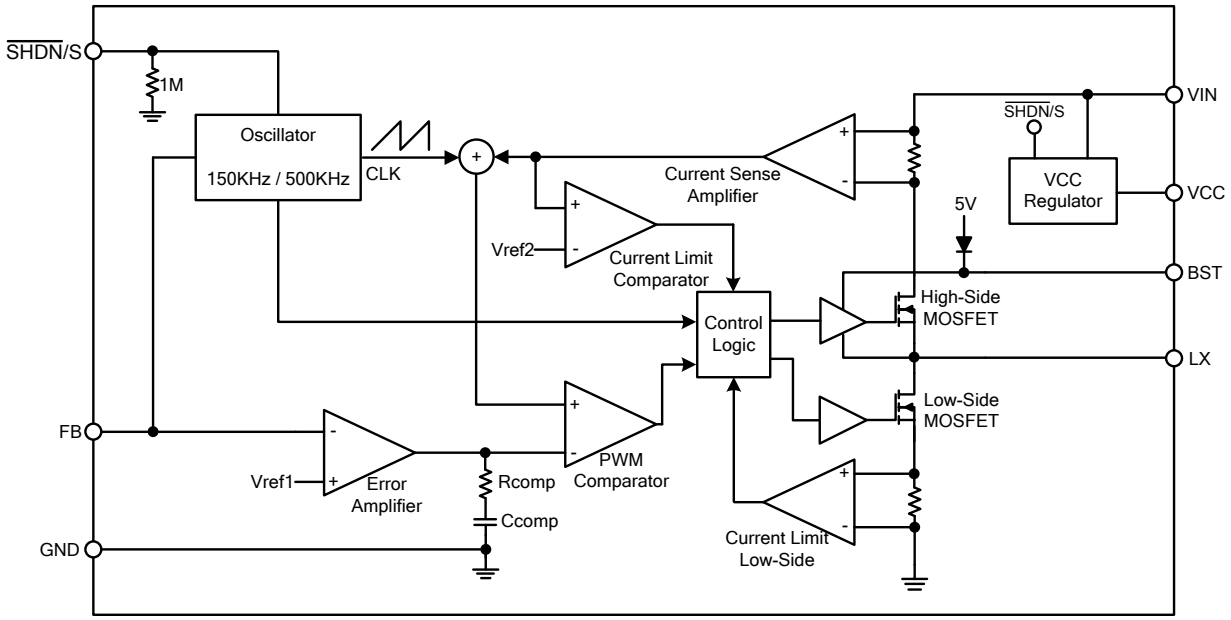


Figure 4. Block Diagram of FR9809

Absolute Maximum Ratings

- Input Supply Voltage V_{IN} ---------- -0.3V to +23V
- LX Voltage V_{LX} ---------- -0.3V to V_{IN} +1V
- BST Voltage V_{BST} ---------- V_{LX} -0.3V to V_{LX} +6V
- All Other Pins Voltage ---------- -0.3V to +6V
- Maximum Junction Temperature (T_J) ---------- +150°C
- Storage Temperature (T_S) ---------- -65°C to +150°C
- Lead Temperature (Soldering, 10sec.) ---------- +260°C
- Power Dissipation @T_A=25°C, (P_D)

  SOP-8 (Exposed Pad) ---------- 2.08W
- Package Thermal Resistance, (θ_{JA})

  SOP-8 (Exposed Pad) ---------- 60°C/W
- Package Thermal Resistance, (θ_{JC})

  SOP-8 (Exposed Pad) ---------- 15°C/W

Note 1：Stresses beyond those listed under “Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions

- Input Supply Voltage (V_{IN}) ---------- +4.75V to +21V
- Operation Temperature Range ---------- -40°C to +85°C

Electrical Characteristics

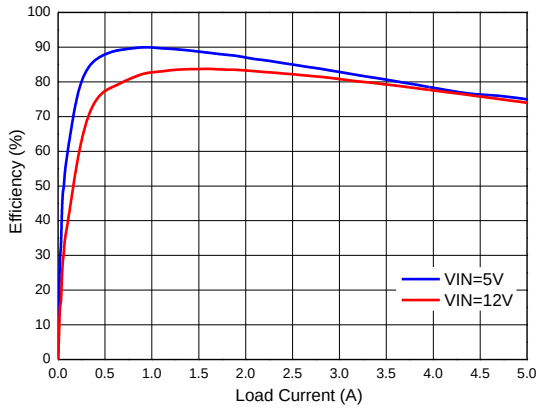
(V_{IN}=12V, T_A=25°C, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Supply Voltage	V_{IN}		4.75		21	V
VIN Shutdown Supply Current	I_{SD}	$V_{\overline{SHDN}}$=0V			1	μA
VIN Quiescent Supply Current	I_{DDQ}	$V_{\overline{SHDN}}$=2V, V_{FB}=1V		1.5		mA
Feedback Voltage	V_{FB}	4.75V≦V_{IN}≦21V	780	805	830	mV
High-Side MOSFET R_{DS}(ON) (Note2)	HSR_{DS}(ON)			110		mΩ
Low-Side MOSFET R_{DS}(ON) (Note2)	LSR_{DS}(ON)			20		mΩ
MOSFET Leakage Current	I_{LX}(Leak)	$V_{\overline{SHDN}}$=0V, V_{LX}=0V		0	10	μA
High-Side MOSFET Current Limit (Note2)	I_{LIMIT}			8		A
Maximum Duty Cycle	D_{MAX}	V_{FB}=0.7V		90		%
Oscillation frequency	F_{LX}		350	500	650	KHz
Short-Circuit Oscillation Frequency	F_{LX}(Short)	V_{FB}=0.3V		150		KHz
Sync Frequency Range	F_{SYNC}		300		800	KHz
Input UVLO Threshold	VUVLO(Vth)	V_{IN} Rising		4		V
Under Voltage Lockout Threshold Hysteresis	VUVLO(Hys)			200		mV
$\overline{SHDN}$/S Input Low Voltage	$V_{\overline{SHDN}}$ (L)				0.4	V
$\overline{SHDN}$/S Input High Voltage	$V_{\overline{SHDN}}$ (H)		2.0			V
$\overline{SHDN}$/S Input Current	$I_{\overline{SHDN}}$	$V_{\overline{SHDN}}$=2V		2		μA
VCC Regulator	V_{CC}			4.5		V
Soft-Start Time	T_{SS}			600		μs
Thermal Shutdown Threshold (Note 2)	T_{SD}			170		°C

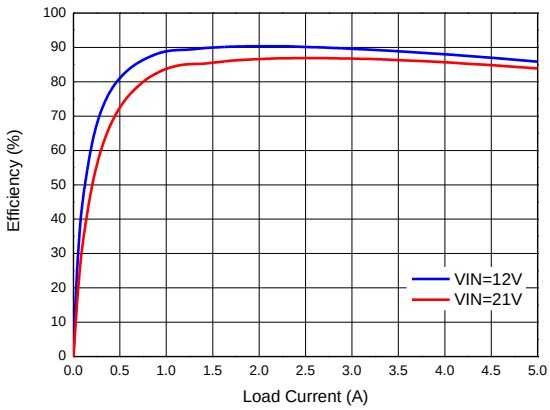
Note 2：Guarantee by design.

Typical Performance Curves

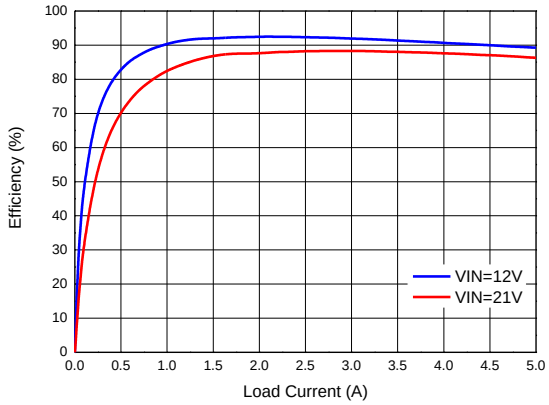
V_{IN}=12V, V_{OUT}=3.3V, C1=10µF x 2, C2=22µF x 2, L1=1.8µH, TA=+25°C, unless otherwise noted.



V_{OUT}=1.2V
Figure 5. Efficiency vs. Loading



V_{OUT}=3.3V
Figure 6. Efficiency vs. Loading



V_{OUT}=5V
Figure 7. Efficiency vs. Loading

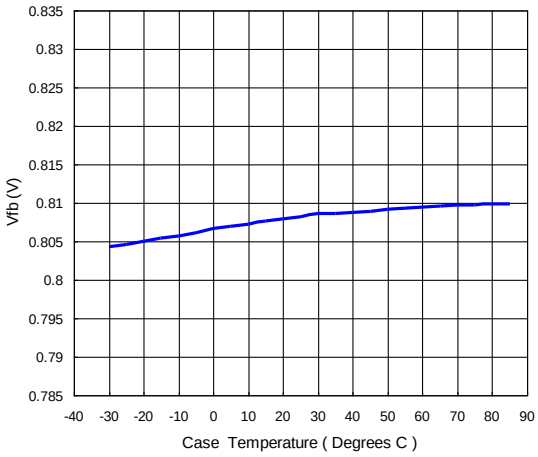


Figure 8. Feedback Voltage vs. Temperature

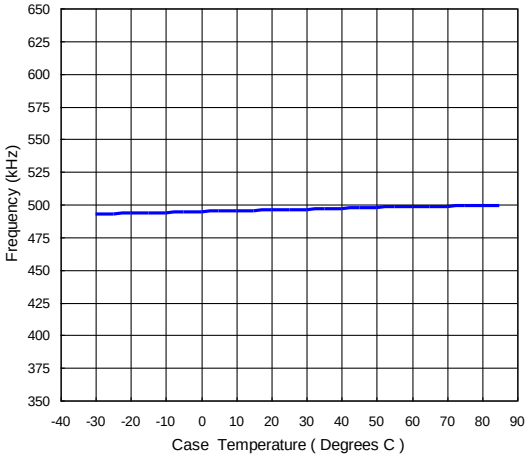


Figure 9. Frequency vs. Temperature

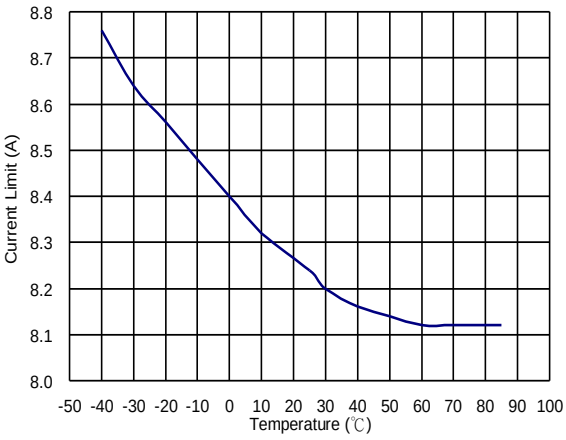


Figure 10. Current Limit vs. Temperature

Typical Performance Curves (Continued)

V_{IN}=12V, V_{OUT}=3.3V, C1=10μF x 2, C2=22μF x 2, L1=1.8μH, TA=+25°C, unless otherwise noted.

I_{OUT}=0A

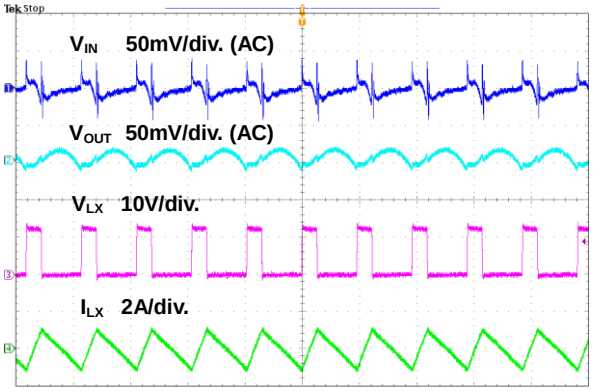


Figure 11. DC Ripple Waveform

I_{OUT}=5A

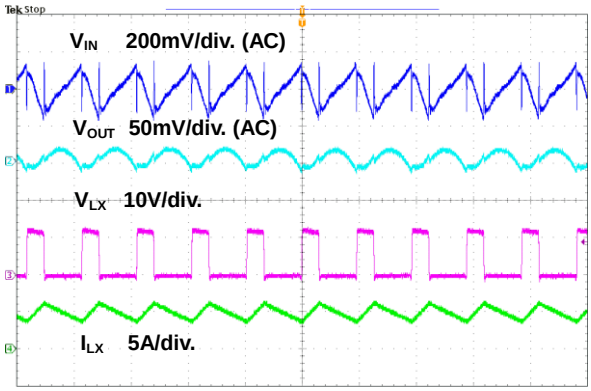


Figure 12. DC Ripple Waveform

I_{OUT}=0A

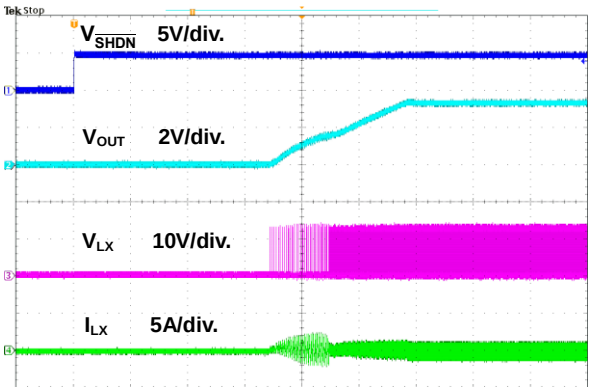


Figure 13. Startup Through $\overline{SHDN}$ Waveform

I_{OUT}=5A

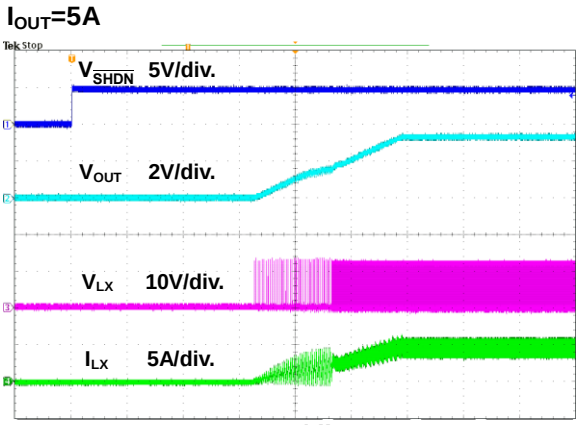


Figure 14. Startup Through $\overline{SHDN}$ Waveform

I_{OUT}=0A

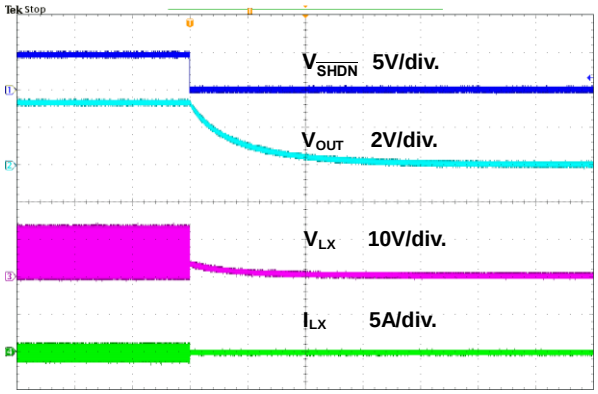


Figure 15. Shutdown Through $\overline{SHDN}$ Waveform

I_{OUT}=5A

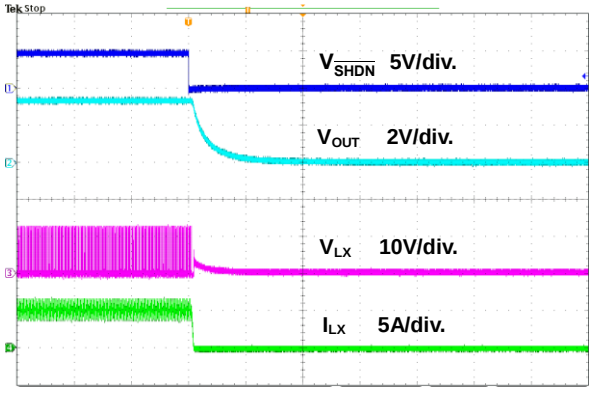


Figure 16. Shutdown Through $\overline{SHDN}$ Waveform

Typical Performance Curves (Continued)

V_{IN} = 12V, V_{OUT} = 3.3V, C1 =10µF x 2, C2 = 22µF x 2, L1 = 1.8µH, TA = +25°C, unless otherwise noted.

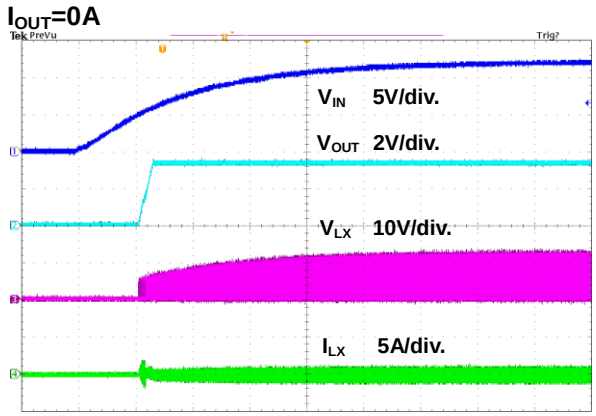


Figure 17. Startup Through VIN Waveform

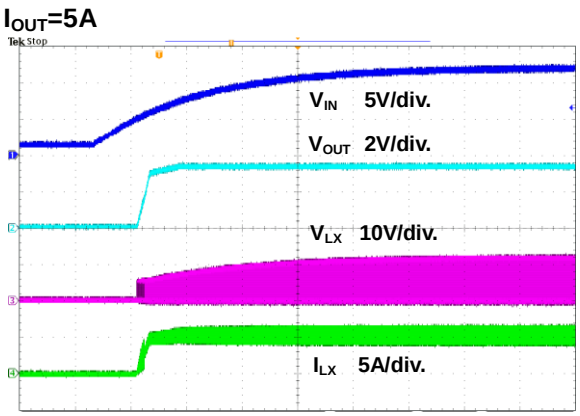


Figure 18. Startup Through VIN Waveform

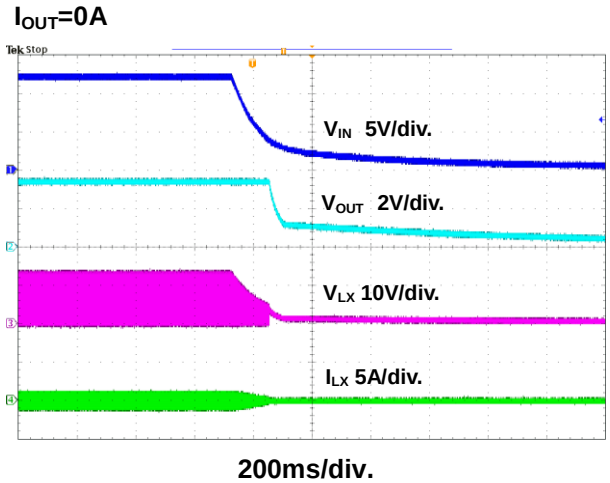


Figure 19. Shutdown Through VIN Waveform

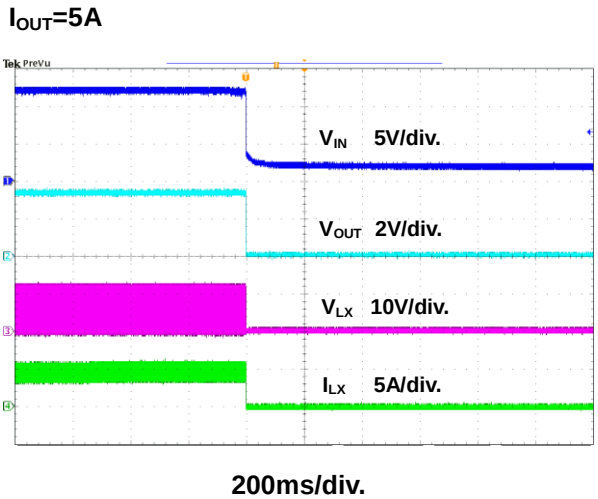


Figure 20. Shutdown Through VIN Waveform

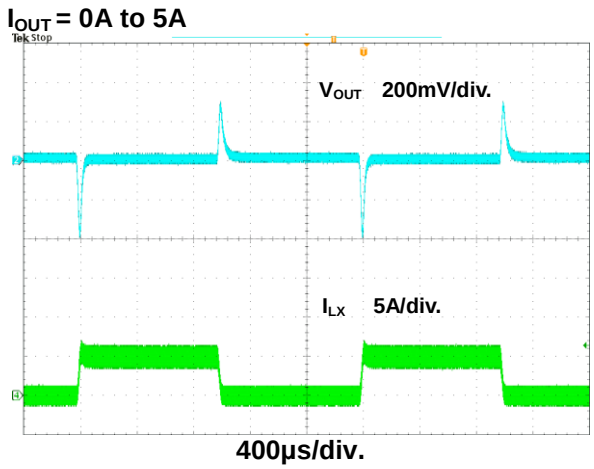


Figure 21. Load Transient Waveform

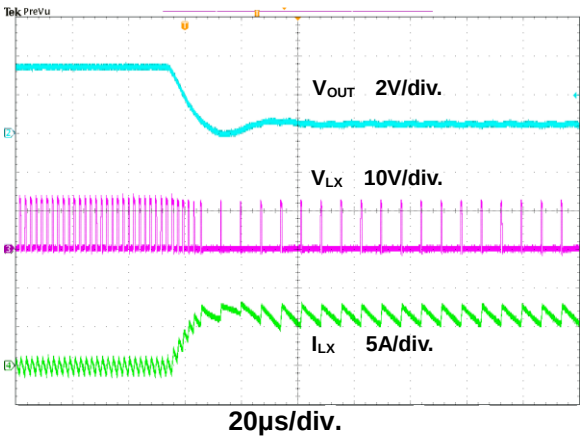


Figure 22. Short Protect Waveform

Function Description

Introduction

FR9809 is a constant-frequency current-mode step-down synchronous DC/DC converter. It regulates input voltage from 4.75V to 21V and provides 5A of continuous load current.

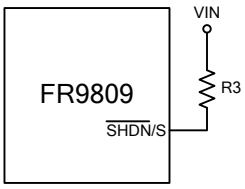
To achieve bias power supply, FR9809 contains an internal voltage regulator to support the internal circuits. For applications in which VIN is less than 4.5V, output decreases and a 0.1µF ceramic capacitor are required for decoupling. If VIN is greater than 4.5V, the output of the regulator will be in full regulation.

The error amplifier compares the FB voltage with the internal 0.805V reference. And the voltage of error amplifier output is compared to the switch current to control the RS flip-flop. At the beginning of each clock cycle, the high-side NMOS turns on when the oscillator sets the RS flip-flop, and turns off when current comparator resets the RS flip-flop. Then the low-side NMOS will turn on until the clock period ends.

Internal Soft-Start

The internal soft-start function is used to eliminate the output voltage overshooting during start-up. When the chip initiates, the internal reference voltage will rise slowly to 0.805V and the internal COMP signal will rise slowly to achieve output voltage. The soft-start time is approximate 600µs.

$\overline{\text{SHDN}}$/S



The FR9809 $\overline{\text{SHDN}}$/S pin provides digital control to turn on/turn off the regulator. For automatic start-up, tie $\overline{\text{SHDN}}$/S and VIN with a resister, as shown in the figure. The recommended value of R3 is 100KΩ. The FR9809 can be synchronized with an external clock from 300KHz to 800KHz by using the $\overline{\text{SHDN}}$/S pin.

Device Protection:

1. Input Under Voltage Lockout

When the power of FR9809 is on, the internal circuits will be held inactive until VIN exceeds the input UVLO threshold voltage. The regulator will be disabled when VIN falls below the input UVLO threshold voltage. The hysteretic of the UVLO comparator is 200mV.

2. Over Current Protection

The FR9809 OCP protection function is designed to sense the cycle-by-cycle over current limit signal to prevent device damaged due to short. When the inductor current peak value reaches the current limit threshold, the output voltage will start to drop until the FB voltage is less than 30% of the reference. FR9809 subsequently enters hiccup mode to periodically restart the part and exits the hiccup mode once the over current condition is lifted.

3. Over Temperature Protection

The FR9809 incorporates an over temperature protection circuit to protect itself from overheating. When the junction temperature exceeds the thermal shutdown threshold temperature, the regulator will shutdown. When the junction temperature is less than the recovery threshold temperature, the chip will re-enable.

Application Information

Output Voltage Setting

The output voltage V_{OUT} is set by using a resistive divider from the output to FB. The FB pin regulated voltage is 0.805V. Thus the output voltage is:

$$V_{OUT}=0.805\times\left(1+\frac{R1}{R2}\right)V$$

Table 1 lists recommended values of R1 and R2 for most used output voltage.

Table 1 Recommended Resistance Values

V_{OUT}	R1 (1%)	R2 (1%)
5V	30.9kΩ	5.76kΩ
3.3V	30.9kΩ	9.76kΩ
2.5V	4.99kΩ	2.32kΩ
1.8V	4.99kΩ	3.92kΩ
1.2V	4.99kΩ	10kΩ

Resistors R1 and R2 should be placed close to the FB pin to prevent stray pickup.

Input Capacitor Selection

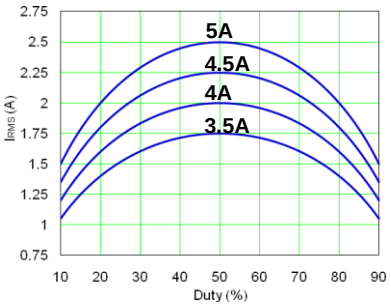
The use of the input capacitor is filtering the input voltage ripple and the MOSFETS switching spike voltage. Because the input current to the step-down converter is discontinuous, the input capacitor is required to supply the current to the converter to keep the DC input voltage. The capacitor voltage rating should be 1.25 to 1.5 times greater than the maximum input voltage. The input capacitor ripple current RMS value is calculated as:

$$I_{IN(RMS)}=I_{OUT}\times\sqrt{D\times(1-D)}$$

$$D=\frac{V_{OUT}}{V_{IN}}$$

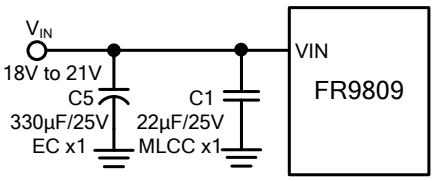
Where D is the duty cycle of the power MOSFET.

This function reaches the maximum value at D=0.5 and the equivalent RMS current is equal to $I_{OUT}/2$. The following diagram is the graphical representation of above equation.



A low ESR capacitor is required to keep the noise minimum. Ceramic capacitors are better, but tantalum or low ESR electrolytic capacitors may also suffice. When using tantalum or electrolytic capacitors, a 0.1μF ceramic capacitor should be placed as close to the IC as possible.

It is recommended that the input EC capacitor should be added for applications if the FR9809 suffers high spike input voltage (ex. hot plug test). It can eliminate the spike voltage and induce the IC damage from high input voltage stress (see Note1).



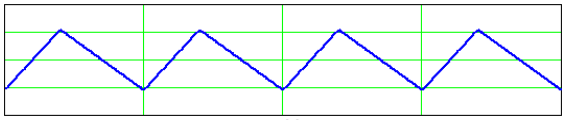
Output Capacitor Selection

The output capacitor is used to keep the DC output voltage and supply the load transient current. When operating in constant current mode, the output ripple is determined by four components:

$$V_{RIPPLE}(t)=V_{RIPPLE(C)}(t)+V_{RIPPLE(ESR)}(t)+V_{RIPPLE(ESL)}(t)+V_{NOISE}(t)$$

The following figures show the form of the ripple contributions.

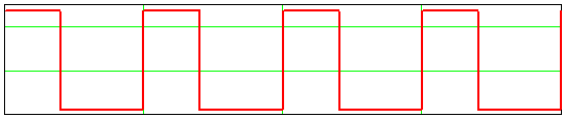
$V_{RIPPLE(ESR)}(t)$



(t)

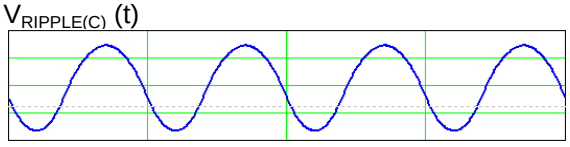
+

$V_{RIPPLE(ESL)}$ (t)



+ (t)

$V_{RIPPLE(C)}$ (t)

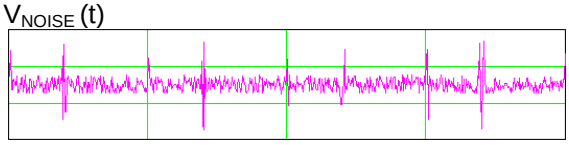


(t)

Application Information (Continued)

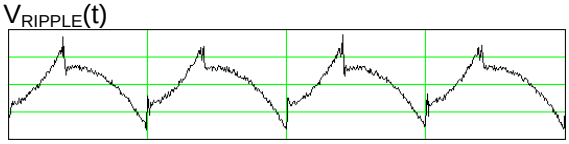
+

V_{NOISE} (t)



=

V_{RIPPLE}(t)



(t)

$$V_{RIPPLE(ESR,\ p\text{-}p)}=\frac{V_{OUT}}{F_{OSC}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times ESR$$

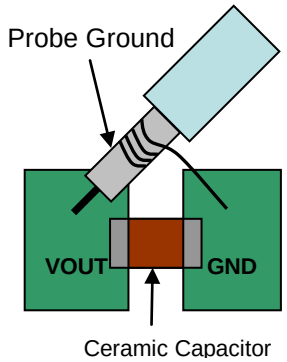
$$V_{RIPPLE(ESL,\ p\text{-}p)}=\frac{ESL}{L+ESL}\times V_{IN}$$

$$V_{RIPPLE(C,\ p\text{-}p)}=\frac{V_{OUT}}{8\times F_{OSC}^{2}\times L\times C_{OUT}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Where F_{OSC} is the switching frequency, L is the inductance value, V_{IN} is the input voltage, ESR is the equivalent series resistance value of the output capacitor, ESL is the equivalent series inductance value of the output capacitor and the C_{OUT} is the output capacitor.

Low ESR capacitors are preferred to use. Ceramic, tantalum or low ESR electrolytic capacitors can be used depending on the output ripple requirements. When using the ceramic capacitors, the ESL component is usually negligible.

It is important to use the proper method to eliminate high frequency noise when measuring the output ripple. The figure shows how to locate the probe across the capacitor when measuring output ripple. Remove the scope probe plastic jacket in order to expose the ground at the tip of the probe. It gives a very short connection from the probe ground to the capacitor and eliminates noise.

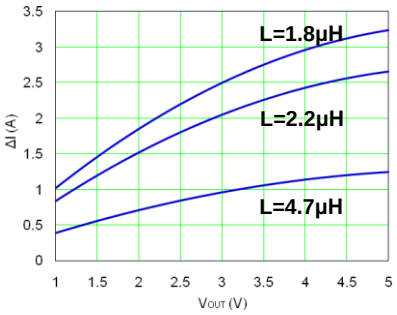


Inductor Selection

The output inductor is used for storing energy and filtering output ripple current. But the trade-off condition often happens between maximum energy storage and the physical size of the inductor. The first consideration for selecting the output inductor is to make sure that the inductance is large enough to keep the converter in the continuous current mode. That will lower ripple current and result in lower output ripple voltage. The ΔI_L is inductor peak-to-peak ripple current:

$$\Delta I_L=\frac{V_{OUT}}{F_{OSC}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

The following diagram is an example to graphical represent ΔI_L equation.



V_{IN}=12V, F_{OSC}=500KHz

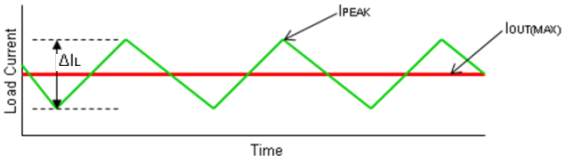
A good compromise value between size and efficiency is to set the peak-to-peak inductor ripple current ΔI_L equal to 30% of the maximum load current. But setting the peak-to-peak inductor ripple current ΔI_L between 20%~50% of the maximum load current is also acceptable. Then the inductance can be calculated with the following equation:

$$\Delta I_L=0.3\times I_{OUT(MAX)}$$

$$L=\frac{(V_{IN}-V_{OUT})\times V_{OUT}}{V_{IN}\times F_{OSC}\times\Delta I_L}$$

To guarantee sufficient output current, peak inductor current must be lower than the FR9809 high-side MOSFET current limit. The peak inductor current is shown as below:

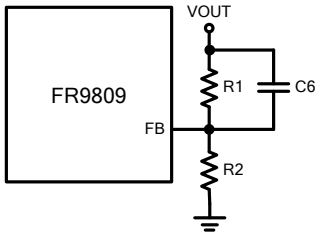
$$I_{PEAK}=I_{OUT(MAX)}+\frac{\Delta I_L}{2}$$



Application Information (Continued)

Feedforward Capacitor Selection

Internal compensation function allows users saving time in design and saving cost by reducing the number of external components. The use of a feedforward capacitor C6 in the feedback network is recommended to improve the transient response or higher phase margin.



For optimizing the feedforward capacitor, knowing the cross frequency is the first thing. The cross frequency (or the converter bandwidth) can be determined by using a network analyzer. When getting the cross frequency with no feedforward capacitor identified, the value of feedforward capacitor C6 can be calculated with the following equation:

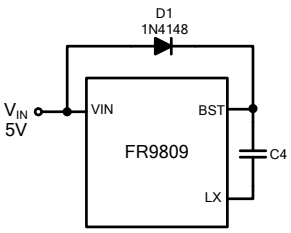
$$C6=\frac{1}{2\pi\times F_{CROSS}}\times\sqrt{\frac{1}{R1}\times\left(\frac{1}{R1}+\frac{1}{R2}\right)}$$

Where F_{CROSS} is the cross frequency.

To reduce transient ripple, the feedforward capacitor value can be increased to push the cross frequency to higher region. Although this can improve transient response, it also decreases phase margin and causes more ringing. In the other hand, if more phase margin is desired, the feedforward capacitor value can be decreased to push the cross frequency to lower region. In general, the feedforward capacitor range is between 10pF to 1nF.

External Diode Selection

For 5V input applications, it is recommended to add an external bootstrap diode. This helps improving efficiency. The bootstrap diode can be a low cost one such as 1N4148.



PCB Layout Recommendation

The device's performance and stability are dramatically affected by PCB layout. It is recommended to follow these general guidelines shown as below:

1. Place the input capacitors and output capacitors as close to the device as possible. The traces which connect to these capacitors should be as short and wide as possible to minimize parasitic inductance and resistance.
2. Place feedback resistors close to the FB pin.
3. Keep the sensitive signal (FB) away from the switching signal (LX).
4. The exposed pad of the package should be soldered to an equivalent area of metal on the PCB. This area should connect to the GND plane and have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers. The GND plane area connecting to the exposed pad should be maximized to improve thermal performance.
5. Multi-layer PCB design is recommended.

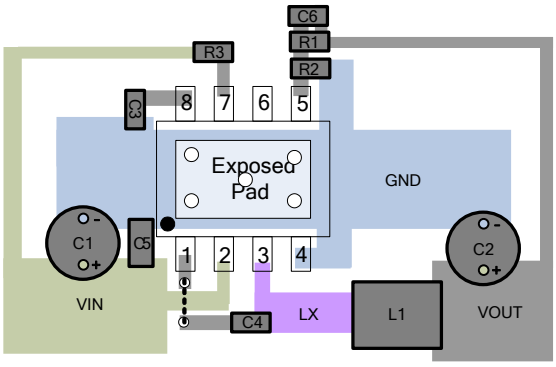
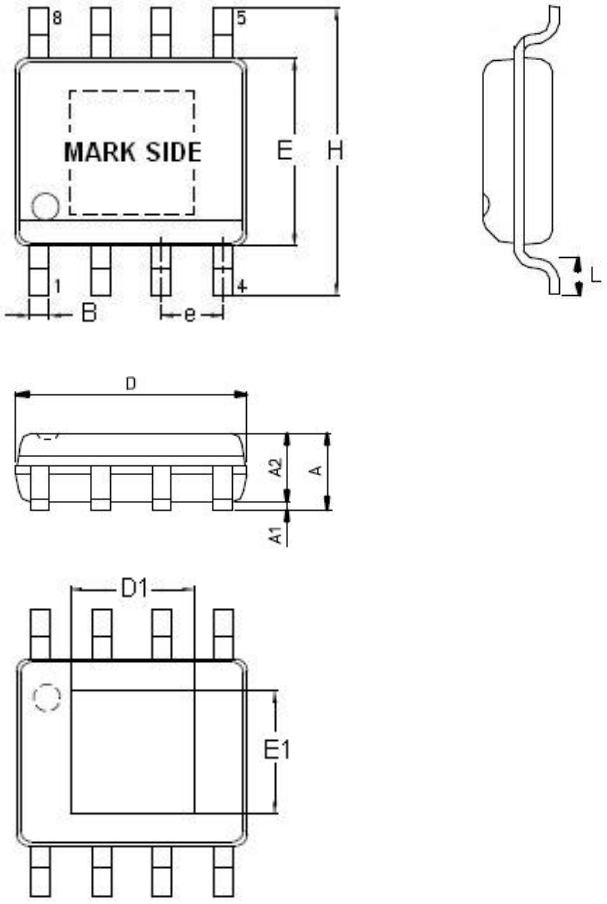


Figure 23. FR9809 SOP-8 (Exposed Pad) package C_{IN}/C_{OUT} with EC capacitors Recommended PCB Layout Diagram

Outline Information

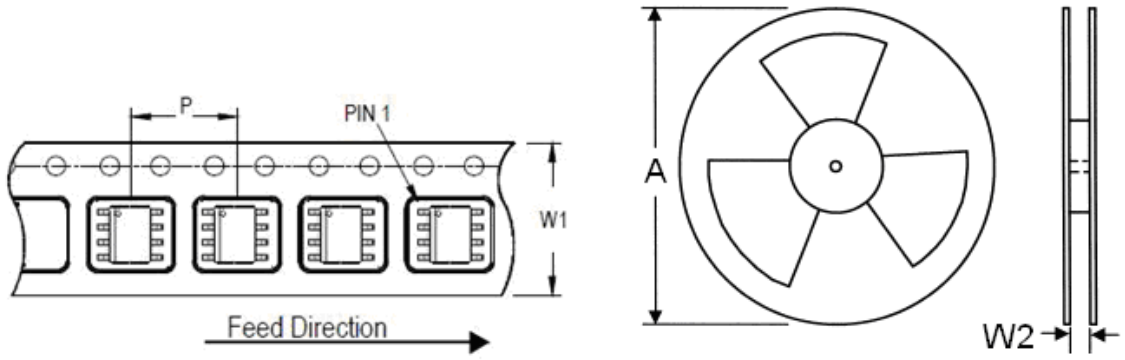
SOP-8 (Exposed Pad) Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	1.25	1.70
A1	0.00	0.15
A2	1.25	1.55
B	0.31	0.51
D	4.80	5.00
D1	3.04	3.50
E	3.80	4.00
E1	2.15	2.41
e	1.20	1.34
H	5.80	6.20
L	0.40	1.27

Note：Followed From JEDEC MO-012-E.

Carrier Dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
12	8	13	330	12.4	400~1000	2,500

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