

# FQP18N50V2/FQPF18N50V2

## 500V N-Channel MOSFET

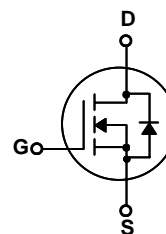
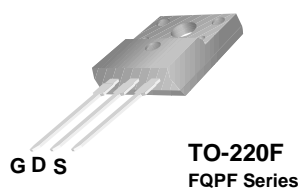
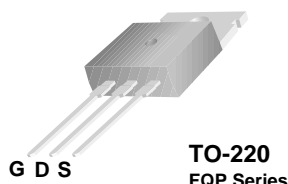
### General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies, active power factor correction, electronic lamp ballast based on half bridge topology.

### Features

- 18A, 500V,  $R_{DS(on)} = 0.265\Omega @ V_{GS} = 10V$
- Low gate charge ( typical 42 nC)
- Low Crss ( typical 11 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



### Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter	FQP18N50V2	FQPF18N50V2	Units
V <sub>DSS</sub>	Drain-Source Voltage	500		V
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C) - Continuous (T <sub>C</sub> = 100°C)	18	18	A
		12.1	12.1	A
I <sub>DM</sub>	Drain Current - Pulsed (Note 1)	72	72	A
V <sub>GSS</sub>	Gate-Source Voltage	± 30		V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)	330		mJ
I <sub>AR</sub>	Avalanche Current (Note 1)	18		A
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)	25		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5		V/ns
P <sub>D</sub>	Power Dissipation (T <sub>C</sub> = 25°C) - Derate above 25°C	208	69	W
		1.67	0.55	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +150		°C
T <sub>L</sub>	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		°C

### Thermal Characteristics

Symbol	Parameter	FQP18N50V2	FQPF18N50V2	Units
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	0.6	1.8	°C/W
R <sub>θCS</sub>	Thermal Resistance, Case-to-Sink	0.5	--	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	62.5	62.5	°C/W

## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	500	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.5	--	V/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 400\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 9\text{ A}$	--	0.225	0.265	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 9\text{ A}$ (Note 4)	--	16	--	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	2530	3290	pF
$C_{oss}$	Output Capacitance		--	300	390	pF
$C_{riss}$	Reverse Transfer Capacitance		--	11	14.3	pF
$C_{oss}$	Output Capacitance	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	76	--	pF
$C_{oss\text{ eff.}}$	Effective Output Capacitance	$V_{DS} = 0\text{V to } 400\text{ V}, V_{GS} = 0\text{ V}$	--	150	--	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\text{ V}, I_D = 18\text{ A},$ $R_G = 25\ \Omega$	--	40	90	ns
$t_r$	Turn-On Rise Time		--	150	310	ns
$t_{d(off)}$	Turn-Off Delay Time		--	95	200	ns
$t_f$	Turn-Off Fall Time		(Note 4, 5)	--	110	230
$Q_g$	Total Gate Charge	$V_{DS} = 400\text{ V}, I_D = 18\text{ A},$ $V_{GS} = 10\text{ V}$	--	42	55	nC
$Q_{gs}$	Gate-Source Charge		--	12	--	nC
$Q_{gd}$	Gate-Drain Charge		(Note 4, 5)	--	14	--

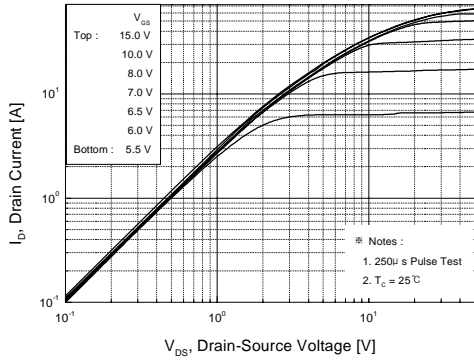
### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	18	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	72	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 18\text{ A}$	--	--	1.4	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 18\text{ A},$ $di_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4)	--	420	--	ns
$Q_{rr}$	Reverse Recovery Charge		--	5.4	--	$\mu\text{C}$

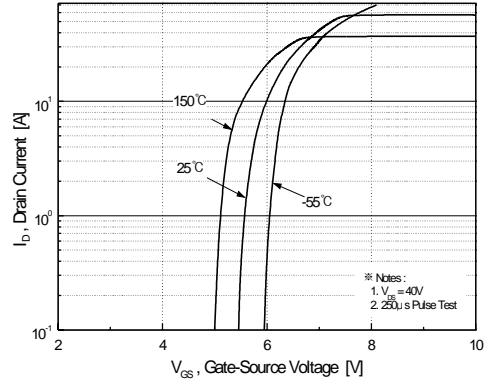
#### Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L = 1.83\text{mH}, I_{AS} = 18\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 18\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width  $\leq 300\ \mu\text{s}$ , Duty cycle  $\leq 2\%$
5. Essentially independent of operating temperature

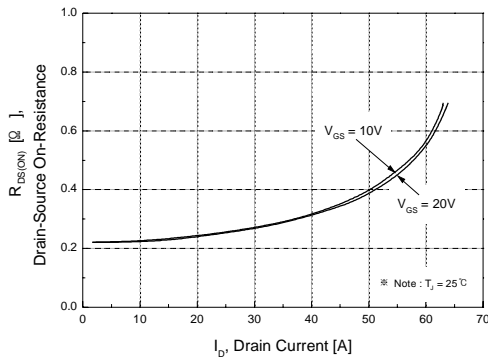
## Typical Characteristics



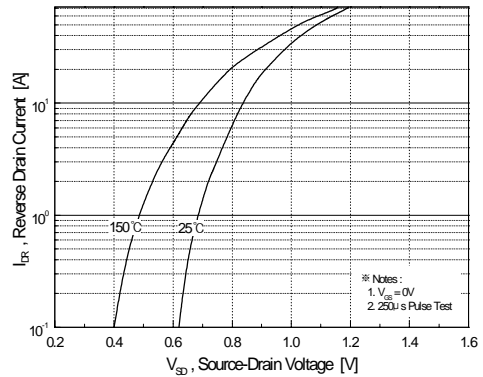
**Figure 1. On-Region Characteristics**



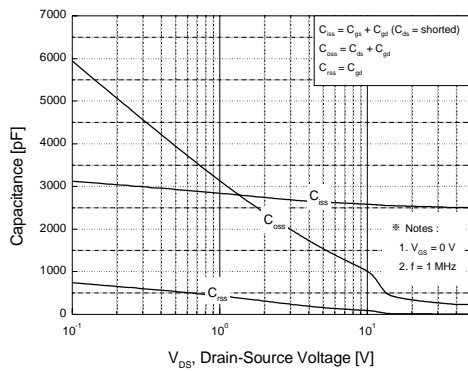
**Figure 2. Transfer Characteristics**



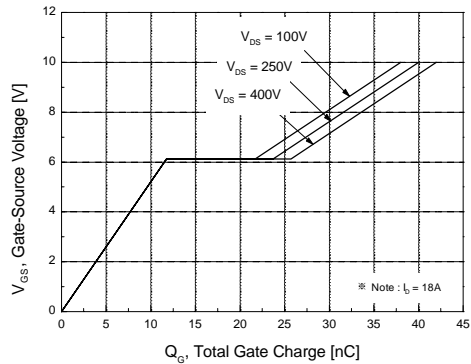
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**

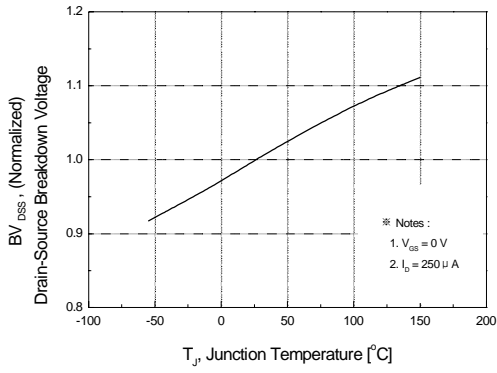


**Figure 5. Capacitance Characteristics**

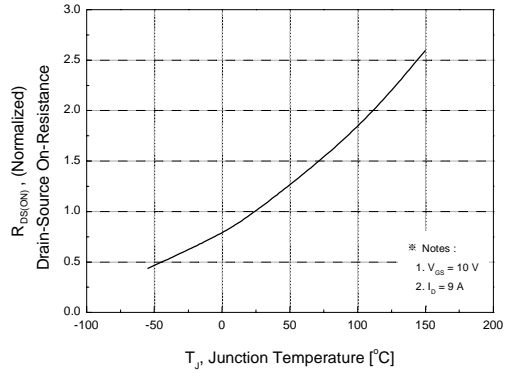


**Figure 6. Gate Charge Characteristics**

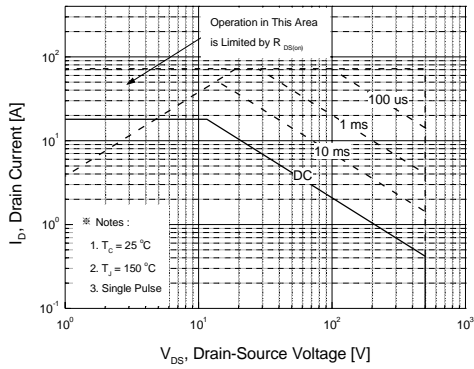
**Typical Characteristics** (Continued)



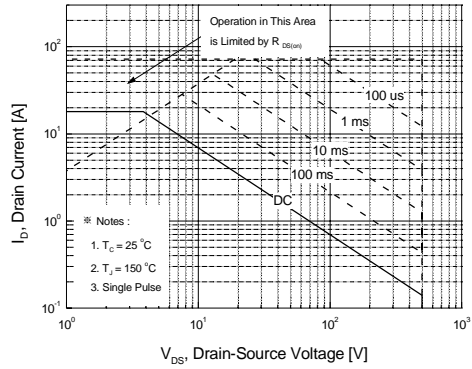
**Figure 7. Breakdown Voltage Variation vs. Temperature**



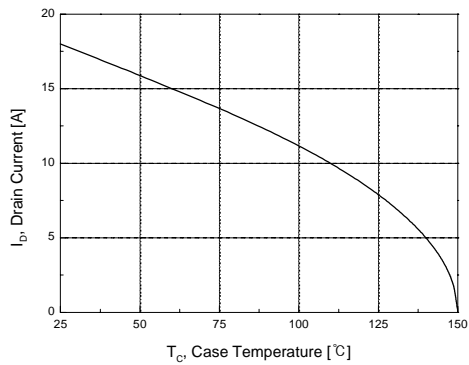
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9-1. Maximum Safe Operating Area for FQP18N50V2**



**Figure 9-2. Maximum Safe Operating Area for FQPF18N50V2**



**Figure 10. Maximum Drain Current vs. Case Temperature**

Typical Characteristics (Continued)

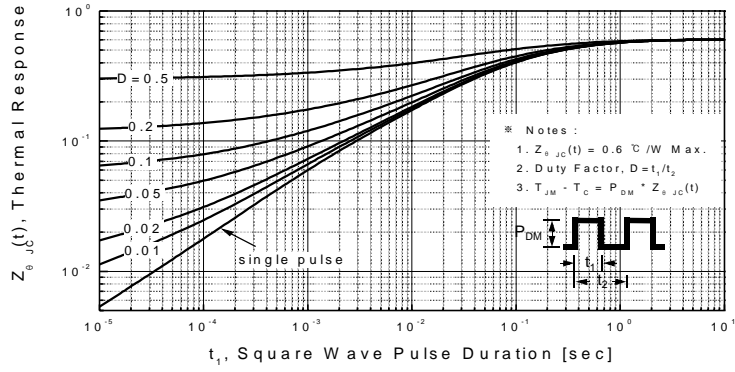


Figure 11-1. Transient Thermal Response Curve for FQP18N50V2

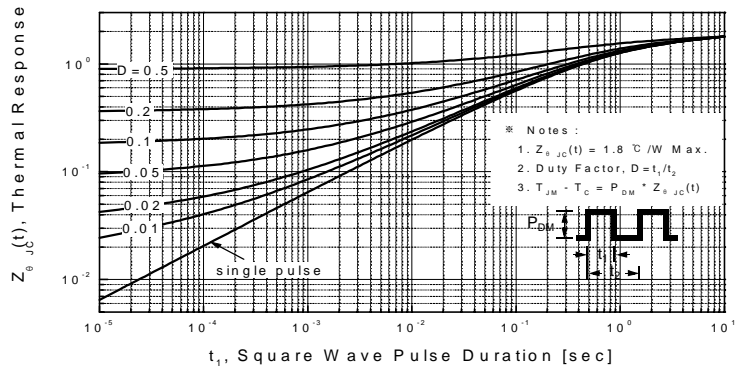


Figure 11-2. Transient Thermal Response Curve for FQPF18N50V2

**Gate Charge Test Circuit & Waveform**



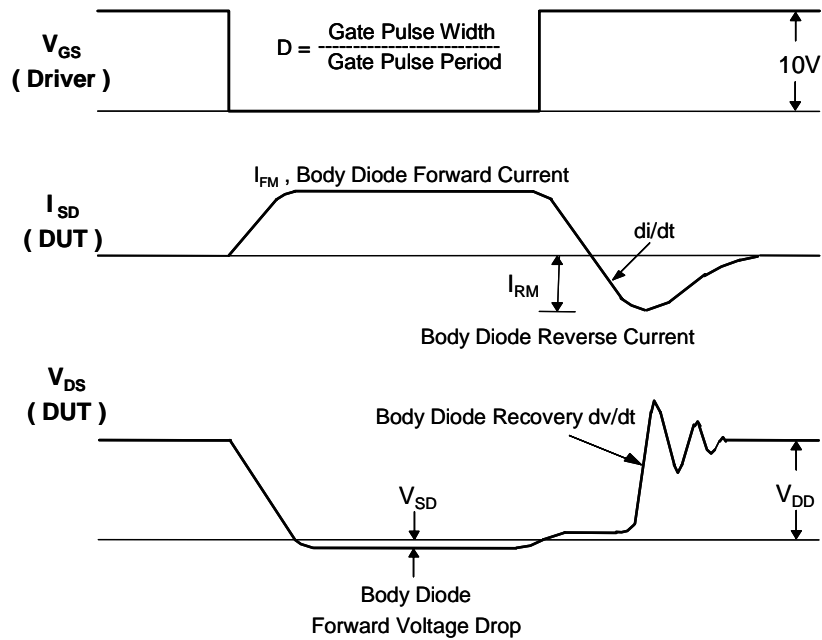
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**



Peak Diode Recovery dv/dt Test Circuit & Waveforms









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