ANALOG DEVICES

Single Supply, Rail-to-Rail Low Power, FET-Input Op Amp

AD824

FEATURES

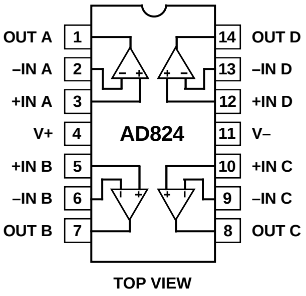
- Single Supply Operation: 3 V to 30 V
- Very Low Input Bias Current: 2 pA
- Wide Input Voltage Range
- Rail-to-Rail Output Swing
- Low Supply Current: 500 μA/Amp
- Wide Bandwidth: 2 MHz
- Slew Rate: 2 V/μs
- No Phase Reversal

APPLICATIONS

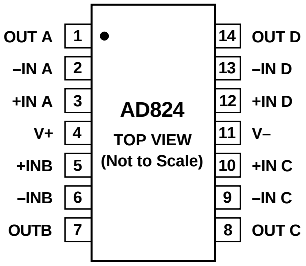
- Photo Diode Preamplifier
- Battery Powered Instrumentation
- Power Supply Control and Protection
- Medical Instrumentation
- Remote Sensors
- Low Voltage Strain Gage Amplifiers
- DAC Output Amplifier

PIN CONFIGURATIONS

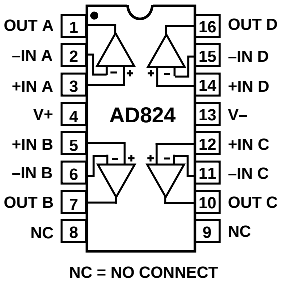
14-Lead Epoxy DIP
(N Suffix)



14-Lead Epoxy SO
(R Suffix)



16-Lead Epoxy SO
(R Suffix)



GENERAL DESCRIPTION

The AD824 is a quad, FET input, single supply amplifier, featuring rail-to-rail outputs. The combination of FET inputs and rail-to-rail outputs makes the AD824 useful in a wide variety of low voltage applications where low input current is a primary consideration.

The AD824 is guaranteed to operate from a 3 V single supply up to ±15 volt dual supplies.

Fabricated on ADI's complementary bipolar process, the AD824 has a unique input stage that allows the input voltage to safely extend beyond the negative supply and to the positive supply without any phase inversion or latchup. The output voltage swings to within 15 millivolts of the supplies. Capacitive loads to 350 pF can be handled without oscillation.

The FET input combined with laser trimming provides an input that has extremely low bias currents with guaranteed offsets below 300 μV. This enables high accuracy designs even with high source impedances. Precision is combined with low noise, making the AD824 ideal for use in battery powered medical equipment.

Applications for the AD824 include portable medical equipment, photo diode preamplifiers and high impedance transducer amplifiers.

The ability of the output to swing rail-to-rail enables designers to build multistage filters in single supply systems and maintain high signal-to-noise ratios.

The AD824 is specified over the extended industrial (–40°C to +85°C) temperature range and is available in 14-pin DIP and narrow 14-pin and 16-pin SO packages.

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AD824–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (@ V_S = +5.0 V, V_{CM} = 0 V, V_{OUT} = 0.2 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage AD824A	V_{OS}			0.1	1.0	mV
		T_{MIN} to T_{MAX}			1.5	mV
Offset Voltage AD824B	V_{OS}				300	µV
		T_{MIN} to T_{MAX}			900	µV
Input Bias Current	I_B			2	12	pA
		T_{MIN} to T_{MAX}		300	4000	pA
Input Offset Current	I_{OS}			2	10	pA
		T_{MIN} to T_{MAX}		300		pA
Input Voltage Range			–0.2		3.0	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2 V	66	80		dB
		V_{CM} = 0 V to 3 V	60	74		dB
		T_{MIN} to T_{MAX}	60			dB
Input Impedance				$10^{13}\|\|3.3$		Ω||pF
Large Signal Voltage Gain	A_{VO}	V_O = 0.2 V to 4.0 V				
		R_L = 2 kΩ	20	40		V/mV
		R_L = 10 kΩ	50	100		V/mV
		R_L = 100 kΩ	250	1000		V/mV
		T_{MIN} to T_{MAX}, R_L = 100 kΩ	180	400		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_{SOURCE} = 20 µA	4.975	4.988		V
		T_{MIN} to T_{MAX}	4.97	4.985		V
		I_{SOURCE} = 2.5 mA	4.80	4.85		V
		T_{MIN} to T_{MAX}	4.75	4.82		V
Output Voltage Low	V_{OL}	I_{SINK} = 20 µA		15	25	mV
		T_{MIN} to T_{MAX}		20	30	mV
		I_{SINK} = 2.5 mA		120	150	mV
		T_{MIN} to T_{MAX}		140	200	mV
Short Circuit Limit	I_{SC}	Sink/Source		±12		mA
		T_{MIN} to T_{MAX}		±10		mA
Open-Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		100		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 12 V	70	80		dB
		T_{MIN} to T_{MAX}	66			dB
Supply Current/Amplifier	I_{SY}	T_{MIN} to T_{MAX}		500	600	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, A_V = 1		2		V/µs
Full-Power Bandwidth	BW_P	1% Distortion, V_O = 4 V p-p		150		kHz
Settling Time	t_S	V_{OUT} = 0.2 V to 4.5 V, to 0.01%		2.5		µs
Gain Bandwidth Product	GBP			2		MHz
Phase Margin	ϕo	No Load		50		Degrees
Channel Separation	CS	f = 1 kHz, R_L = 2 kΩ		–123		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		16		nV/$\sqrt{Hz}$
Current Noise Density	i_n	f = 1 kHz		0.8		fA/$\sqrt{Hz}$
Total Harmonic Distortion	THD	f = 10 kHz, R_L = 0, A_V = +1		0.005		%

ELECTRICAL SPECIFICATIONS (@ V_S = ±15.0 V, V_{OUT} = 0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage AD824A	V_{OS}			0.5	2.5	mV
		T_{MIN} to T_{MAX}		0.6	4.0	mV
Offset Voltage AD824B	V_{OS}			0.5	1.5	mV
		T_{MIN} to T_{MAX}		0.6	2.5	mV
Input Bias Current	I_B	V_{CM} = 0 V		4	35	pA
		T_{MIN} to T_{MAX}		500	4000	pA
Input Bias Current	I_B	V_{CM} = –10 V		25		pA
Input Offset Current	I_{OS}			3	20	pA
		T_{MIN} to T_{MAX}		500		pA
Input Voltage Range			–15		13	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = –15 V to 13 V	70	80		dB
		T_{MIN} to T_{MAX}	66			dB
Input Impedance				$10^{13}\parallel 3.3$		$\Omega\parallel$pF
Large Signal Voltage Gain	A_{VO}	Vo = –10 V to +10 V;				
		R_L = 2 kΩ	12	50		V/mV
		R_L = 10 kΩ	50	200		V/mV
		R_L = 100 kΩ	300	2000		V/mV
		T_{MIN} to $T_{MAX,}$ R_L = 100 kΩ	200	1000		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_{SOURCE} = 20 µA	14.975	14.988		V
		T_{MIN} to T_{MAX}	14.970	14.985		V
		I_{SOURCE} = 2.5 mA	14.80	14.85		V
		T_{MIN} to T_{MAX}	14.75	14.82		V
Output Voltage Low	V_{OL}	I_{SINK} = 20 µA		–14.985	–14.975	V
		T_{MIN} to T_{MAX}		–14.98	–14.97	V
		I_{SINK} = 2.5 mA		–14.88	–14.85	V
		T_{MIN} to T_{MAX}		–14.86	–14.8	V
Short Circuit Limit	I_{SC}	Sink/Source, T_{MIN} to T_{MAX}	±8	±20		mA
Open-Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		100		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 15 V	70	80		dB
		T_{MIN} to T_{MAX}	68			dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		560	625	µA
		T_{MIN} to T_{MAX}			675	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, A_V = 1		2		V/µs
Full-Power Bandwidth	BW_P	1% Distortion, V_O = 20 V p-p		33		kHz
Settling Time	t_S	V_{OUT} = 0 V to 10 V, to 0.01%		6		µs
Gain Bandwidth Product	GBP			2		MHz
Phase Margin	ϕo			50		Degrees
Channel Separation	CS	f = 1 kHz, R_L =2 kΩ		–123		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		16		nV/$\sqrt{Hz}$
Current Noise Density	i_n	f = 1 kHz		1.1		fA/$\sqrt{Hz}$
Total Harmonic Distortion	THD	f =10 kHz, V_O = 3 V rms,				
		R_L = 10 kΩ		0.005		%

AD824–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (@ V_S = +3.0 V, V_{CM} = 0 V, V_{OUT} = 0.2 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage AD824A -3 V	V_{OS}			0.2	1.0	mV
		T_{MIN} to T_{MAX}			1.5	mV
Input Bias Current	I_B			2	12	pA
		T_{MIN} to T_{MAX}		250	4000	pA
Input Offset Current	I_{OS}			2	10	pA
		T_{MIN} to T_{MAX}		250		pA
Input Voltage Range			0		1	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 1 V	58	74		dB
		T_{MIN} to T_{MAX}	56			dB
Input Impedance				$10^{13}\|\|3.3$		Ω‖pF
Large Signal Voltage Gain	A_{VO}	V_O = 0.2 V to 2.0 V				
		R_L = 2 kΩ	10	20		V/mV
		R_L = 10 kΩ	30	65		V/mV
		R_L = 100 kΩ	180	500		V/mV
		T_{MIN} to $T_{MAX,}$ R_L = 100 kΩ	90	250		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_{SOURCE} = 20 µA	2.975	2.988		V
		T_{MIN} to T_{MAX}	2.97	2.985		V
		I_{SOURCE} = 2.5 mA	2.8	2.85		V
		T_{MIN} to T_{MAX}	2.75	2.82		V
Output Voltage Low	V_{OL}	I_{SINK} = 20 µA		15	25	mV
		T_{MIN} to T_{MAX}		20	30	mV
		I_{SINK} = 2.5 mA		120	150	mV
		T_{MIN} to T_{MAX}		140	200	mV
Short Circuit Limit	I_{SC}	Sink/Source		±8		mA
Short Circuit Limit	I_{SC}	Sink/Source, T_{MIN} to T_{MAX}		±6		mA
Open-Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		100		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 12 V,	70			dB
		T_{MIN} to T_{MAX}	66			dB
Supply Current/Amplifier	I_{SY}	V_O = 0.2 V, T_{MIN} to T_{MAX}		500	600	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L =10 kΩ, A_V = 1		2		V/µs
Full-Power Bandwidth	BW_P	1% Distortion, V_O = 2 V p-p		300		kHz
Settling Time	t_S	V_{OUT} = 0.2 V to 2.5 V, to 0.01%		2		µs
Gain Bandwidth Product	GBP			2		MHz
Phase Margin	ϕo			50		Degrees
Channel Separation	CS	f = 1 kHz, R_L = 2 kΩ		–123		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		16		$nV/\sqrt{Hz}$
Current Noise Density	i_n			0.8		$fA/\sqrt{Hz}$
Total Harmonic Distortion	THD	f = 10 kHz, R_L = 0, A_V = +1		0.01		%

WAFER TEST LIMITS (@ V_S = +5.0 V, V_{CM} = 0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}		1.0	mV max
Input Bias Current	I_B		12	pA max
Input Offset Current	I_{OS}		20	pA
Input Voltage Range	V_{CM}		–0.2 to 3.0	V min
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2 V	66	dB min
Power Supply Rejection Ratio	PSRR	V = + 2.7 V to +12 V	70	µV/V
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	15	V/mV min
Output Voltage High	V_{OH}	I_{SOURCE} = 20 µA	4.975	V min
Output Voltage Low	V_{OL}	I_{SINK} = 20 µA	25	mV max
Supply Current/Amplifier	I_{SY}	V_O = 0 V, R_L = ∞	600	µA max

NOTE
Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18 V
Input Voltage	$-V_S$ – 0.2 V to $+V_S$
Differential Input Voltage	±30 V
Output Short Circuit Duration to GND	Indefinite
Storage Temperature Range	
N, R Package	–65°C to +150°C
Operating Temperature Range	
AD824A, B	–40°C to +85°C
Junction Temperature Range	
N, R Package	–65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	+300°C

Package Type	θ_{JA}[2]	θ_{JC}	Units
14-Pin Plastic DIP (N)	76	33	°C/W
14-Pin SOIC (R)	120	36	°C/W
16-Pin SOIC (R)	92	27	°C/W

NOTES

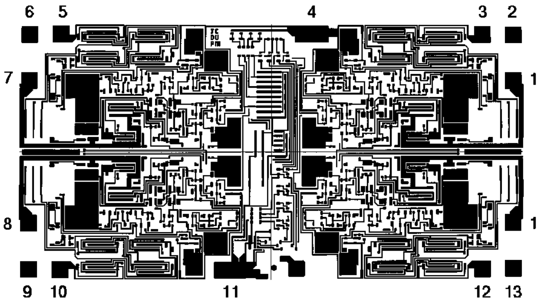
[1] Absolute maximum ratings apply to both DICE and packaged parts unless otherwise noted.

[2] θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

ORDERING GUIDE

Model	Temperature Range	Package Option
AD824AN	–40°C to +85°C	14-Pin Plastic DIP
AD824BN	–40°C to +85°C	14-Pin Plastic DIP
AD824AR	–40°C to +85°C	14-Pin SOIC
AD824AR-3V	–40°C to +85°C	14-Pin SOIC
AD824AN-3V	–40°C to +85°C	14-Pin Plastic DIP
AD824AR-14	–40°C to +85°C	14-Pin SOIC
AD824AR-14-3V	–40°C to +85°C	14-Pin SOIC
AD824AR-16	–40°C to +85°C	16-Pin SOIC
AD824AChips	+25°C	DICE

DICE CHARACTERISTICS



AD824 Die Size 0.70 X 0.130 inch, 9,100 sq. mils. Substrate (Die Backside) Is Connected to V+. Transistor Count, 143.

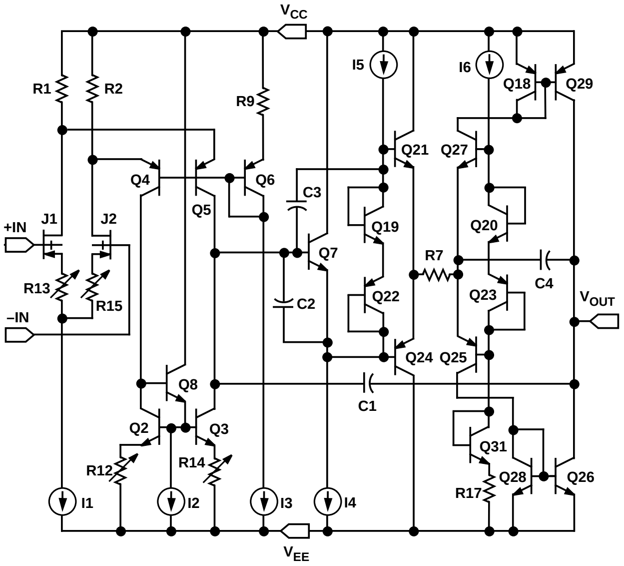


Figure 1. Simplified Schematic of 1/4 AD824

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD824 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD824–Typical Characteristics

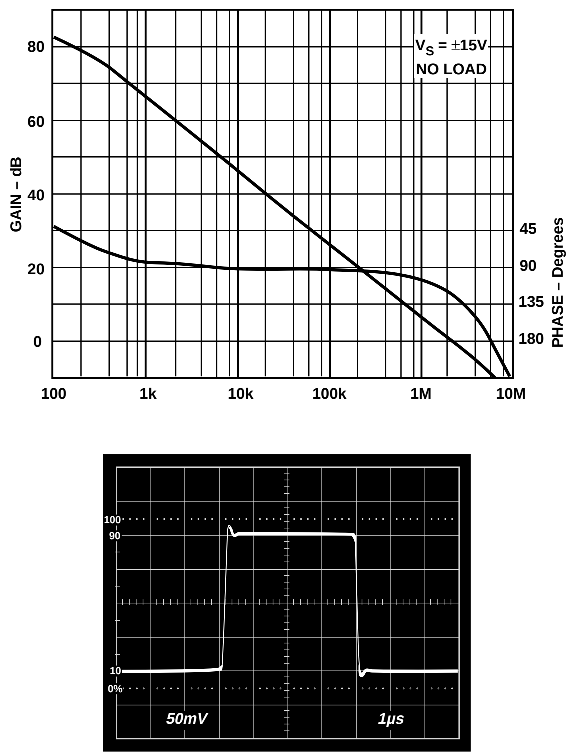


Figure 2. Open-Loop Gain/Phase and Small Signal Response, $V_S = \pm 15$ V, No Load

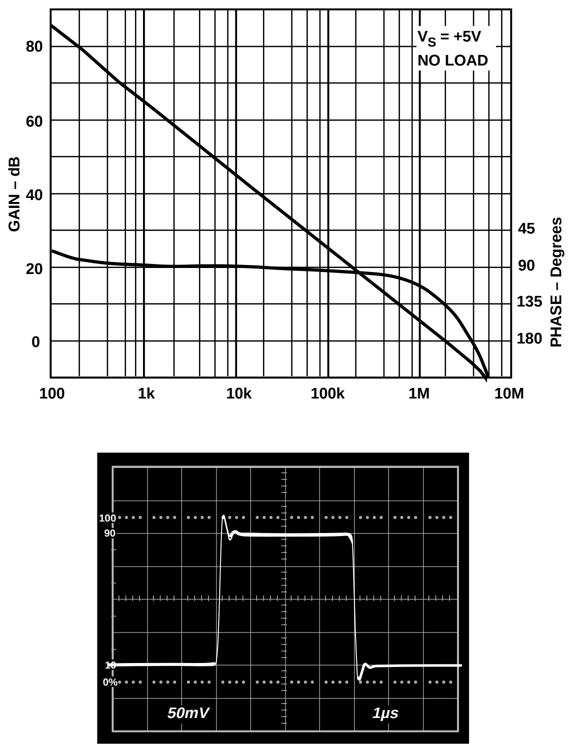


Figure 4. Open-Loop Gain/Phase and Small Signal Response, $V_S = +5$ V, No Load

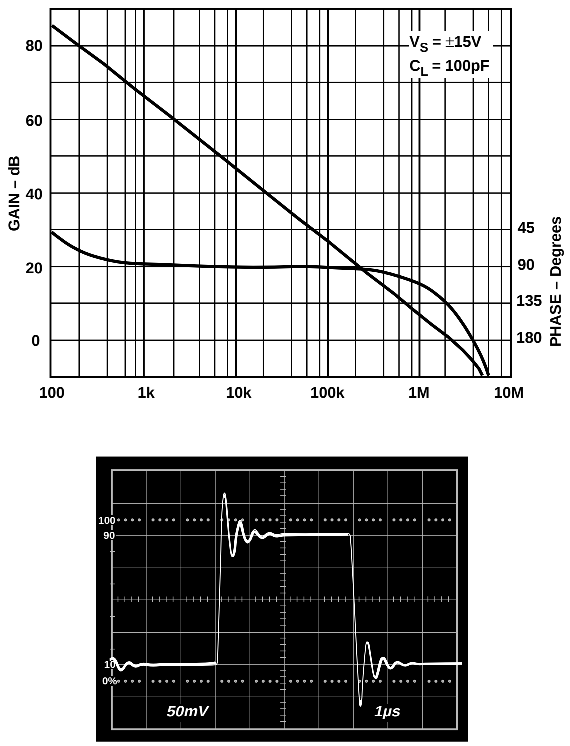


Figure 3. Open-Loop Gain/Phase and Small Signal Response, $V_S = \pm 15$ V, C_L = 100 pF

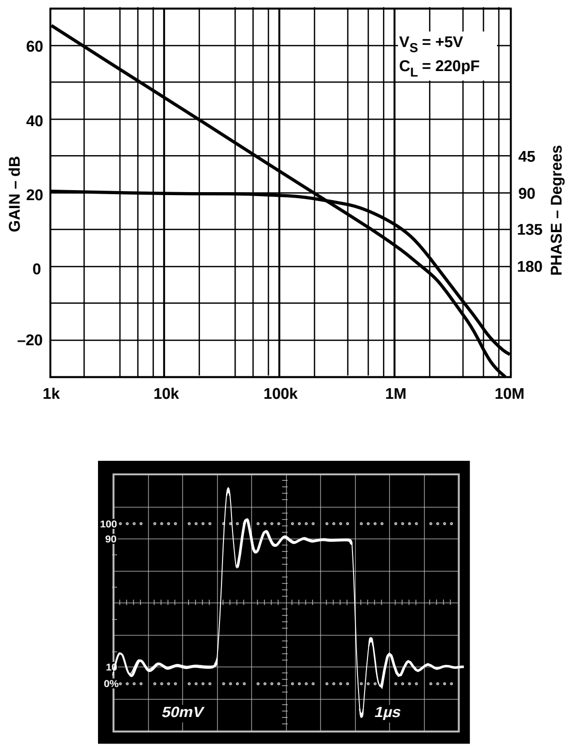


Figure 5. Open-Loop Gain/Phase and Small Signal Response, $V_S = +5$ V, C_L = 220 pF

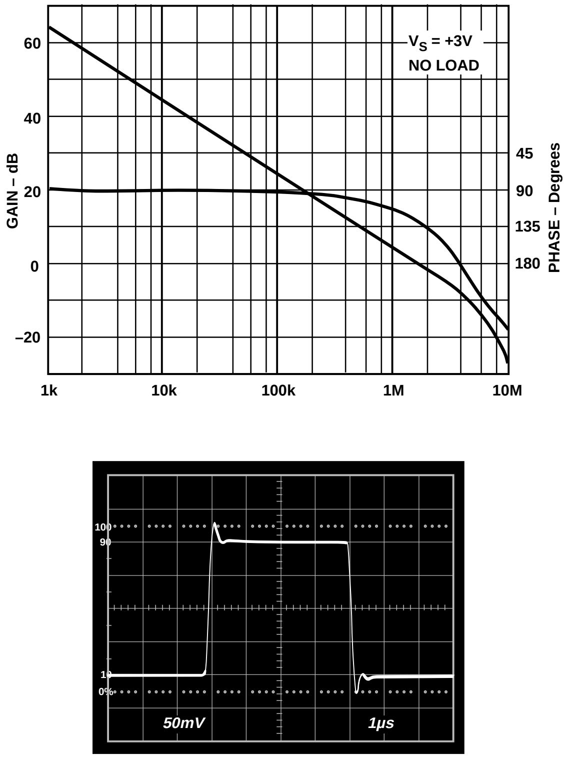


Figure 6. Open-Loop Gain/Phase and Small Signal Response, V_S = +3 V, No Load

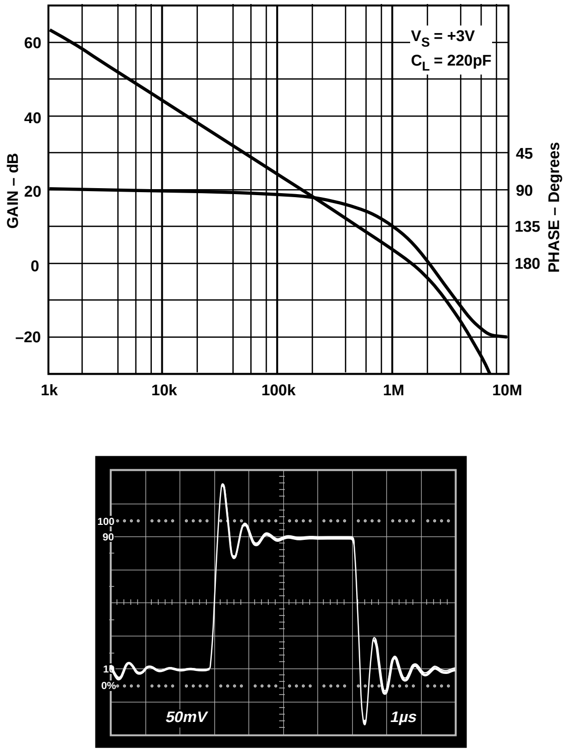


Figure 7. Open-Loop Gain/Phase and Small Signal Response, V_S = +3 V, C_L = 220 pF

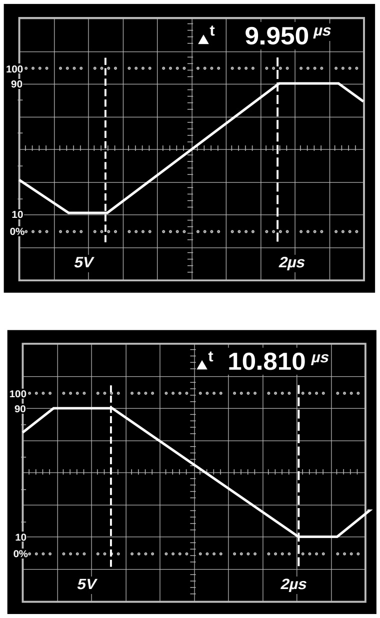


Figure 8. Slew Rate, R_L = 10k

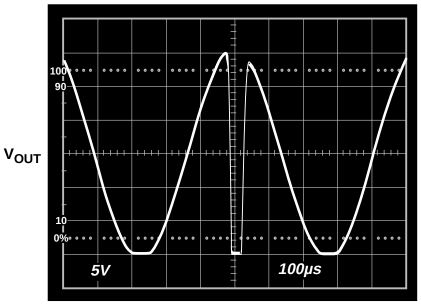


Figure 9. Phase Reversal with Inputs Exceeding Supply by 1 Volt

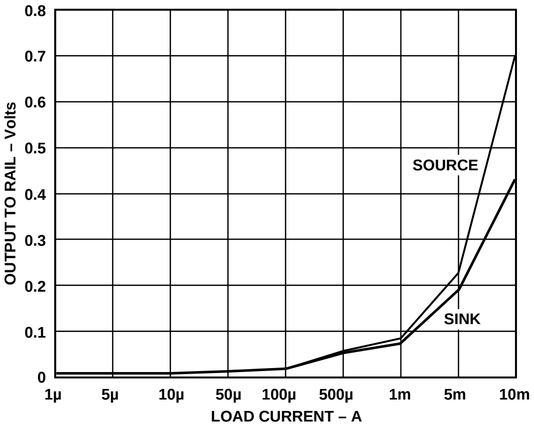


Figure 10. Output Voltage to Supply Rail vs. Sink and Source Load Currents

AD824–Typical Characteristics

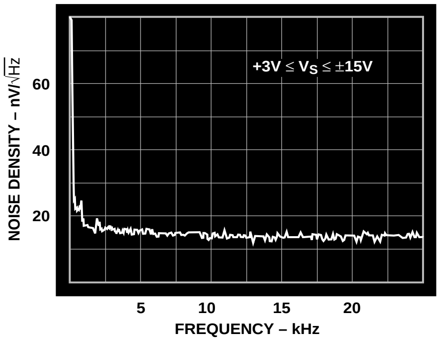


Figure 11. Voltage Noise Density

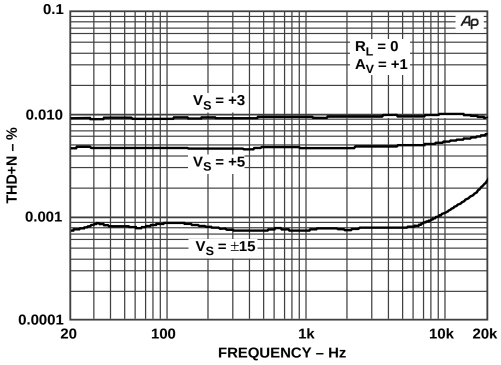


Figure 12. Total Harmonic Distortion

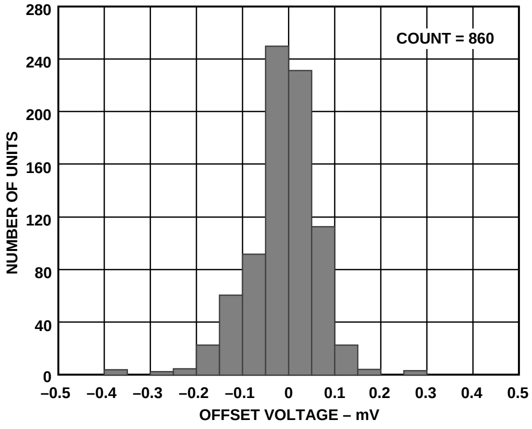


Figure 13. Input Offset Distribution, V_S = 5, 0

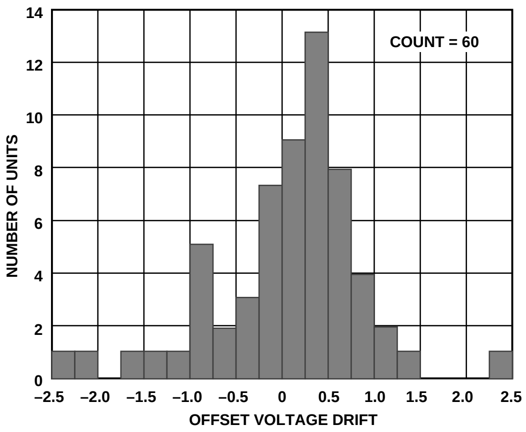


Figure 14. TC V_{OS} Distribution, –55°C to +125°C, V_S = 5, 0

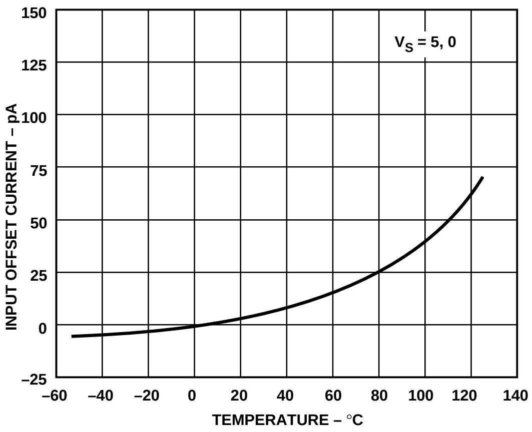


Figure 15. Input Offset Current vs. Temperature

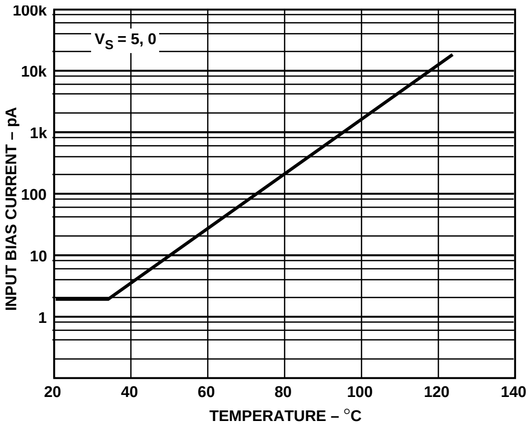


Figure 16. Input Bias Current vs. Temperature

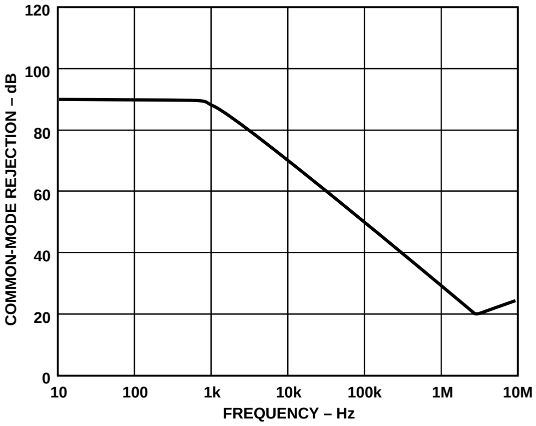


Figure 17. Common-Mode Rejection vs. Frequency

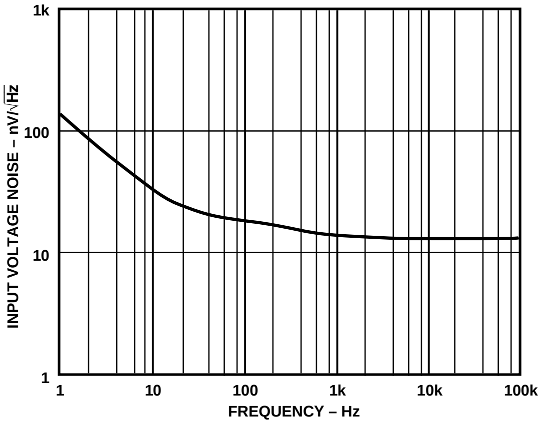


Figure 20. Input Voltage Noise Spectral Density vs. Frequency

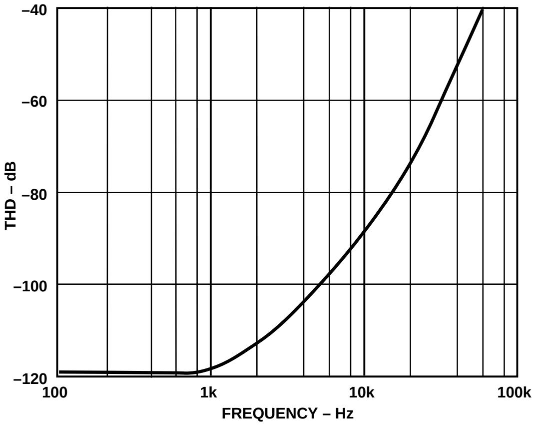


Figure 18. THD vs. Frequency, 3 V rms

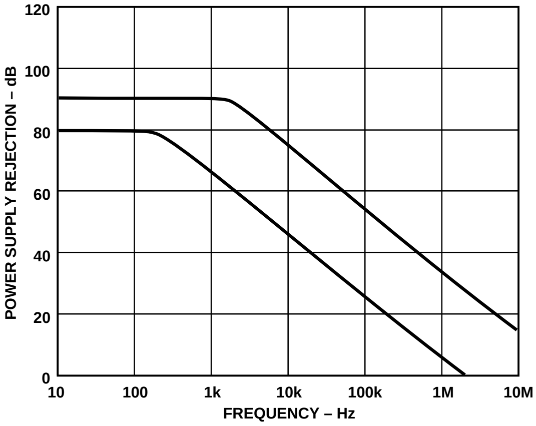


Figure 21. Power Supply Rejection vs. Frequency

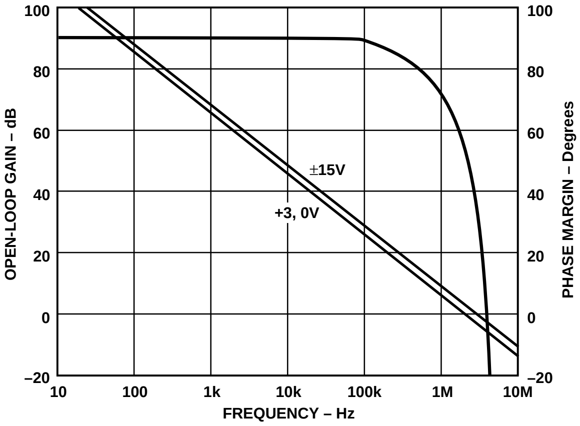


Figure 19. Open-Loop Gain and Phase vs. Frequency

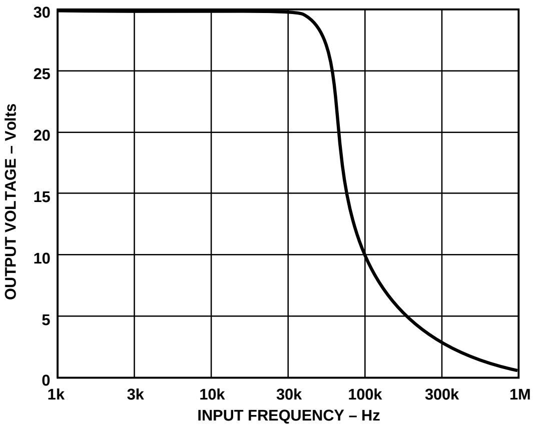


Figure 22. Large Signal Frequency Response

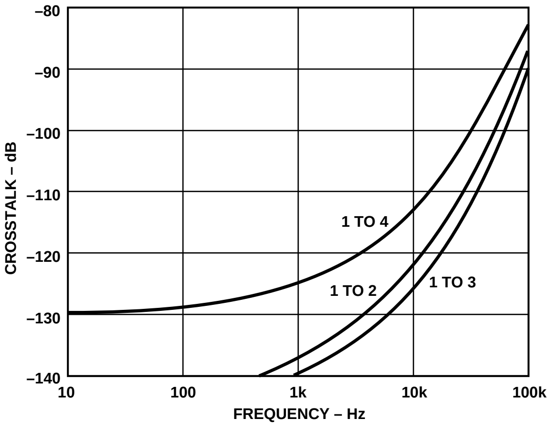


Figure 23. Crosstalk vs. Frequency

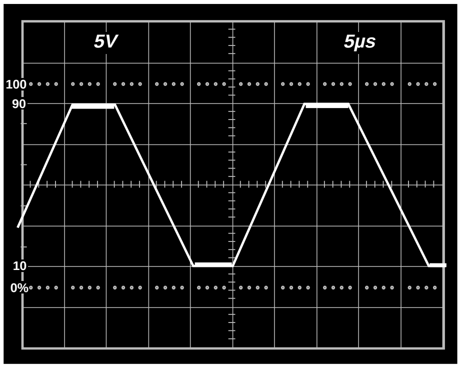


Figure 26. Large Signal Response

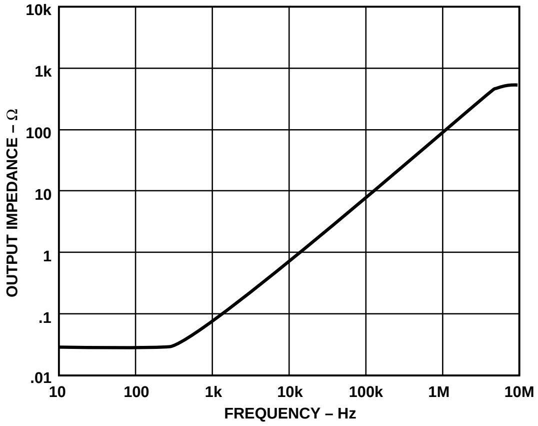


Figure 24. Output Impedance vs. Frequency, Gain = +1

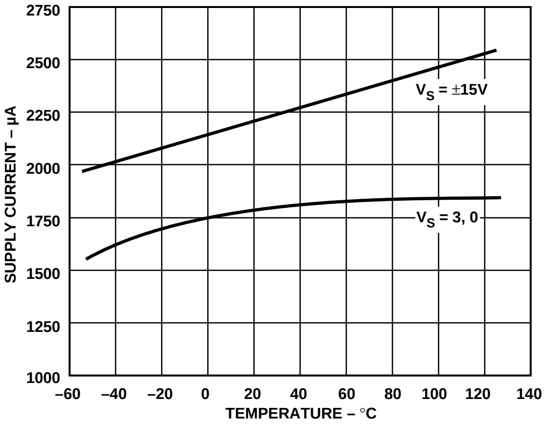


Figure 27. Supply Current vs. Temperature

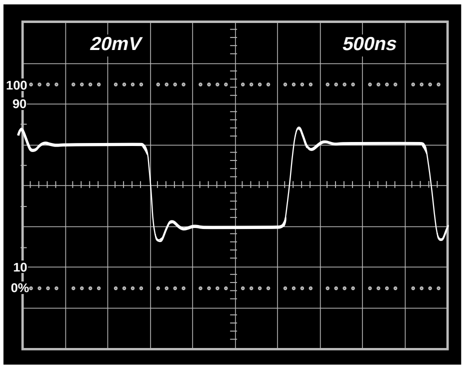


Figure 25. Small Signal Response, Unity Gain Follower, 10k||100 pF Load

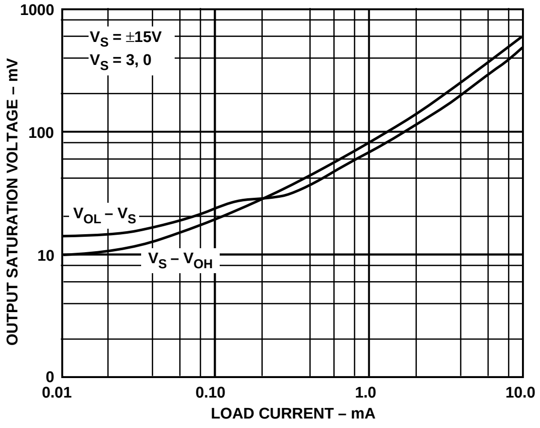


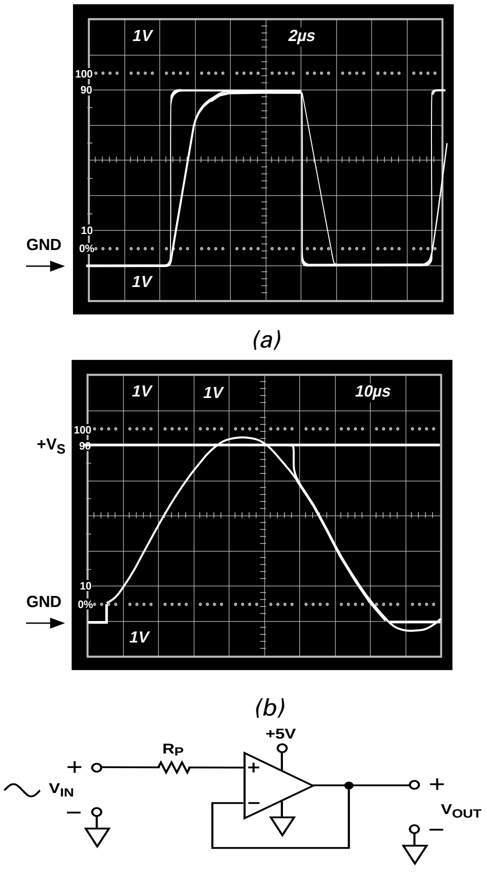
Figure 28. Output Saturation Voltage

APPLICATION NOTES

INPUT CHARACTERISTICS

In the AD824, n-channel JFETs are used to provide a low offset, low noise, high impedance input stage. Minimum input common-mode voltage extends from 0.2 V below $-V_S$ to 1 V less than $+V_S$. Driving the input voltage closer to the positive rail will cause a loss of amplifier bandwidth.

The AD824 does not exhibit phase reversal for input voltages up to and including $+V_S$. Figure 29a shows the response of an AD824 voltage follower to a 0 V to +5 V ($+V_S$) square wave input. The input and output are superimposed. The output tracks the input up to $+V_S$ without phase reversal. The reduced bandwidth above a 4 V input causes the rounding of the output wave form. For input voltages greater than $+V_S$, a resistor in series with the AD824's noninverting input will prevent phase reversal at the expense of greater input voltage noise. This is illustrated in Figure 29b.



(a)

(b)

Figure 29. (a) Response with $R_P = 0$; V_{IN} from 0 to $+V_S$
(b) $V_{IN} = 0$ to $+ V_S + 200$ m V
$V_{OUT} = 0$ to $+ V_S$
$R_P = 49.9$ kΩ

Since the input stage uses n-channel JFETs, input current during normal operation is positive; the current flows out from the input terminals. If the input voltage is driven more positive than $+V_S - 0.4$ V, the input current will reverse direction as internal device junctions become forward biased. This is illustrated in Figure 9.

A current-limiting resistor should be used in series with the input of the AD824 if there is a possibility of the input voltage exceeding the positive supply by more than 300 mV or if an input voltage will be applied to the AD824 when $\pm V_S = 0$. The amplifier will be damaged if left in that condition for more than 10 seconds. A 1 kΩ resistor allows the amplifier to withstand up to 10 volts of continuous overvoltage and increases the input voltage noise by a negligible amount.

Input voltages less than $-V_S$ are a completely different story. The amplifier can safely withstand input voltages 20 volts below the minus supply voltage as long as the total voltage from the positive supply to the input terminal is less than 36 volts. In addition, the input stage typically maintains picoamp level input currents across that input voltage range.

OUTPUT CHARACTERISTICS

The AD824's unique bipolar rail-to-rail output stage swings within 15 mV of the positive and negative supply voltages. The AD824's approximate output saturation resistance is 100 Ω for both sourcing and sinking. This can be used to estimate output saturation voltage when driving heavier current loads. For instance, the saturation voltage will be 0.5 volts from either supply with a 5 mA current load.

For load resistances over 20 kΩ, the AD824's input error voltage is virtually unchanged until the output voltage is driven to 180 mV of either supply.

If the AD824's output is overdriven so as to saturate either of the output devices, the amplifier will recover within 2 µs of its input returning to the amplifier's linear operating region.

Direct capacitive loads will interact with the amplifier's effective output impedance to form an additional pole in the amplifier's feedback loop, which can cause excessive peaking on the pulse response or loss of stability. Worst case is when the amplifier is used as a unity gain follower. Figures 5 and 7 show the AD824's pulse response as a unity gain follower driving 220 pF. Configurations with less loop gain, and as a result less loop bandwidth, will be much less sensitive to capacitance load effects. Noise gain is the inverse of the feedback attenuation factor provided by the feedback network in use.

Figure 30 shows a method for extending capacitance load drive capability for a unity gain follower. With these component values, the circuit will drive 5,000 pF with a 10% overshoot.

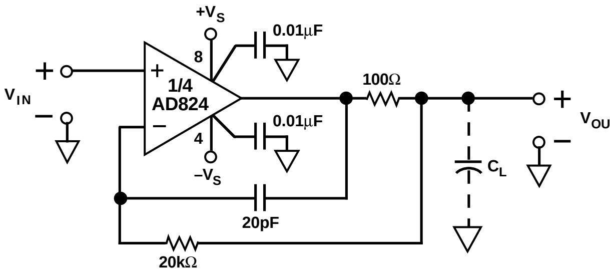
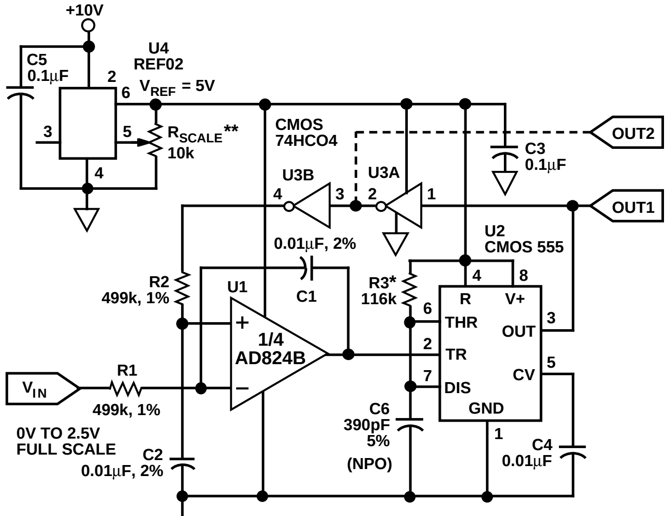


Figure 30. Extending Unity Gain Follower Capacitive Load Capability Beyond 350 pF

APPLICATIONS

Single Supply Voltage-to-Frequency Converter

The circuit shown in Figure 31 uses the AD824 to drive a low power timer, which produces a stable pulse of width t_1. The positive going output pulse is integrated by R1-C1 and used as one input to the AD824, which is connected as a differential integrator. The other input (nonloading) is the unknown voltage, V_{IN}. The AD824 output drives the timer trigger input, closing the overall feedback loop.



NOTES:

$f_{OUT} = V_{IN} / (VREF^* t_1)$, $t_1 = 1.1^*R3^*C6$

$= 25kHz\ f_S$ AS SHOWN.

* = 1% METAL FILM, <50ppm/°C TC

** = 10%, 20T FILM, <100ppm/°C TC

$t_1 = 33\mu s$ FOR $f_{OUT} = 20kHz$ @ $V_{IN} = 2.0V$

Figure 31. Single Supply Voltage-to-Frequency Converter

Typical AD824 bias currents of 2 pA allow megaohm-range source impedances with negligible dc errors. Linearity errors on the order of 0.01% full scale can be achieved with this circuit. This performance is obtained with a 5 volt single supply, which delivers less than 3 mA to the entire circuit.

Single Supply Programmable Gain Instrumentation Amplifier

The AD824 can be configured as a single supply instrumentation amplifier that is able to operate from single supplies down to 3 V or dual supplies up to ±15 V. AD824 FET inputs' 2 pA bias currents minimize offset errors caused by high unbalanced source impedances.

An array of precision thin-film resistors sets the in amp gain to be either 10 or 100. These resistors are laser-trimmed to ratio match to 0.01% and have a maximum differential TC of 5 ppm/°C.

Table I. AD824 In Amp Performance

Parameters	V_S = 3 V, 0 V	V_S = ±5 V
CMRR	74 dB	80 dB
Common-Mode Voltage Range	–0.2 V to +2 V	–5.2 V to +4 V
3 dB BW, G = 10	180 kHz	180 kHz
G = 100	18 kHz	18 kHz
$t_{SETTLING}$		
2 V Step (V_S = 0 V, 3 V)	2 µs	
5 V (V_S = ±5 V)		5 µs
Noise @ f = 1 kHz, G = 10	270 nV/√Hz	270 nV/√Hz
G = 100	2.2 µV/√Hz	2.2 µV/√Hz

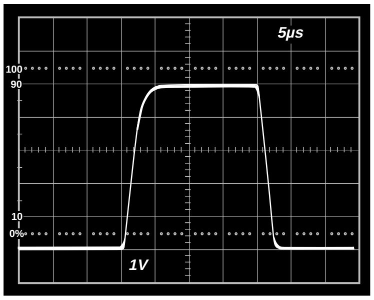
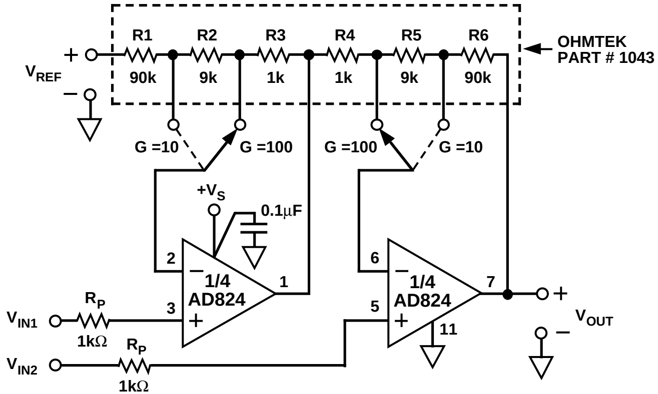


Figure 32a. Pulse Response of In Amp to a 500 mV p-p Input Signal; V_S = +5 V, 0 V; Gain = 10



$$(G = 10) \quad V_{OUT} = (V_{IN1} - V_{IN2})\left(1 + \frac{R6}{R4 + R5}\right) + V_{REF}$$

$$(G = 100) \quad V_{OUT} = (V_{IN1} - V_{IN2})\left(1 + \frac{R5 + R6}{R4}\right) + V_{REF}$$

FOR R1 = R6, R2 = R5 AND R3 = R4

Figure 32b. A Single Supply Programmable Instrumentation Amplifier

3 Volt, Single Supply Stereo Headphone Driver

The AD824 exhibits good current drive and THD+N performance, even at 3 V single supplies. At 1 kHz, total harmonic distortion plus noise (THD+N) equals –62 dB (0.079%) for a 300 mV p-p output signal. This is comparable to other single supply op amps that consume more power and cannot run on 3 V power supplies.

In Figure 33, each channel's input signal is coupled via a 1 µF Mylar capacitor. Resistor dividers set the dc voltage at the noninverting inputs so that the output voltage is midway between the power supplies (+1.5 V). The gain is 1.5. Each half of the AD824 can then be used to drive a headphone channel. A 5 Hz high-pass filter is realized by the 500 µF capacitors and the headphones, which can be modeled as 32 ohm load resistors to ground. This ensures that all signals in the audio frequency range (20 Hz–20 kHz) are delivered to the headphones.

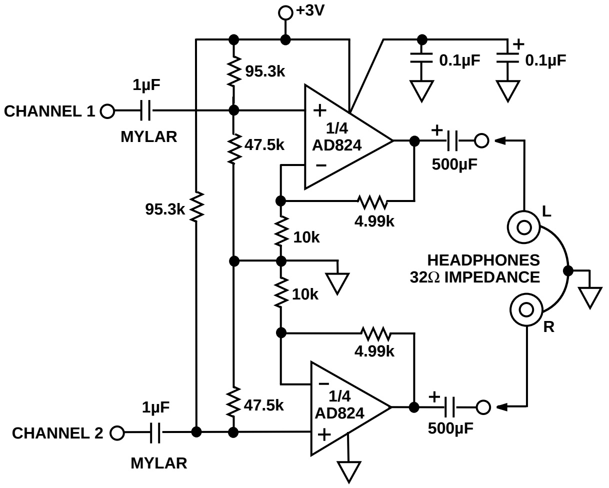


Figure 33. 3 Volt Single Supply Stereo Headphone Driver

Low Dropout Bipolar Bridge Driver

The AD824 can be used for driving a 350 ohm Wheatstone bridge. Figure 34 shows one half of the AD824 being used to buffer the AD589—a 1.235 V low power reference. The output of +4.5 V can be used to drive an A/D converter front end. The other half of the AD824 is configured as a unity-gain inverter and generates the other bridge input of –4.5 V. Resistors R1 and R2 provide a constant current for bridge excitation. The AD620 low power instrumentation amplifier is used to condition the differential output voltage of the bridge. The gain of the AD620 is programmed using an external resistor R_G and determined by:

$$G = \frac{49.4\ k\Omega}{R_G} + 1$$

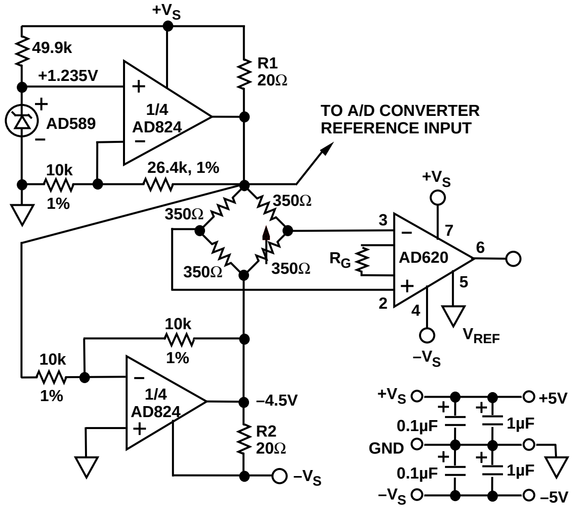


Figure 34. Low Dropout Bipolar Bridge Driver

A 3.3 Volt/5 Volt Precision Sample-and-Hold Amplifier

In battery-powered applications, low supply voltage operational amplifiers are required for low power consumption. Also, low supply voltage applications limit the signal range in precision analog circuitry. Circuits like the sample-and-hold circuit shown in Figure 35, illustrate techniques for designing precision analog circuitry in low supply voltage applications. To maintain high signal-to-noise ratios (SNRs) in a low supply voltage application requires the use of rail-to-rail, input/output operational amplifiers. This design highlights the ability of the AD824 to operate rail-to-rail from a single +3 V/+5 V supply, with the advantages of high input impedance. The AD824, a quad JFET-input op amp, is well suited to S/H circuits due to its low input bias currents (3 pA, typical) and high input impedances ($3 \times 10^{13}\ \Omega$, typical). The AD824 also exhibits very low supply currents so the total supply current in this circuit is less than 2.5 mA.

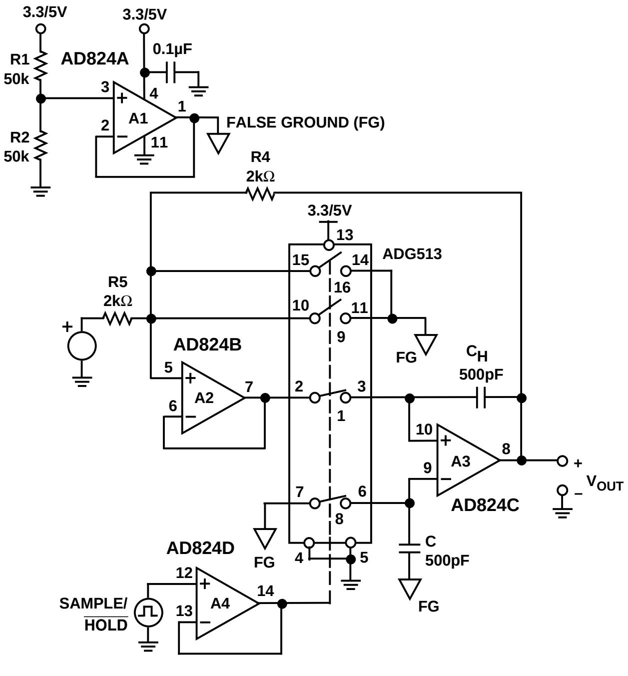


Figure 35. 3.3 V/5.5 V Precision Sample and Hold

In many single supply applications, the use of a false ground generator is required. In this circuit, R1 and R2 divide the supply voltage symmetrically, creating the false ground voltage at one-half the supply. Amplifier A1 then buffers this voltage creating a low impedance output drive. The S/H circuit is configured in an inverting topology centered around this false ground level.

A design consideration in sample-and-hold circuits is voltage droop at the output caused by op amp bias and switch leakage currents. By choosing a JFET op amp and a low leakage CMOS switch, this design minimizes droop rate error to better than 0.1 µV/µs in this circuit. Higher values of C_H will yield a lower droop rate. For best performance, C_H and C2 should be polystyrene, polypropylene or Teflon capacitors. These types of capacitors exhibit low leakage and low dielectric absorption. Additionally, 1% metal film resistors were used throughout the design.

In the sample mode, SW1 and SW4 are closed, and the output is $V_{OUT} = -V_{IN}$. The purpose of SW4, which operates in parallel with SW1, is to reduce the pedestal, or hold step, error by injecting the same amount of charge into the noninverting input of A3 that SW1 injects into the inverting input of A3. This creates a common-mode voltage across the inputs of A3 and is then rejected by the CMR of A3; otherwise, the charge injection from SW1 would create a differential voltage step error that would appear at V_{OUT}. The pedestal error for this circuit is less than 2 mV over the entire 0 V to 3.3 V/5 V signal range. Another method of reducing pedestal error is to reduce the pulse amplitude applied to the control pins. In order to control the ADG513, only 2.4 V are required for the "ON" state and 0.8 V for the "OFF" state. If possible, use an input control signal whose amplitude ranges from 0.8 V to 2.4 V instead of a full range 0 V to 3.3 V/5 V for minimum pedestal error.

Other circuit features include an acquisition time of less than 3 µs to 1%; reducing C_H and C2 will speed up the acquisition time further, but an increased pedestal error will result. Settling time is less than 300 ns to 1%, and the sample-mode signal BW is 80 kHz.

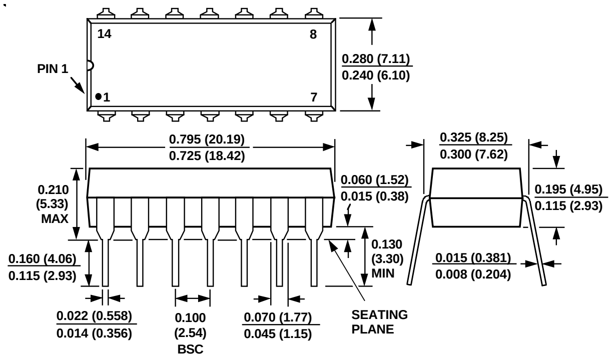
The ADG513 was chosen for its ability to work with 3 V/5 V supplies and for having normally-open and normally-closed precision CMOS switches on a dielectrically isolated process. SW2 is not required in this circuit; however, it was used in parallel with SW3 to provide a lower R_{ON} analog switch.

```
* AD824 SPICE Macro-model         9/94, Rev. A *
                                  ARG/ADI
*
* Copyright 1994 by Analog Devices, Inc.
*
* Refer to "README.DOC" file for License Statement.
Use of this model indicates your acceptance with
the terms and provisions in the License Statement. *
* Node assignments
*                              noninverting input
*                              | inverting input
*                              | | positive supply
*                              | | | negative supply
*                              | | | | output
*                              | | | | |
.SUBCKT AD824                  1 2 99 50 25
*
* INPUT STAGE & POLE AT 3.1 MHz
*
R3      5       99      1.193E3
R4      6       99      1.193E3
CIN     1       2       4E-12
C2      5       6       19.229E-12
I1      4       50      108E-6
IOS     1       2       1E-12
EOS     7       1       POLY(1) (12,98) 100E-6 1
J1      4       2       5            JX
J2      4       7       6            JX
*
* GAIN STAGE & DOMINANT POLE
*
EREF    98      0       (30,0) 1
R5      9       98      2.205E6
C3      9       25      54E-12
G1      98      9       (6,5) 0.838E-3
V1      8       98      -1
V2      98      10      -1
D1      9       10      DX
D2      8       9       DX
*
* COMMON-MODE GAIN NETWORK WITH ZERO AT 1 kHz *
R21     11      12      1E6
R22     12      98      100
C14     11      12      159E-12
E13     11      98      POLY(2) (2,98) (1,98) 0 0.5 0.5
*
* POLE AT 10 MHz
*
R23     18      98      1E6
C15     18      98      15.9E-15
G15     98      18      (9,98) 1E-6
*
* OUTPUT STAGE
*
ES      26      98      (18,98) 1
RS      26      22      500
IB1     98      21      2.404E-3
IB2     23      98      2.404E-3
D10     21      98      DY
D11     98      23      DY
C16     20      25      2E-12
C17     24      25      2E-12
DQ1     97      20      DQ
Q2      20      21      22  NPN
Q3      24      23      22  PNP
DQ2     24      51      DQ
Q5      25      20      97  PNP 20
Q6      25      24      51  NPN 20
VP      96      97      0
VN      51      52      0
EP      96      0       (99,0) 1
EN      52      0       (50,0) 1
R25     30      99      5E6
R26     30      50      5E6
FSY1    99      0       VP 1
FSY2    0       50      VN 1
DC1     25      99      DX
DC2     50      25      DX
*
* MODELS USED
*
.MODEL JX NJF(BETA=3.2526E-3 VTO=-2.000 IS=2E-12) .MODEL
NPN NPN(BF=120 VAF=150 VAR=15 RB=2E3
+ RE=4 RC=550 IS=1E-16)
.MODEL PNP PNP(BF=120 VAF=150 VAR=15 RB=2E3 + RE=4
RC=750 IS=1E-16)
.MODEL DX D(IS=1E-15)
.MODEL DY D()
.MODEL DQ D(IS=1E-16)
.ENDS AD824
```

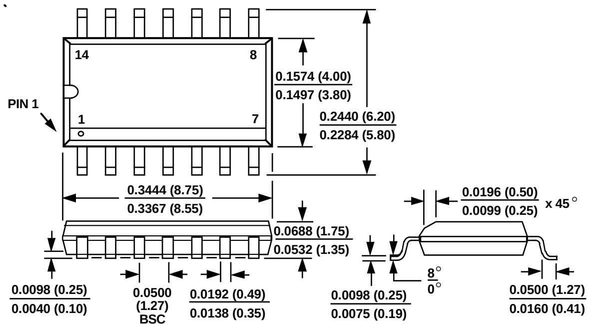
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

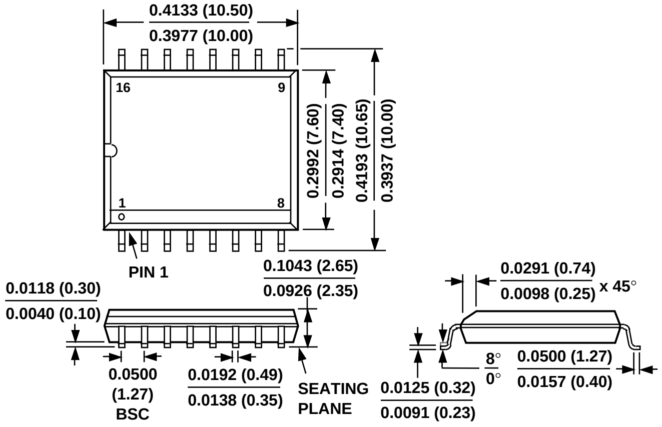
14-Pin Plastic (N) Package
(N-14)



14-Pin SOIC (R) Package
(R-14)



16-Pin SOIC Package
(R-16)



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