



## Application Note

ACA0861 - A, B, C, D  
750/860 MHz CATV Line Amplifiers  
Rev 2

### RELEVANT PRODUCTS

- ACA0861A
- ACA0861B
- ACA0861C
- ACA0861D

### OVERVIEW - WHY USE THIS PART?

A new option is now available to CATV Trunk amplifier and Line Extender designers. The ANADIGICS ACA0861 family of surface mount monolithic GaAs RF Linear Amplifiers has been developed to replace, in future designs, the standard Silicon Hybrid amplifiers presently in use. This family of amplifiers was designed specifically for the demanding CATV market. A product with outstanding performance, coupled with exceptional reliability and ruggedness, as required by the CATV industry, is the result of years of research and development. Designers utilizing this part can expect better linearity, higher overall gain, flatter frequency response, better return loss, lower noise figure, and lower power consumption all at a competitive price compared to standard RF Hybrids. The use of a surface mount package allows fully automated assembly, reducing the inherent product costs.

While use of this part requires more up-front engineering than using the present CATV Hybrids in the standard package, the user will benefit in the long term in the following ways:

1. Lower total material costs than for the standard hybrid circuit.
2. Lower assembly costs due to fully automated assembly on the PCB.
3. Better CTB, CSO and XMODs
4. Better return loss
5. Lower power consumption

Why use this part? Because it is the highest performance, lowest cost solution available.

### BASIC CIRCUITS OPERATION

The ACA0861 consists of two monolithic GaAs RF linear amplifiers connected in parallel, as shown in

Figure 1. A basic cascade circuit topology, shown in Figure 2, is used for each amplifier. This circuit approach meets the demanding performance requirements of low distortion and low noise figure.

Two ACA0861 Amplifiers cascaded between baluns are used to create a hybrid equivalent, each amplifier having 12dB gain each. Reducing the gain to 12dB allows the use of more feedback per amplifier, improving the distortion of the amplifier, flattening the gain and improving device to device repeatability, while spreading out the power dissipation. Dividing the power dissipated between two packages allows the use of fully machine insertable plastic surface mount packages for the amplifiers, greatly reducing final PCB assembly costs.

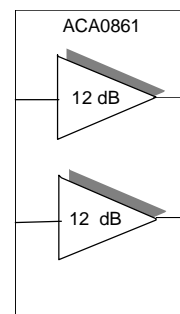


Figure 1: ACA0861 Block Diagram

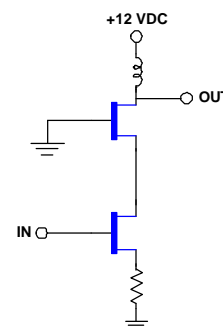


Figure 2: Basic Amplifier Stage Circuit Topology

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The amplifiers are fabricated on GaAs using a 20 GHz MESFET process. Utilizing MESFETs enhances third order distortion performance (CTB), since MESFETs are generally square law devices with low third order terms. Monolithic amplifiers provide matching between amplifiers, which yields outstanding second order cancellation, giving improved CSO performance to what is currently available. Flat frequency response, good input and output match and low distortion up to 860 MHz is achieved by using 20 GHz  $f_t$  transistors. On-chip circuitry assures good RF stability under high VSWR load conditions, preventing unwanted oscillations. The use of MESFETs also gives low noise figures, typically 2.5 dB for the amplifiers alone, and 3.5 dB for the full cascade. The noise figure remains very flat across the full frequency range.

The input and output impedance of each amplifier is designed to be 37.5 ohms, half of the standard 75 ohms. This gives a matched 75 ohm input and output impedance when combined with external transmission line baluns. Typically, the overall return loss is greater than 18 dB across the full frequency band.

Figure 3 shows the basic biasing circuit used. This consists of external 390 nH RF bias chokes, 300pF coupling capacitors and RF bypassing capacitors and a fixed resistor to select the desired bias current. The supply voltage is +12 VDC, not the typical +24 VDC of hybrid modules. The reduced voltage allows for a significant DC power dissipation saving. A resistor is used to set the supply current drawn by the amplifiers. The resistor values are initially fixed for each of the four amplifier types but can be set to a different value by the end user, changing the current and distortion characteristics of the amplifier, to optimize the performance for a given application.

### THE ACA0861 FAMILY OF AMPLIFIERS

There are four ACA0861 amplifier versions (A through D) available. Specifying distortion performance at specific output signal levels differentiates the amplifiers. Amplifiers A & C have distortion performance specified at + 34 dBmV output signal level for low level or input stage applications. Amplifiers B & D have distortion performance specified at + 44 dBmV output signal level for high level or output stage applications. Each of the four amplifiers operates at a different current. This adds

a great deal of flexibility in the design of Trunk Amplifiers or Line Extenders since new designs can provide a optimum distortion level at the minimum power dissipation with the repeatability of monolithic fabrication. Refer to the ACA0861 data sheet for individual specifications.

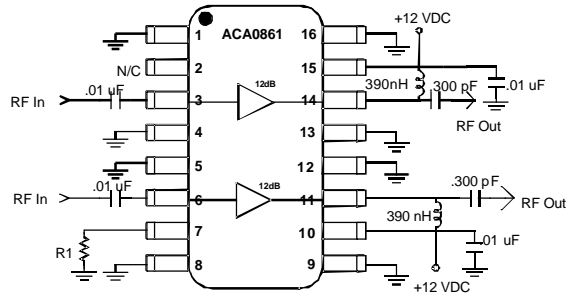


Figure 3: Basic Biasing Circuit

Table 1: Pin Description

PIN	DESCRIPTION	PIN	DESCRIPTION
1	GND	9	GND
2	Leave Open	10	+VD
3	RF <sub>IN</sub> #1	11	RF <sub>OUT</sub> #2
4	GND	12	GND
5	GND	13	GND
6	RF <sub>IN</sub> #2	14	RF <sub>OUT</sub> #1
7	I <sub>ADJ</sub> Resistor	15	+VD
8	GND	16	GND

Table 2: R1 Resistor Values

PART TYPE	R1 VALUE
ACA0861A	21.5
ACA0861B	274
ACA0861C	121
ACA0861D	Open

**BUILDING A HYBRID EQUIVALENT**

**Basic Schematic**

To construct a hybrid equivalent amplifier the circuit shown in Figure 4 is used. This consists of two ACA0861 amplifiers cascaded between two transmission line baluns. To construct an equivalent to a standard 860 MHz hybrid, one ACA0861A is cascaded with one ACA0861B. To construct an improved 860 MHz power doubler hybrid equivalent, one ACA0861C is cascaded with one ACA0861D. Even better performance can be achieved by cascading two ACA0861D together. See Table 3 for different cascading possibilities. This configuration typically provides 22 dB of gain when balun losses are accounted for.

Separating the overall gain between two stages provides a lot of flexibility for the designer who is now able to mix and match the amplifiers to provide the exact distortion performance required at the minimum power dissipation. Three or four stages can also be cascaded reducing the number of baluns required. Biasing coils, coupling capacitors and bias select resistors are needed as shown.

**External Component Selection**

Chip surface mount external components should be used for biasing and coupling. The bias coils should have a low equivalent series resistance to limit the voltage drop across them, have a high enough current rating for the part selected and should not have a series resonance within the passband of interest. Capacitors should be chip surface mount type. The current select resistor can be a small chip resistor (maximum current is 2 mA).

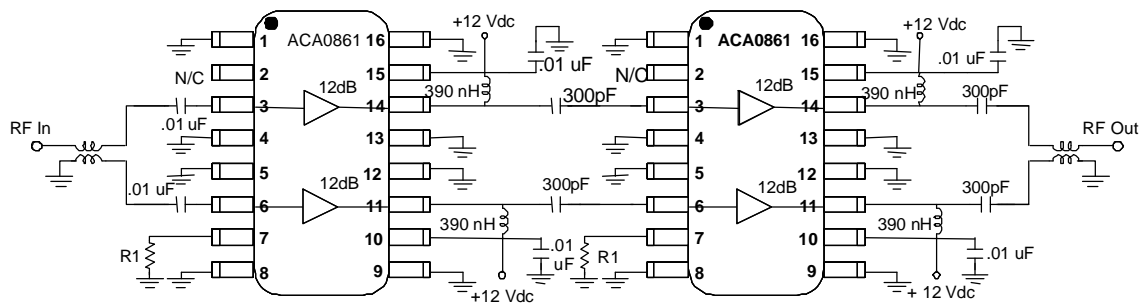
**Layout Consideration**

The same care and precautions commonly used in all RF layouts should be used here. For optimum performance, transmission lines between the baluns should have characteristic impedance of 37.5 ohms. Transmission lines connected to the secondary of the baluns should be laid out for 75 ohm characteristic impedance. The 37.5 ohm transmission lines may get wide depending on the thickness of the circuit board. If the line thickness is too wide, a coplanar transmission line can be used to reduce the line width.

The bottom of the package contains a heat slug, which provides a low thermal impedance path to remove the heat generated by the device, and is the DC and RF ground. This must be soldered to a good DC /RF ground with a low thermal resistance to the chassis (see the section on Thermal Considerations).

**Balun Selection/Design**

Two baluns are required in addition to the amplifiers. Typically, a transmission line balun is used due to its good frequency response, amplitude balance, phase balance and ease of assembly. The schematic diagram and assembly diagram of the transmission line balun is shown in Figure 5. For good results use 75 ohm characteristic impedance twin lead for the transmission line with typically 5 to 6 turns around a ferrite core. The ferrite core should be low loss with a high enough permeability to



**Figure 4: Hybrid Equivalent Circuit**

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provide high return impedance to the output with the number of turns used. The number of turns used is affected by two considerations; there must be enough turns to achieve adequate flux for the low frequency response required and not too many turns, or the high frequency response will be affected by stray

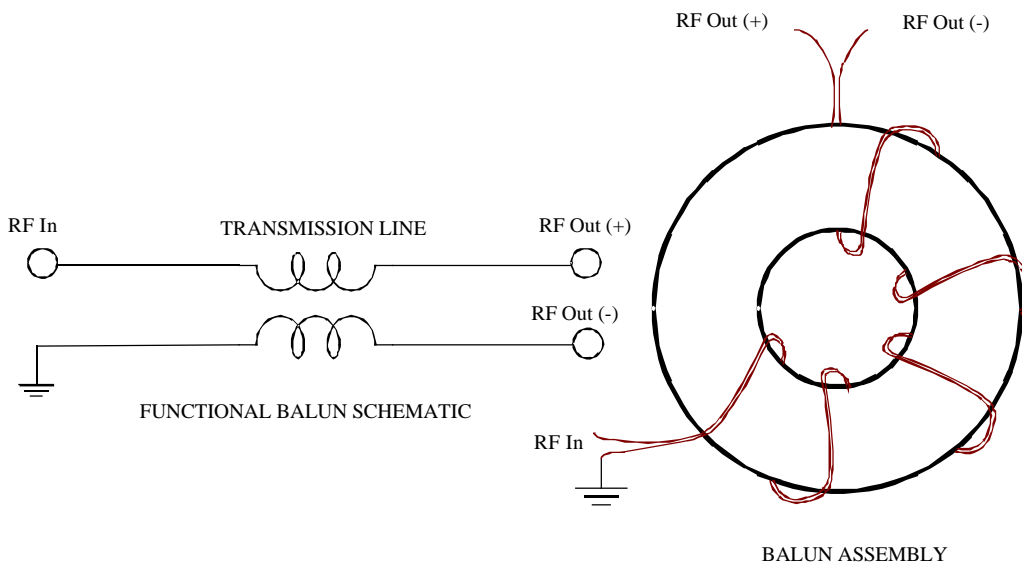
capacitance. Table 4 also includes a parts list for a typical 750/860 MHz balun. This circuit does not use a third, or tertiary winding which may be used to improve phase or amplitude balance. Other balun configurations can be used, though they must match into 37.5 ohm impedance.

**Table 3: Cascade Possibilities**

CASCADE POSSIBILITIES		
1ST STAGE	2ND STAGE	RESULT
ACA0861A	ACA0861B	STANDARD 750/860 MHZ HYBRID
ACA0861C	ACA0861D	750/860 MHZ POWER DOUBLER
ACA0861A	ACA0861C	LOW POWER, INCREASED DISTORTION
ACA0861B	ACA0861D	HIGH POWER, VERY LOW DISTORTION
ACA0861D	ACA0861D	VERY HIGH POWER, EXTREMELY LOW DISTORTION

**Table 4: Parts List for Balun**

ITEM	MANUFACTURER/PART NUMBER
Ferrite Core	Philips 135CT050-3D3
Twin Lead	MWS B2383611



**Figure 5: Balun Schematic and Assembly**

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### IMPROVED TEMPERATURE BIAS CIRCUIT

The standard distortion performance vs. temperature of the ACA0861 family of amplifiers can be improved, when necessary, by the addition of an external 5.6K ohm resistor with a positive temperature coefficient and by disconnecting pin 10 on the ACA0861. This change is shown in Figure 6. The figure shows the 5.6K ohm resistor connected between the +12 VDC supply and pin 7 of the device. In addition, pin 10 is now left floating and cannot be connected to ground. This circuit reduces the DC current variation of the amplifiers with temperature and minimizes any distortion performance changes.

For optimum performance the 5.6K ohm resistor temperature coefficients listed in Table 5 are recommended.

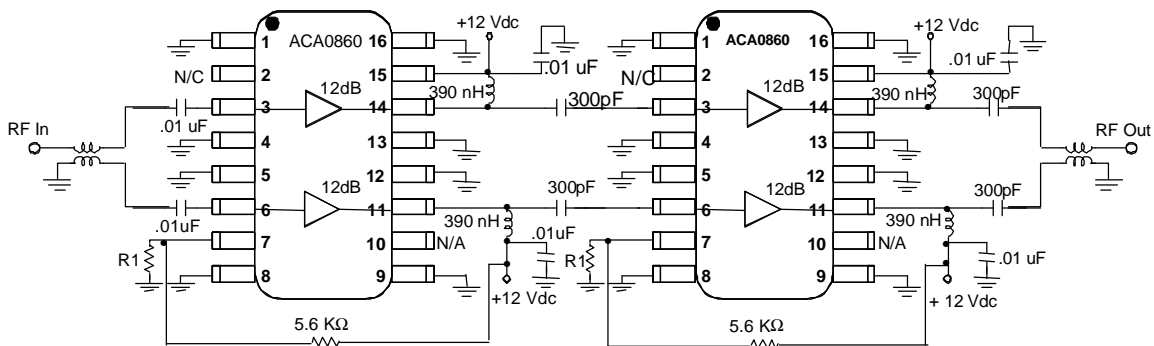
**Table 5: Temperature Coefficients of Resistor**

PART NUMBER	TCR	NOTES
ACA0861A	+7000 ppm/C	Usually not needed
ACA0861B	+3900 ppm/C	
ACA0861C	+3900 ppm/C	
ACA0861D	+1400 ppm/C	

A potential source for the resistors is the LT73 line of positive temperature coefficient resistors from KOA Speer Electronics, Inc. @ (814) 362-5536 in the USA. These are chip resistors and are supplied on tape and reel. Please note that the user must determine if these resistors are acceptable for their application, ANADIGICS does not make any claims as to third party products.

### RELIABILITY RESULTS

The ACA0861 family of amplifiers is designed specifically for the demanding CATV market, where the reliability of the parts in a hostile environment is of utmost importance. This product was designed from the beginning with this in mind. An oversized layout, eutectic mount, and custom SOIC package with a heat slug were developed to minimize the channel temperature, greatly improving reliability. These devices are fabricated using a proven GaAs MESFET process with the largest GaAs reliability database in the industry. Temperature cycling, temperature shock, and HAST tests have all confirmed that a rugged design exists. Overall, an MTF of 10<sup>7</sup> hours is expected with a package heat slug temperature of up to 110°C. A summary of the reliability testing to date is shown Table 6.



**Figure 6: ACA0861 Improved Temperature Bias Option**

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**Table 6: Test Conditions**

TEST	SPECIFICATION	CONDITIONS	PASS/FAIL
Temperature Cycling w/ Pre-stress	PRESTRESS JEDEC-JESD22 Test Method A112 (Reduced)  TEMP CYCLE STRESS MIL-STD-883 Method 1010	PRESTRESS 85%RH/85C/72Hours Reflow 230C,Peak  STRESS -65C to +150C Air to Air 100 Cycles 500 Cycles 1000 Cycles	110 / 0 55 / 0 55 / 0
Steady State Humidity w/Pre-stress	PRESTRESS JEDEC-JESD22 Test Method A112 (Reduced)  HUMIDITY STRESS JEDEC-22-A101 Without Bias	PRESTRESS 85%RH/85C/72 Hours Reflow 230C Peak  STRESS 85%RH/85C 1000 Hours	153 / 0
Hast Accelerated Humidity	JEDEC 22-A110 w/o Bias	85%RH/125C 72 Hours	110 / 0
Solderability	MIL-STD-883 Method 2003	8 Hour Steam Age 95% Coverage	22 / 0
Lead Integrity	ANADIGICS 80010-330	One 90 Bend and Return	22 / 0
Brand Permanence	MIL-STD-883 Method 2015	Terpene Solvent Only	22 / 0
Wire Pull	ANADIGICS 60021-001	4-Grams Minimum 4-Wires/Device	263 / 1
Die Shear		1-Kgram Minimum	66 / 0
ESD	MIL-STD-883 Method 3015 HBM/100PF/1500 ohm	+/- 250 Volts Pins 2, 3, 6, 7, 10, 11,14,15	21 / 0

**THERMAL MOUNTING CONSIDERATIONS**

The PCB layout for the ACA0861 family of amplifiers must consider both the electrical requirements of the parts (proper line impedance, bypassing, etc.) and the thermal requirements. The thermal requirement, to meet the stated MTF on the data sheet, states that the maximum temperature of the heat slug on the bottom of the ACA0861 package is 110° C. The PCB must be designed to meet this

requirement at the maximum expected system ambient temperature. To do this, the following two parameters need to be known: the maximum external ambient temperature and the temperature rise of the chassis above the external ambient temperature due to the internal heat being generated by the parts inside. Once these two parameters are known the maximum temperature rise between the chassis and the ACA0861 devices can easily be calculated.

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The maximum allowable temperature rise ( $\Delta T_{\max}$ ) from the chassis to the ACA0861 is calculated as follows:

$$\Delta T_{\max} = T_{\text{op}} - T_{\text{ext}} - \Delta T_{\text{chassis}}$$

where

$T_{\text{op}}$  is the maximum operating temperature of the ACA0861, measured at the heat slug (110 °C);

$T_{\text{ext}}$  is the maximum external temperature;

and  $\Delta T_{\text{chassis}}$  is the temperature rise of the chassis due to internal heating.

For example, if  $T_{\text{ext}} = 60^\circ\text{C}$  and  $\Delta T_{\text{chassis}} = 20^\circ\text{C}$ ,

then  $\Delta T_{\max} = 110^\circ\text{C} - 60^\circ\text{C} - 20^\circ\text{C} = 30^\circ\text{C}$ .

In the above example, a 30° C rise is allowed in the PCB mount between the bottom of the ACA0861 and the chassis. Knowing this, a PCB can be designed that provides a thermal resistance which will maintain a 30° C rise or less.

### Thermal Interfaces

There are typically three different thermal interfaces between the bottom of the ACA0861 and the chassis. The first is the solder connection of the ACA0861 heat slug to the PCB. The second interface is the heat transfer through the PCB, and the third is the PCB to chassis interface. (See Figure 7.)

The first interface, the solder connection of the ACA0861 heat slug to the PCB, should cover the full area of the ACA0861 heat slug for maximum effectiveness.

The second interface is the heat transfer through the PCB. FR4, the typical PCB material, has very poor thermal conduction properties and cannot be used without the addition of plated through via holes under the ACA0861. The vias holes should be copper plated and then solder filled for the lowest thermal resistance. The vias then conduct the heat through the FR4 to the bottom of the PCB, while the FR4 material provides little conduction. The thermal resistance of the vias holes, given in degree C rise per watt of power dissipation, is a function of via diameter and the thickness of the copper plating on

the walls of the vias. Tables 1, 2, and 3 show the calculated thermal resistance of solder filled plated through via holes with different via diameters and copper plating thicknesses. Table 1 shows the thermal resistance with 0.8 mil copper plating, Table 2 with 1 mil, and Table 3 with 2 mil copper plating, where 1 mil = 0.001". The thermal resistance of the copper plating alone is shown in the column "plating". The thermal resistance of the solder fill is shown in the next column and the column labeled "combined" shows the calculated thermal resistance of both the copper plating and the solder fill for a single via. The next columns show the thermal resistance achieved by using multiple vias.

As an example, a 35 mil diameter via with 2 mil thick copper plating has the following properties:

Thermal resistance of the copper plating = 29.6° C/W  
Thermal resistance of the solder fill = 63.4° C/W  
Combined thermal resistance of single via = 20.17° C/W

A thermal resistance of 20.17 °C/Watt would produce a 125° C rise with 6.2 Watts of power dissipation (ACA0861D device), and therefore, a single via cannot be used. As more vias are added the combined thermal resistance decreases quickly and is determined the same way as for parallel resistors.

From Table 7, ten 35 mil vias have a thermal resistance of 2.02° C per Watt, while 40 vias have a thermal resistance of only 0.50° C per Watt. If forty 35 mil dia. vias are used instead of one, the temperature rises though the PCB is now only 3.1°C at 6.2 watts. The actual via diameter, thickness of the copper plating, and number of vias used will be determined by the limits of the PCB manufacturing process used.

The third interface is between the PCB and the chassis. Note the chassis is considered an infinite heat sink in this application note. Unlike the ACA0861 to PCB interface, this cannot be a solder connection due to the mismatch in thermal expansion of the PCB and chassis material and other production problems. A thermally conductive elastomer or gasket material is recommended. One such material that may be applicable for this application is Thermagon, Inc.'s\* T-PLI 200 material. This material is a thermally conductive, conformable elastomer that is available in either sheet form or cut to size. This

\* Thermagon, Inc. (216) 741-7659

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material should conform to any irregularities on the PCB and chassis surfaces caused by the manufacturing process while providing a low thermal resistance. A sheet thickness of 20 mils appears to be the best compromise between thermal resistance, tolerance buildup, and handling. The 20 mil thick material has a stated thermal resistance of 0.14° C in 2 per Watt. Using a square area of 0.1 square inch at this interface and a power dissipation of 6.2 Watts, a temperature rise of 8.7° C is expected. The PCB should be attached to the chassis with screws, providing a slight compression of the elastomer material. The user must determine if this material is acceptable for their application; ANADIGICS does not make any claims as to third party products.

### Putting It All Together

An FR4 board was manufactured using 35 mil diameter vias on a 4 by 12 grid with 45 mil center to center spacing. A total of 48 vias was used as shown in Figure 7. Vias were extended beyond the heat slug area on the top on the PCB due to the heat conduction of the copper plating. The board was fabricated with 2 mil copper plating and solder filled

vias. An ACA0861D part was soldered to the PCB and the PCB was clamped to a brass block with 20-mil thick T-PLI material between the PCB and brass block. Approximately 4 mils of compression of the T-PLI material was used. An IR scan of the assembly was then done showing a 14° rise from the brass block to the bottom of the heat slug at 5.64 watts power dissipation. This agrees well with the theoretical calculation. The PCB and T-PLI material have a calculated thermal resistance, based upon the IR measurement, of 2.5° C per Watt. At the full 6.2 watts of dissipation, the rise from the chassis to ACA0861 heat slug would be only 15.5° C.

### Thermal Conclusion

The ACA0861 family of amplifiers uses a 16 pin wide body SOIC package that was custom designed for surface mount applications with high power dissipation. The use of multiple copper plated, solder filled vias under the package's heat slug while using a thermal conductive elastomer or gasket material between the PCB and chassis provides a low thermal resistance mount.

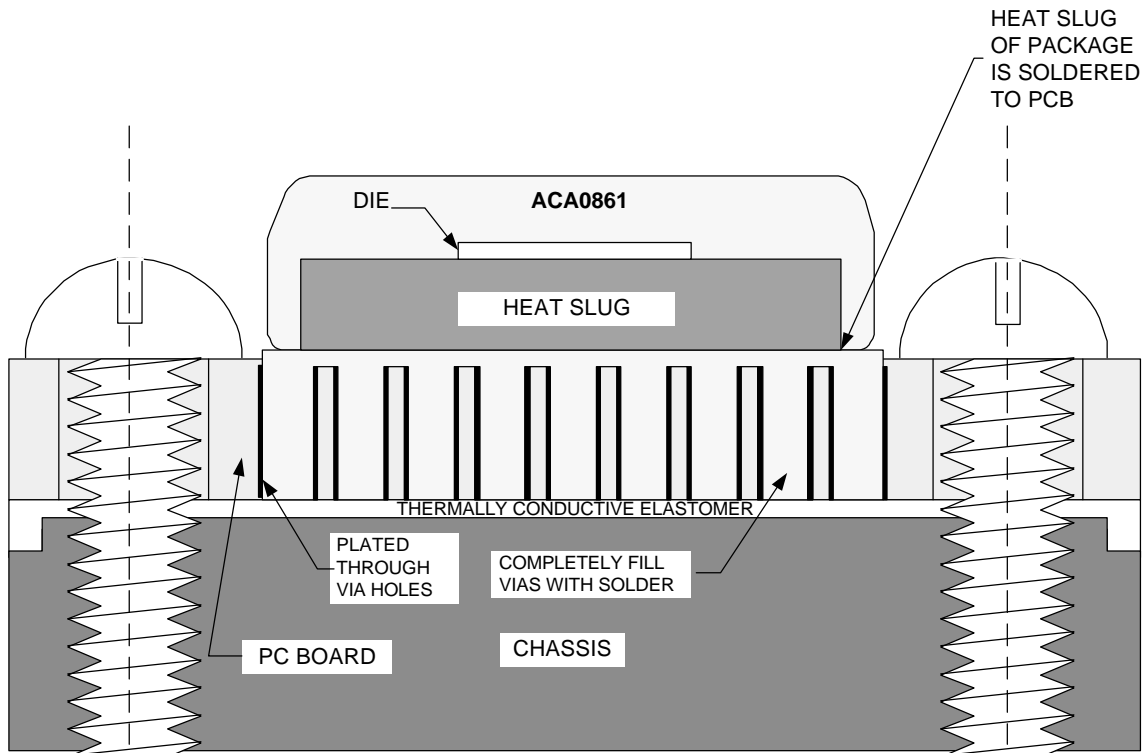


Figure 7: ACA0861 PCB Mounting - Front



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**Table 7: Thermal Resistance of Solder Filled, Plated Through Via Hole - 0.8 mil Plating Thickness**

Via Dia (Mils)	Thermal resistance (°C/Watt)			Multiple Vias					
	Plating	Fill	Combined	10	20	30	40	50	60
10	265.2	863.7	202.92	20.29	10.15	6.76	5.07	4.06	3.38
11	239.2	689.7	177.62	17.76	8.88	5.92	4.44	3.55	2.96
12	217.9	563.4	157.12	15.71	7.86	5.24	3.93	3.14	2.62
13	200.0	468.9	140.21	14.02	7.01	4.67	3.51	2.80	2.34
14	184.9	396.3	126.06	12.61	6.30	4.20	3.15	2.52	2.10
15	171.8	339.4	114.08	11.41	5.70	3.80	2.85	2.28	1.90
16	160.5	293.9	103.83	10.38	5.19	3.46	2.60	2.08	1.73
17	150.6	257.0	94.96	9.50	4.75	3.17	2.37	1.90	1.58
18	141.9	226.6	87.24	8.72	4.36	2.91	2.18	1.74	1.45
19	134.1	201.3	80.47	8.05	4.02	2.68	2.01	1.61	1.34
20	127.1	180.0	74.49	7.45	3.72	2.48	1.86	1.49	1.24
21	120.8	161.9	69.19	6.92	3.46	2.31	1.73	1.38	1.15
22	115.1	146.4	64.45	6.44	3.22	2.15	1.61	1.29	1.07
23	109.9	133.1	60.20	6.02	3.01	2.01	1.50	1.20	1.00
24	105.2	121.5	56.37	5.64	2.82	1.88	1.41	1.13	0.94
25	100.8	111.3	52.90	5.29	2.65	1.76	1.32	1.06	0.88
26	96.8	102.4	49.76	4.98	2.49	1.66	1.24	1.00	0.83
27	93.1	94.5	46.90	4.69	2.34	1.56	1.17	0.94	0.78
28	89.7	87.4	44.28	4.43	2.21	1.48	1.11	0.89	0.74
29	86.5	81.2	41.88	4.19	2.09	1.40	1.05	0.84	0.70
30	83.6	75.6	39.68	3.97	1.98	1.32	0.99	0.79	0.66
31	80.8	70.5	37.65	3.77	1.88	1.26	0.94	0.75	0.63
32	78.2	65.9	35.78	3.58	1.79	1.19	0.89	0.72	0.60
33	75.8	61.8	34.04	3.40	1.70	1.13	0.85	0.68	0.57
34	73.5	58.1	32.43	3.24	1.62	1.08	0.81	0.65	0.54
35	71.4	54.6	30.94	3.09	1.55	1.03	0.77	0.62	0.52
36	69.3	51.5	29.55	2.95	1.48	0.98	0.74	0.59	0.49
37	67.4	48.6	28.25	2.82	1.41	0.94	0.71	0.56	0.47
38	65.6	46.0	27.04	2.70	1.35	0.90	0.68	0.54	0.45
39	63.9	43.6	25.90	2.59	1.30	0.86	0.65	0.52	0.43
40	62.3	41.3	24.84	2.48	1.24	0.83	0.62	0.50	0.41
41	60.7	39.3	23.84	2.38	1.19	0.79	0.60	0.48	0.40
42	59.2	37.3	22.90	2.29	1.15	0.76	0.57	0.46	0.38
43	57.8	35.6	22.02	2.20	1.10	0.73	0.55	0.44	0.37
44	56.5	33.9	21.18	2.12	1.06	0.71	0.53	0.42	0.35
45	55.2	32.4	20.40	2.04	1.02	0.68	0.51	0.41	0.34
46	54.0	30.9	19.66	1.97	0.98	0.66	0.49	0.39	0.33
47	52.8	29.6	18.96	1.90	0.95	0.63	0.47	0.38	0.32
48	51.7	28.3	18.29	1.83	0.91	0.61	0.46	0.37	0.30
49	50.6	27.1	17.66	1.77	0.88	0.59	0.44	0.35	0.29
50	49.6	26.0	17.06	1.71	0.85	0.57	0.43	0.34	0.28

Notes:  
 PCB Thickness = 62 mils  
 Plating Thickness = 0.8 mils  
 Plating Thermal Conductivity = 3.98 W/cm°C  
 Fill Conductivity = 0.51 W/cm°C

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**Table 8: Thermal Resistance of Solder Filled, Plated Through Via Hole - 1 mil Plating Thickness**

Via Dia (Mils)	Thermal Resistance (C/Watt)			Multiple Vias					
	Plating	Fill	Combined	10	20	30	40	50	60
10	216.9	952.2	176.67	17.67	8.83	5.89	4.42	3.53	2.94
11	195.2	752.3	155.00	15.50	7.75	5.17	3.88	3.10	2.58
12	177.5	609.4	137.45	13.74	6.87	4.58	3.44	2.75	2.29
13	162.7	503.6	122.96	12.30	6.15	4.10	3.07	2.46	2.05
14	150.2	423.2	110.84	11.08	5.54	3.69	2.77	2.22	1.85
15	139.4	360.6	100.56	10.06	5.03	3.35	2.51	2.01	1.68
16	130.1	310.9	91.74	9.17	4.59	3.06	2.29	1.83	1.53
17	122.0	270.8	84.12	8.41	4.21	2.80	2.10	1.68	1.40
18	114.8	238.0	77.47	7.75	3.87	2.58	1.94	1.55	1.29
19	108.5	210.9	71.62	7.16	3.58	2.39	1.79	1.43	1.19
20	102.7	188.1	66.45	6.64	3.32	2.21	1.66	1.33	1.11
21	97.6	168.8	61.85	6.18	3.09	2.06	1.55	1.24	1.03
22	93.0	152.3	57.73	5.77	2.89	1.92	1.44	1.15	0.96
23	88.7	138.2	54.04	5.40	2.70	1.80	1.35	1.08	0.90
24	84.9	125.9	50.70	5.07	2.53	1.69	1.27	1.01	0.84
25	81.3	115.2	47.68	4.77	2.38	1.59	1.19	0.95	0.79
26	78.1	105.8	44.93	4.49	2.25	1.50	1.12	0.90	0.75
27	75.1	97.5	42.42	4.24	2.12	1.41	1.06	0.85	0.71
28	72.3	90.1	40.12	4.01	2.01	1.34	1.00	0.80	0.67
29	69.7	83.6	38.01	3.80	1.90	1.27	0.95	0.76	0.63
30	67.3	77.7	36.07	3.61	1.80	1.20	0.90	0.72	0.60
31	65.1	72.5	34.28	3.43	1.71	1.14	0.86	0.69	0.57
32	63.0	67.7	32.63	3.26	1.63	1.09	0.82	0.65	0.54
33	61.0	63.4	31.09	3.11	1.55	1.04	0.78	0.62	0.52
34	59.2	59.5	29.67	2.97	1.48	0.99	0.74	0.59	0.49
35	57.4	56.0	28.34	2.83	1.42	0.94	0.71	0.57	0.47
36	55.8	52.7	27.10	2.71	1.36	0.90	0.68	0.54	0.45
37	54.2	49.7	25.95	2.59	1.30	0.86	0.65	0.52	0.43
38	52.8	47.0	24.86	2.49	1.24	0.83	0.62	0.50	0.41
39	51.4	44.5	23.85	2.38	1.19	0.79	0.60	0.48	0.40
40	50.1	42.2	22.90	2.29	1.14	0.76	0.57	0.46	0.38
41	48.8	40.1	22.00	2.20	1.10	0.73	0.55	0.44	0.37
42	47.6	38.1	21.16	2.12	1.06	0.71	0.53	0.42	0.35
43	46.5	36.3	20.37	2.04	1.02	0.68	0.51	0.41	0.34
44	45.4	34.5	19.62	1.96	.998	0.65	0.49	0.39	0.33
45	44.4	33.0	18.91	1.89	0.95	0.63	0.47	0.38	0.32
46	43.4	31.5	18.24	1.82	0.91	0.61	0.46	0.36	0.30
47	42.4	30.1	17.61	1.76	0.88	0.59	0.44	0.35	0.29
48	41.5	28.8	17.01	1.70	0.85	0.57	0.43	0.34	0.28
49	40.7	27.6	16.44	1.64	0.82	0.55	0.41	0.33	0.27
50	39.8	26.4	15.90	1.59	0.79	0.53	0.40	0.32	0.26

*Notes:*

*PCB Thickness = 62 mils*

*Plating Thickness = 1 mil*

*Plating Thermal Conductivity = 3.98 W/cm°C*

*Fill Conductivity = 0.51 W/cm°C*

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Table 9: Thermal Resistance of Solder Filled, Plated Through Via Hole - 2 mil Plating Thickness

Via Dia (Mils)	Thermal Resistance (C/Watt)			Multiple Vias					
	Plating	Fill	Combined	10	20	30	40	50	60
10	122.0	1692.8	113.81	11.38	5.69	3.79	2.85	2.28	1.90
11	1.08.5	1243.7	99.76	9.98	4.99	3.33	2.49	2.00	1.66
12	97.6	952.2	88.53	8.85	4.43	2.95	2.21	1.77	1.48
13	88.7	752.3	79.37	7.94	3.97	2.65	1.98	1.59	1.32
14	81.3	609.4	71.76	7.18	3.59	2.39	1.79	1.44	1.20
15	75.1	503.6	65.34	6.53	3.27	2.18	1.63	1.31	1.09
16	69.7	423.2	59.86	5.99	2.99	2.00	1.50	1.20	1.00
17	65.1	360.6	55.13	5.51	2.76	1.84	1.38	1.10	0.92
18	61.0	310.9	51.00	5.10	2.55	1.70	1.27	1.02	0.85
19	57.4	270.8	47.37	4.74	2.37	1.58	1.18	0.95	0.79
20	54.2	238.0	44.17	4.42	2.21	1.47	1.10	0.88	0.74
21	51.4	210.9	41.31	4.13	2.07	1.38	1.03	0.83	0.69
22	48.8	188.1	38.75	3.88	1.94	1.29	0.97	0.78	0.65
23	46.5	168.8	36.45	3.64	1.82	1.21	0.91	0.73	0.61
24	44.4	152.3	34.36	3.44	1.72	1.15	0.86	0.69	0.57
25	42.4	138.2	32.47	3.25	1.62	1.08	0.81	0.65	0.54
26	40.7	125.9	30.74	3.07	1.54	1.02	0.77	0.61	0.51
27	39.0	115.2	29.16	2.92	1.46	0.97	0.73	0.58	0.49
28	37.5	105.8	27.71	2.77	1.39	0.92	0.69	0.55	0.46
29	36.2	97.5	26.37	2.64	1.32	0.88	0.66	0.53	0.44
30	34.9	90.1	25.14	2.51	1.26	0.84	0.63	0.50	0.42
31	33.7	83.6	24.00	2.40	1.20	0.80	0.60	0.48	0.40
32	32.5	77.7	22.94	2.29	1.15	0.76	0.57	0.46	0.38
33	31.5	72.5	21.95	2.19	1.10	0.73	0.55	0.44	0.37
34	30.5	67.7	21.03	2.10	1.05	0.70	0.53	0.42	0.35
35	29.6	63.4	20.17	2.02	1.01	0.67	0.50	0.40	0.34
36	28.7	59.5	19.37	1.94	0.97	0.65	0.48	0.39	0.32
37	27.9	56.0	18.61	1.86	0.93	0.62	0.47	0.37	0.31
38	27.1	52.7	17.90	1.79	0.90	0.60	0.45	0.36	0.30
39	26.4	49.7	17.24	1.72	0.86	0.57	0.43	0.34	0.29
40	25.7	47.0	16.61	1.66	0.83	0.55	0.42	0.33	.028
41	25.0	44.5	16.02	1.60	0.80	0.53	0.40	0.32	0.27
42	24.4	42.2	15.46	1.55	0.77	0.52	0.39	0.31	0.26
43	23.8	40.1	14.93	1.49	0.75	0.50	0.37	0.30	0.25
44	23.2	38.1	14.43	1.44	0.72	0.48	0.36	0.29	0.24
45	22.7	36.3	13.96	1.40	0.70	0.47	0.35	0.28	0.23
46	22.2	34.5	13.51	1.35	0.68	0.45	0.34	0.27	0.23
47	21.7	33.0	13.08	1.31	0.65	0.44	0.33	0.26	0.22
48	21.2	31.5	12.67	1.27	0.63	0.42	0.32	0.25	0.21
49	20.8	30.1	12.29	1.23	0.61	0.41	0.31	0.25	0.20
50	20.3	28.8	11.92	1.19	0.60	0.40	0.30	0.24	0.20

Notes:

PCB Thickness = 62 mils

Plating Thickness = 2 mils

Plating Thermal Conductivity = 3.98 W/cm°C

Fill Conductivity = 0.51 W/cm°C

## ACA0861 - A, B, C, D 750/860 MHz CATV Line Amplifiers

### PRECAUTIONS

The following precautions are easily implemented and will assure a quality, high reliability product.

#### ESD

The ACA0861 contains very high frequency transistors inside the package. These transistors, like all high-speed transistors, are susceptible to damage by ESD. Currently, the ACA0861 can be damaged with ESD voltages greater than +/- 250 Volts. To avoid damage to the devices by ESD, take the following precautions:

1. Always wear an ESD wrist strap when handling the devices. This is good practice when handling any electronic device.
2. Limit the exposure to ESD during storage and mounting by using proper ESD handling and storage techniques.

#### Transients on the Bias Lines

The ACA0861 amplifiers can be damaged by large voltage transients on the DC bias lines. These transients can be generated by suddenly connecting, shorting, or disconnecting the DC bias to the devices. This causes a rapid change in the supply current and results in very large voltage transients on the DC bias lines. This is mainly due to the rapid change in current through the circuit inductance ( $v = L \cdot di/dt$ ). To reduce voltage transients, take the following precaution:

The addition of a Transient Voltage Suppressor (TVS) on the DC bias line. This part should be located between the location of the power supply discontinuity and the device, the closer to the device the better. A part should be selected with a nominal breakdown voltage of 15VDC. The 500W Series SAXX TVS from GI may work for this application. A surface mount version is also available from GI, series SMBG TVS or SMBJ TVS. The use of a TVS is required if DC bias discontinuities are expected. The use of TVS and the bias line decoupling capacitors will prevent voltage transients from damaging the devices.

When using multiple ACA0861 devices in a single design, a single TVS can be used to protect all the

devices if the placement of the TVS is between the DC bias discontinuity and the devices.

#### Transients at the RF Outputs

The ACA series of Line Amplifiers can be damaged by large voltage transients appearing at the output of the device. These transients can be the result of lightning, ESD, and other phenomenon. A simple PIN diode circuit added to the output of the D stage device offers greatly improved protection to the devices.

The protection circuit consists of two PIN diodes placed across the RF outputs, as shown in Figure 8. A DC return choke is required on the through port of the balun. The circuit operation is as follows: Both PIN diodes are reverse biased by the 12 VDC bias voltage appearing at the RF output pins of the devices. When negative transient voltage levels exceed -12 Volts the diode will become forward biased and current will flow through the PIN diode. When current is being conducted in the diode the resistance of the diode is reduced. This "shorts" the two RF outputs together. Since the RF outputs are 180 degrees out of phase the transient signal is cancelled. This does not effect the normal operation of the device since the normal RF output voltage levels do not exceed 12 volts.

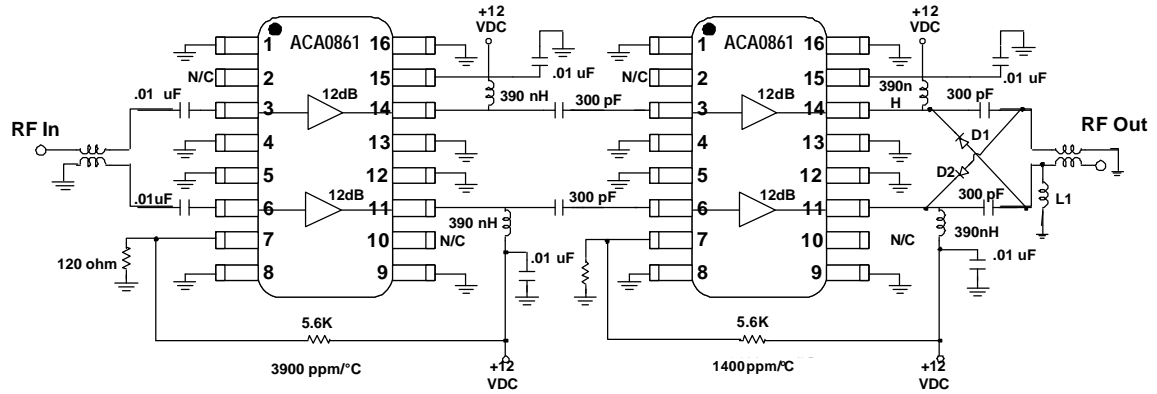
#### Mounting

These devices are high power dissipation surface mount components and require a well-designed thermal mount. All the heat generated by the device is expected to be removed through the bottom heat slug with a low thermal resistance path to the chassis.

### CONCLUSION

A new, and quite different, approach is now available for CATV design engineers. This approach allows for new and creative designs that outperform the present CATV hybrids at a lower overall cost for both the hybrid and assembly which add up to a substantial overall cost savings. The package allows the fully automated assembly and positions companies for expanding bandwidths up to and beyond 2 GHz.

### ACA0861 - A, B, C, D 750/860 MHz CATV Line Amplifiers



Notes:  
 D1 and D2 are PIN SMP – 1320-011. (Alpha Industries)  
 L1 is used as a DC return for D1

**Figure 8: Power Doubler with Surge Suppression Circuit**

**ACA0861 - A, B, C, D 750/860 MHz CATV Line Amplifiers**

**NOTES**

NOTES

## ACA0861 - A, B, C, D 750/860 MHz CATV Line Amplifiers



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