

# 40MX and 42MX FPGA Families

## Features

### High Capacity

- Single-Chip ASIC Alternative
- 3,000 to 54,000 System Gates
- Up to 2.5 kbits Configurable Dual-Port SRAM
- Fast Wide-Decode Circuitry
- Up to 202 User-Programmable I/O Pins

### High Performance

- 5.6 ns Clock-to-Out
- 250 MHz Performance
- 5 ns Dual-Port SRAM Access
- 100 MHz FIFOs
- 7.5 ns 35-Bit Address Decode

### HiRel Features

- Commercial, Industrial, and Military Temperature Plastic Packages

- Commercial, Military Temperature and MIL-STD-883 Ceramic Packages

- QML Certification

- Ceramic Devices Available to DSCC SMD

### Ease of Integration

- Mixed Voltage Operation (5.0V or 3.3V I/O)
- Synthesis-Friendly Architecture to Support ASIC Design Methodologies
- Up to 100% Resource Utilization and 100% Pin Fixing
- Deterministic, User-Controllable Timing
- Unique In-System Diagnostic and Verification Capability with Silicon Explorer II
- Low Power Consumption
- IEEE Standard 1149.1 (JTAG) Boundary Scan Testing
- 5.0V and 3.3V Programmable PCI-Compliant I/O

## Product Profile

| Device                             | A40MX02 | A40MX04    | A42MX09  | A42MX16       | A42MX24  | A42MX36  |
|------------------------------------|---------|------------|----------|---------------|----------|----------|
| <b>Capacity</b>                    |         |            |          |               |          |          |
| System Gates                       | 3,000   | 6,000      | 14,000   | 24,000        | 36,000   | 54,000   |
| SRAM Bits                          | N/A     | N/A        | N/A      | N/A           | N/A      | 2,560    |
| <b>Logic Modules</b>               |         |            |          |               |          |          |
| Sequential                         | —       | —          | 348      | 624           | 954      | 1,230    |
| Combinatorial                      | 295     | 547        | 336      | 608           | 912      | 1,184    |
| Decode                             | —       | —          | N/A      | N/A           | 24       | 24       |
| <b>Clock-to-Out</b>                | 9.5 ns  | 9.5 ns     | 5.6 ns   | 6.1 ns        | 6.1 ns   | 6.3 ns   |
| <b>SRAM Modules (64x4 or 32x8)</b> | N/A     | N/A        | N/A      | N/A           | N/A      | 10       |
| <b>Dedicated Flip-Flops</b>        | —       | —          | 348      | 624           | 954      | 1,230    |
| <b>Maximum Flip-Flops</b>          | 147     | 273        | 516      | 928           | 1,410    | 1,822    |
| <b>Clocks</b>                      | 1       | 1          | 2        | 2             | 2        | 6        |
| <b>User I/O (Maximum)</b>          | 57      | 69         | 104      | 140           | 176      | 202      |
| <b>PCI</b>                         | No      | No         | No       | No            | Yes      | Yes      |
| <b>Boundary Scan Test (BST)</b>    | No      | No         | No       | No            | Yes      | Yes      |
| <b>Packages (by pin count)</b>     |         |            |          |               |          |          |
| PLCC                               | 44, 68  | 44, 68, 84 | 84       | 84            | 84       | —        |
| PQFP                               | 100     | 100        | 100, 160 | 100, 160, 208 | 160, 208 | 208, 240 |
| VQFP                               | 80      | 80         | 100      | 100           | —        | —        |
| TQFP                               | —       | —          | 176      | 176           | 176      | —        |
| CQFP                               | —       | —          | —        | —             | —        | 208, 256 |
| PBGA                               | —       | —          | —        | —             | —        | 272      |

## General Description

Actel's 40MX and 42MX families provide a high-performance, single-chip solution for shortening the system design and development cycle, offering a cost-effective alternative to ASICs. The 40MX and 42MX devices are excellent choices for integrating logic that is currently implemented in multiple PALs, CPLDs, and FPGAs. Example applications include high-speed controllers and address decoding, peripheral bus interfaces, DSP, and co-processor functions.

The MX device architecture is based on Actel's patented antifuse technology implemented in a 0.45µ triple-metal CMOS process. With capacities ranging from 3,000 to 54,000 system gates, the synthesis-friendly MX devices provide performance up to 250 MHz, are live on power-up, and require up to five times lower stand-by power consumption than any other FPGA device. Actel's MX FPGAs provide up to 202 user I/Os and are available in a wide variety of packages and speed grades.

Actel's 42MX devices also feature MultiPlex I/Os, which support mixed voltage systems, enable programmable PCI, deliver high-performance operation at both 5.0V and 3.3V, and provide a low-power mode.

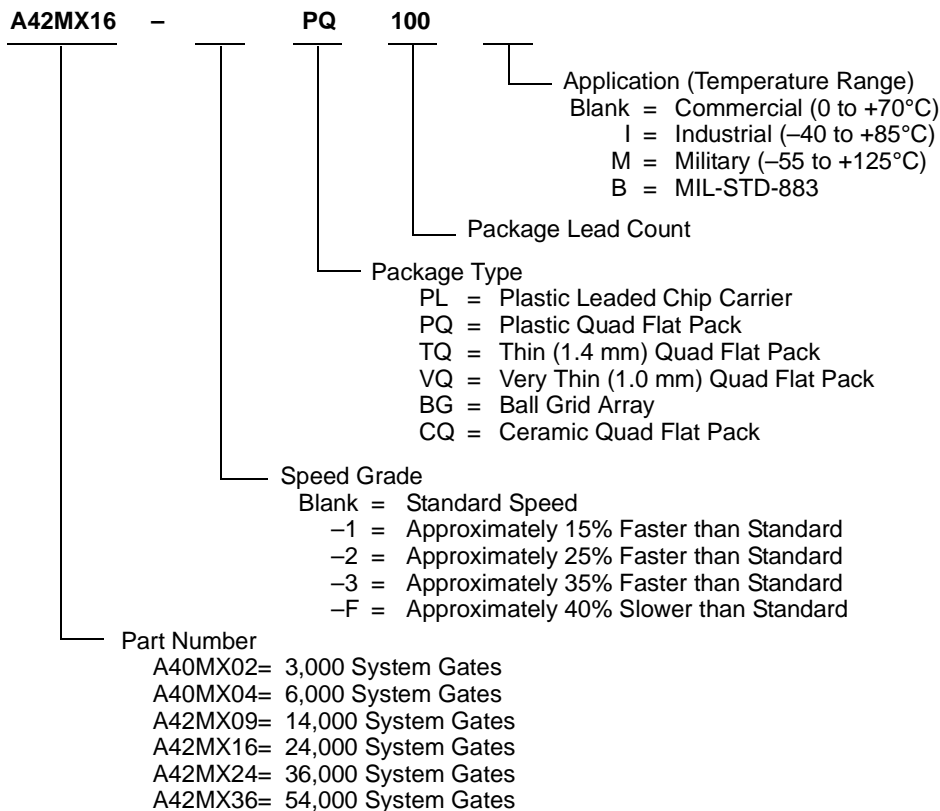
The MX PCI-Compliant devices are fully compliant with the PCI Local Bus Specification (version 2.1). They deliver 200

MHz on-chip operation and 6.1 ns clock-to-output performance with capacities spanning from 36,000 to 54,000 system gates. MX devices comply 100 percent to the electrical and timing specifications detailed in the PCI specification. However, as with all programmable logic devices, the performance of the final product depends upon the user's design and optimization techniques.

The MX24 and MX36 devices also include system-level features such as IEEE Standard 1149.1 (JTAG) Boundary Scan Testing, dual-port SRAM, and fast wide-decode modules. The A42MX36 device offers dual-port SRAM for implementing fast FIFOs, LIFOs, and temporary data storage. The large number of storage elements can efficiently address applications requiring wide datapath manipulation and can perform transformation functions such as those required for telecommunications, networking, and DSP.

All products in the 40MX and 42MX families are available 100 percent tested over the military temperature range. In addition, the largest member of the family, the A42MX36, is available in both CQ208 and CQ256 ceramic packages screened to MIL-STD-883 levels. For easy prototyping and conversion from plastic to ceramic, the CQ208 and PQ208 devices are pin compatible.

## Ordering Information



**Product Plan**

|   | Speed Grade* |    |    |    |    | Application |   |   |   |
|---|--------------|----|----|----|----|-------------|---|---|---|
|   | Std          | -1 | -2 | -3 | -F | C†          | I | M | B |
| <b>A40MX02 Device</b>                           |              |    |    |    |    |             |   |   |   |
| 44-Pin Plastic Leaded Chip Carrier (PLCC)       | ✓            | ✓  | ✓  | ✓  | ✓  | ✓           | ✓ | ✓ | — |
| 68-Pin Plastic Leaded Chip Carrier (PLCC)       | ✓            | ✓  | ✓  | ✓  | ✓  | ✓           | ✓ | ✓ | — |
| 100-Pin Plastic Quad Flat Pack (PQFP)           | ✓            | ✓  | ✓  | ✓  | ✓  | ✓           | ✓ | ✓ | — |
| 80-Pin Very Thin Plastic Quad Flat Pack (VQFP)  | ✓            | ✓  | ✓  | ✓  | ✓  | ✓           | ✓ | ✓ | — |
| <b>A40MX04 Device</b>                           |              |    |    |    |    |             |   |   |   |
| 44-Pin Plastic Leaded Chip Carrier (PLCC)       | ✓            | ✓  | ✓  | ✓  | ✓  | ✓           | ✓ | ✓ | — |
| 68-Pin Plastic Leaded Chip Carrier (PLCC)       | ✓            | ✓  | ✓  | ✓  | ✓  | ✓           | ✓ | ✓ | — |
| 84-Pin Plastic Leaded Chip Carrier (PLCC)       | ✓            | ✓  | ✓  | ✓  | ✓  | ✓           | ✓ | ✓ | — |
| 100-Pin Plastic Quad Flat Pack (PQFP)           | ✓            | ✓  | ✓  | ✓  | ✓  | ✓           | ✓ | ✓ | — |
| 80-Pin Very Thin Plastic Quad Flat Pack (VQFP)  | ✓            | ✓  | ✓  | ✓  | ✓  | ✓           | ✓ | ✓ | — |
| <b>A42MX09 Device</b>                           |              |    |    |    |    |             |   |   |   |
| 84-Pin Plastic Leaded Chip Carrier (PLCC)       | ✓            | ✓  | ✓  | ✓  | ✓  | ✓           | ✓ | ✓ | — |
| 100-Pin Plastic Quad Flat Pack (PQFP)           | ✓            | ✓  | ✓  | ✓  | ✓  | ✓           | ✓ | ✓ | — |
| 160-Pin Plastic Quad Flat Pack (PQFP)           | ✓            | ✓  | ✓  | ✓  | ✓  | ✓           | ✓ | ✓ | — |
| 176-Pin Thin Plastic Quad Flat Pack (TQFP)      | ✓            | ✓  | ✓  | ✓  | ✓  | ✓           | ✓ | ✓ | — |
| 100-Pin Very Thin Plastic Quad Flat Pack (VQFP) | ✓            | ✓  | ✓  | ✓  | ✓  | ✓           | ✓ | ✓ | — |
| <b>A42MX16 Device</b>                           |              |    |    |    |    |             |   |   |   |
| 84-Pin Plastic Leaded Chip Carrier (PLCC)       | ✓            | ✓  | ✓  | ✓  | ✓  | ✓           | ✓ | ✓ | — |
| 100-Pin Plastic Quad Flat Pack (PQFP)           | ✓            | ✓  | ✓  | ✓  | ✓  | ✓           | ✓ | ✓ | — |
| 160-Pin Plastic Quad Flat Pack (PQFP)           | ✓            | ✓  | ✓  | ✓  | ✓  | ✓           | ✓ | ✓ | — |
| 208-Pin Plastic Quad Flat Pack (PQFP)           | ✓            | ✓  | ✓  | ✓  | ✓  | ✓           | ✓ | ✓ | — |
| 176-Pin Thin Plastic Quad Flat Pack (TQFP)      | ✓            | ✓  | ✓  | ✓  | ✓  | ✓           | ✓ | ✓ | — |
| 100-Pin Very Thin Plastic Quad Flat Pack (VQFP) | ✓            | ✓  | ✓  | ✓  | ✓  | ✓           | ✓ | ✓ | — |
| <b>A42MX24 Device</b>                           |              |    |    |    |    |             |   |   |   |
| 84-Pin Plastic Leaded Chip Carrier (PLCC)       | ✓            | ✓  | ✓  | ✓  | ✓  | ✓           | ✓ | ✓ | — |
| 160-Pin Plastic Quad Flat Pack (PQFP)           | ✓            | ✓  | ✓  | ✓  | ✓  | ✓           | ✓ | ✓ | — |
| 208-Pin Plastic Quad Flat Pack (PQFP)           | ✓            | ✓  | ✓  | ✓  | ✓  | ✓           | ✓ | ✓ | — |
| 176-Pin Thin Plastic Quad Flat Pack (TQFP)      | ✓            | ✓  | ✓  | ✓  | ✓  | ✓           | ✓ | ✓ | — |
| <b>A42MX36 Device</b>                           |              |    |    |    |    |             |   |   |   |
| 208-Pin Plastic Quad Flat Pack (PQFP)           | ✓            | ✓  | ✓  | ✓  | ✓  | ✓           | ✓ | ✓ | — |
| 240-Pin Plastic Quad Flat Pack (PQFP)           | ✓            | ✓  | ✓  | ✓  | ✓  | ✓           | ✓ | ✓ | — |
| 272-Pin Plastic Ball Grid Array (PBGA)          | ✓            | ✓  | ✓  | ✓  | ✓  | ✓           | ✓ | ✓ | — |
| 208-Pin Ceramic Quad Flat Pack (CQFP)           | ✓            | ✓  | ✓  | —  | —  | ✓           | — | ✓ | ✓ |
| 256-Pin Ceramic Quad Flat Pack (CQFP)           | ✓            | ✓  | ✓  | —  | —  | ✓           | — | ✓ | ✓ |

Contact your Actel sales representative for product availability.

Applications: C = Commercial    Availability: ✓ = Available  
 I = Industrial                      P = Planned  
 M = Military                        — = Not Planned

\*Speed Grade: -1 = Approx. 15% faster than Standard  
 -2 = Approx. 25% faster than Standard  
 -3 = Approx. 35% faster than Standard  
 -F = Approx. 40% slower than Standard

† Only Std, -1, -2 Speed Grade  
 • Only Std, -1 Speed Grade

## Development Tool Support

The MX devices are fully supported by Actel's line of FPGA development tools, including the Actel DeskTOP series and Designer Series tools. The Actel DeskTOP series is an integrated design environment for PCs that includes design entry, simulation, synthesis, and place-and-route tools. Designer Series, Actel's suite of FPGA development point tools for PCs and Workstations, includes the ACTgen Macro Builder, timing-driven place-and-route and analysis tools, and device programming software.

In addition, the MX devices contain ActionProbe circuitry that provides built-in access to every node in a design,

enabling 100 percent real-time observation and analysis of a device's internal logic nodes without design iteration. The probe circuitry is accessed by Silicon Explorer II, an easy-to-use integrated verification and logic analysis tool that can sample data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to only a few seconds.

## Plastic Device Resources

| Device  | User I/Os      |                |                |                 |                 |                 |                 |                |                 |                 |                 |
|---------|----------------|----------------|----------------|-----------------|-----------------|-----------------|-----------------|----------------|-----------------|-----------------|-----------------|
|         | PLCC<br>44-Pin | PLCC<br>68-Pin | PLCC<br>84-Pin | PQFP<br>100-Pin | PQFP<br>160-Pin | PQFP<br>208-Pin | PQFP<br>240-Pin | VQFP<br>80-Pin | VQFP<br>100-Pin | TQFP<br>176-Pin | PBGA<br>272-Pin |
| A40MX02 | 34             | 57             | —              | 57              | —               | —               | —               | 57             | —               | —               | —               |
| A40MX04 | 34             | 57             | 69             | 69              | —               | —               | —               | 69             | —               | —               | —               |
| A42MX09 | —              | —              | 72             | 83              | 101             | —               | —               | —              | 83              | 104             | —               |
| A42MX16 | —              | —              | 72             | 83              | 125             | 140             | —               | —              | 83              | 140             | —               |
| A42MX24 | —              | —              | 72             | —               | 125             | 176             | —               | —              | —               | 150             | —               |
| A42MX36 | —              | —              | —              | —               | —               | 176             | 202             | —              | —               | —               | 202             |

**Package Definitions** (Contact your Actel sales representative for product availability.)

PLCC = Plastic Leaded Chip Carrier, PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, VQFP = Very Thin Quad Flat Pack, PBGA = Plastic Ball Grid Array

## Ceramic Device Resources

| Device  | User I/Os       |                 |
|---------|-----------------|-----------------|
|         | CQFP<br>208-Pin | CQFP<br>256-Pin |
| A42MX36 | 176             | 202             |

**Package Definitions** (Contact your Actel sales representative for product availability.)

CQFP = Ceramic Quad Flat Pack

## Power Requirements

### 40MX

The 40MX FPGAs will operate in 5.0V-only systems or 3.3V-only systems.

| $V_{CC}$ | Input | Output |
|----------|-------|--------|
| 5.0V     | 5.0V  | 5.0V   |
| 3.3V     | 3.3V  | 3.3V   |

### 42MX

The 42MX FPGAs will operate in 5.0V-only systems, 3.3V-only systems, or mixed 5.0V/3.3V systems.

| $V_{CCA}$ | $V_{CCI}$ | Input      | Output |
|-----------|-----------|------------|--------|
| 5.0V      | 5.0V      | 5.0V       | 5.0V   |
| 3.3V      | 3.3V      | 3.3V       | 3.3V   |
| 5.0V      | 3.3V      | 3.3V, 5.0V | 3.3V   |

## Mixed Voltage Power Up and Power Down

When powering up the device in the mixed voltage mode ( $V_{CCA} = 5.0V$  and  $V_{CCI} = 3.3V$ ),  $V_{CCA}$  must be greater than or equal to  $V_{CCI}$  throughout the power-up sequence. If  $V_{CCI}$  is 0.5V greater than  $V_{CCA}$  when both are above 1.5V, then the I/Os' input protection junction on the I/Os will be forward biased, causing them to draw large amounts of current. When  $V_{CCA}$  and  $V_{CCI}$  are in the 1.5V to 2.0V region and  $V_{CCI}$  is greater than  $V_{CCA}$ , all I/Os would momentarily behave as outputs that are in a logical high state, and  $I_{CC}$  rises to high levels. For power down, any sequence with  $V_{CCA}$  and  $V_{CCI}$  can be implemented.

## Low Power Mode

The 42MX devices have a power-saving feature enabled by a special Low Power pin (LP). In this mode, the device consumes very minimal power, with standby current as low as 15 $\mu$ A (see "Electrical Specifications" on page 13 and 14). All  $\mu$  I/Os are tristated, all input buffers are turned off, and the core of the device is turned off. Since the core is turned off, the state of the registers and the contents of the SRAM are lost. The device enters low power mode 800ns after the LP pin is set High. It will resume normal operation 200 $\mu$ s after the LP pin is driven to a logic Low.

## MX Architectural Overview

The 40MX and 42MX devices are composed of fine-grained building blocks that enable fast, efficient logic designs. All devices within these families are composed of logic modules, I/O modules, routing resources, and clock networks, which are the building blocks for designing fast logic designs. In addition, the A42MX36 device contains embedded dual-port SRAM and wide decode modules. The dual-port SRAM modules are optimized for high-speed datapath functions such as FIFOs, LIFOs, and scratchpad memory. The "Product Profile" on page 1 lists the specific logic resources contained within each device.

### Logic Modules

The 40MX logic module is an eight-input, one-output logic circuit designed to implement a wide range of logic functions with efficient use of interconnect routing resources (Figure 1).

The logic module can implement the four basic logic functions (NAND, AND, OR, and NOR) in gates of two, three, or four inputs. Each function may have many versions with different combinations of active LOW inputs. The logic module can also implement a variety of D-latches, exclusivity functions, AND-ORs, and OR-ANDs. No dedicated hard-wired latches or flip-flops are required in the array, since latches and flip-flops can be constructed from logic modules wherever needed in the application.

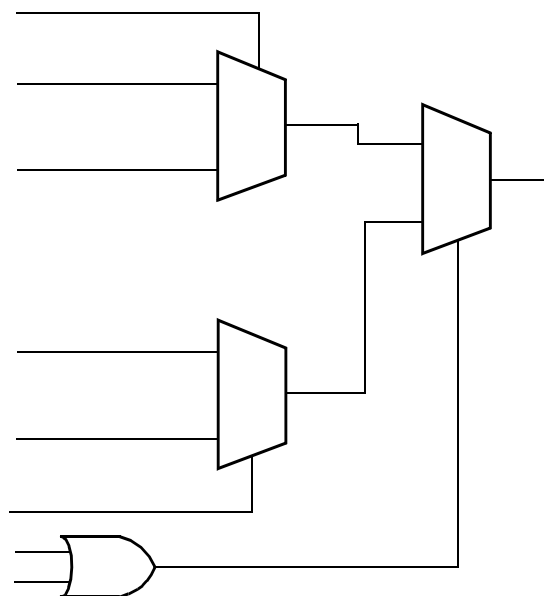


Figure 1 • 40MX Logic Module

The 42MX devices contain three types of logic modules: combinatorial (C-modules), sequential (S-modules), and decode (D-modules).

The C-module, shown in Figure 2, implements the following function:

$$Y = !S1 * !S0 * D00 + !S1 * S0 * D01 + S1 * !S0 * D10 + S1 * S0 * D11$$

where

$$S0 = A0 * B0$$

$$S1 = A1 + B1$$

The S-module, shown in Figure 3, is designed to implement high-speed sequential functions within a single logic module. The S-module implements the same combinatorial logic function as the C-module while adding a sequential element. The sequential element can be configured as either a D flip-flop or a transparent latch. To increase flexibility, the S-module register can be bypassed so that it implements purely combinatorial logic.

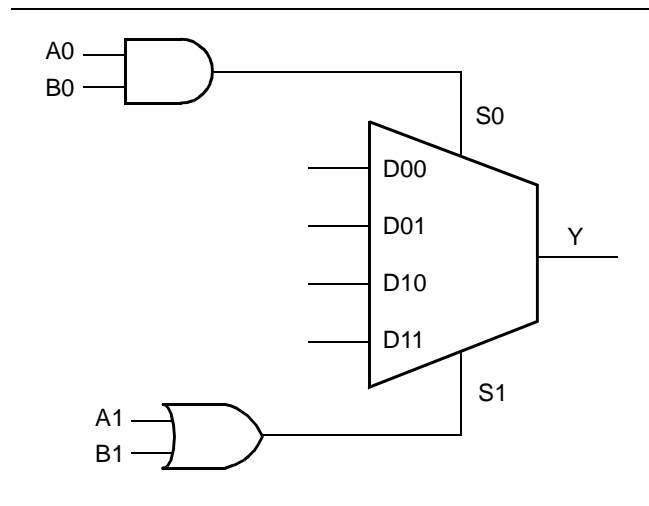


Figure 2 • C-Module Implementation

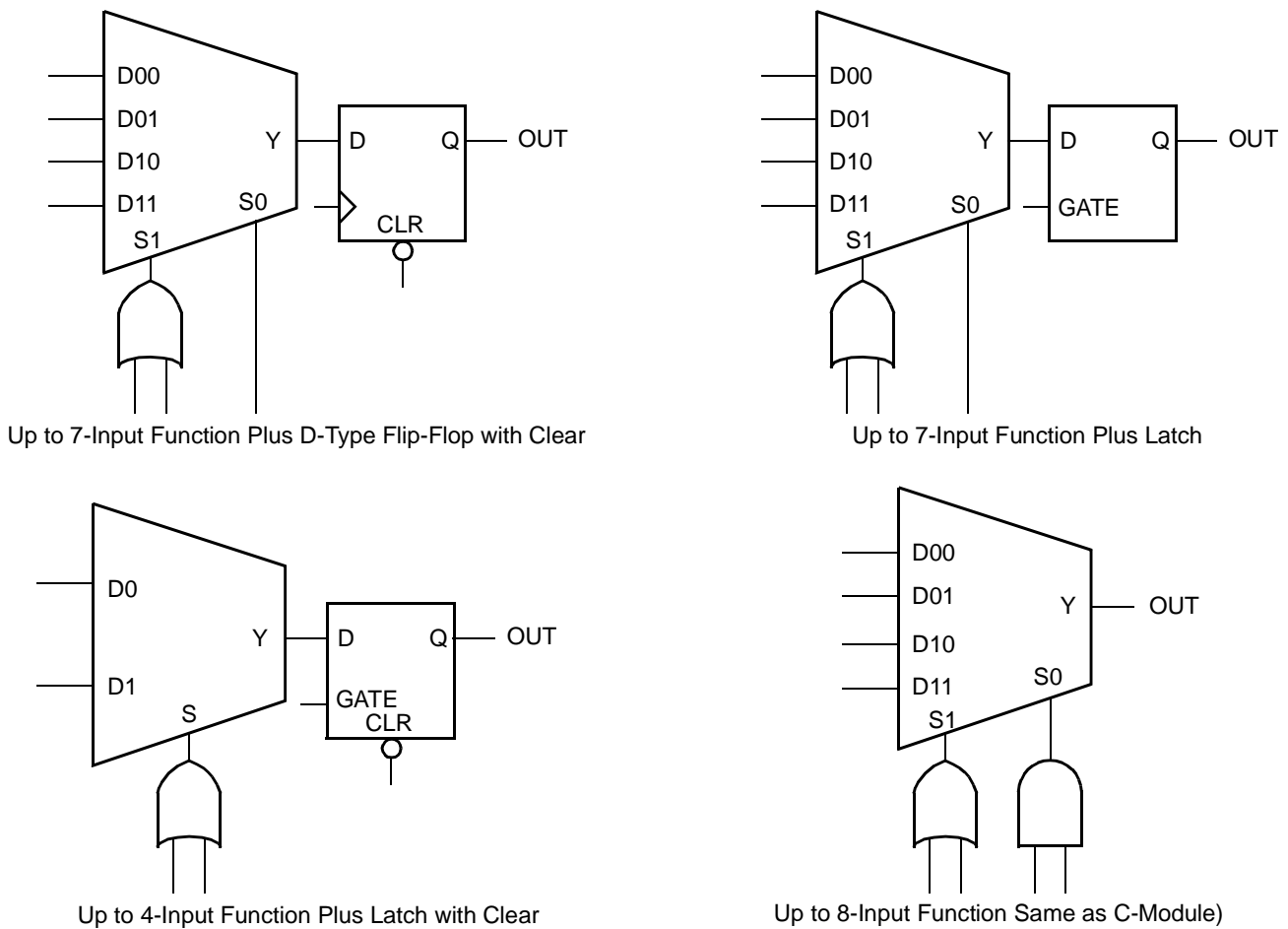


Figure 3 • S-Module Implementation

Some of the 42MX devices contain D-modules, which are arranged around the periphery of the devices. D-modules contain wide-decode circuitry, which provides a fast, wide-input AND function similar to that found in product-term architectures (Figure 4). The D-module allows 42MX devices to perform wide-decode functions at speeds comparable to CPLDs and PALs. The output of the D-module has a programmable inverter for active HIGH or LOW assertion. The D-module output is hard-wired to an output pin, but it can also be fed back into the array to be incorporated into other logic.

**Dual-Port SRAM Modules**

The A42MX36 device contains dual-port SRAM modules that have been optimized for synchronous or asynchronous applications. The SRAM modules are arranged in 256-bit blocks that can be configured as 32x8 or 64x4. SRAM modules can be cascaded together to form memory spaces of user-definable width and depth. A block diagram of the 42MX dual-port SRAM block is shown in Figure 5.

The 42MX SRAM modules are true dual-port structures containing independent read and write ports. Each SRAM module contains six bits of read and write addressing (RDAD[5:0] and WRAD[5:0], respectively) for 64x4-bit blocks. When configured in byte mode, the highest order address bits (RDAD5 and WRAD5) are not used. The read and write ports of the SRAM block contain independent clocks (RCLK and WCLK) with programmable polarities

offering active HIGH or LOW implementation. The SRAM block contains eight data inputs (WD[7:0]), and eight outputs (RD[7:0]) which are connected to segmented vertical routing tracks.

The 42MX dual-port SRAM blocks provide an optimal solution for high-speed buffered applications requiring fast FIFO and LIFO queues. Actel's ACTgen Macro Builder provides the capability to quickly design memory functions, such as FIFOs, LIFOs, and RAM arrays. In addition, unused SRAM blocks can be used to implement registers for other logic within the design.

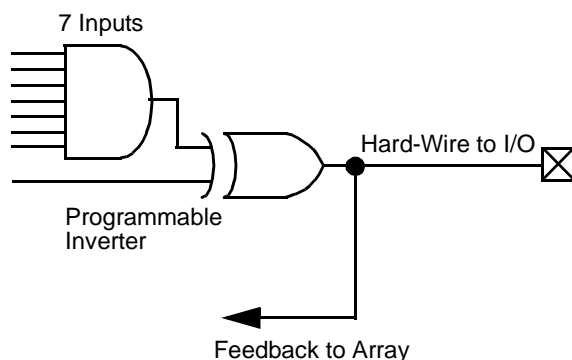


Figure 4 • D-Module Implementation

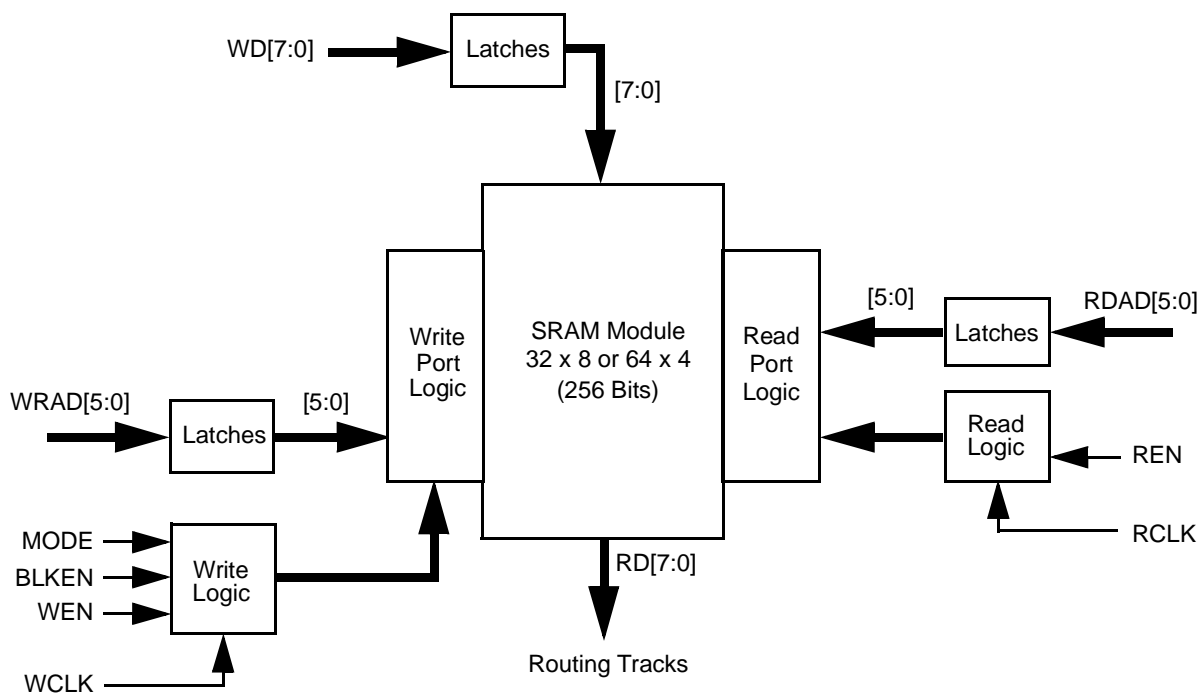


Figure 5 • 42MX Dual-Port SRAM Block

### MultiPlex I/O Modules

MultiPlex I/O supports the most common voltage standards today: pure 5.0V operation, pure 3.3V operation, and mixed 3.3V operation with 5.0V I/O tolerance for maximum performance. Internal array performance is retained in 3.3V systems by using complimentary pass gates that operate as fast as they do at 5.0V at 3.3V.

MultiPlex I/O includes selectable PCI output drives in certain 42MX devices, enabling 100% PCI-compliance for both 5.0V and 3.3V systems. For low-power systems, MultiPlex I/O is used to turn off all inputs and outputs to cut current consumption to below 100µA.

The MultiPlex I/O modules provide the interface between the device pins and the logic array. The top of Figure 6 is a block diagram of the 42MX I/O module. A variety of user functions, determined by a library macro selection, can be implemented in the module. (Refer to the *Macro Library Guide* for more information.) All 42MX I/O modules contain tristate buffers, with input and output latches that can be configured for input, output, or bi-directional operation.

All 42MX devices contain flexible I/O structures (Figure 7 on page 9), where each output pin has a dedicated output-enable control. The I/O module can be used to latch input or output data, or both, providing a fast set-up time. In addition, the Actel Designer Series software tools can build a D-type flip-flop using a C-module to register input and output signals. To achieve 5.0V or 3.3V PCI-compliant output drives on A42MX24 and A42MX36 devices, a chip-wide PCI fuse is programmed. When the PCI fuse is not programmed, the output drive is standard. (See the bottom portion of Figure 6.)

Actel's Designer Series development tools provide a design library of I/O macrofunctions that can implement all I/O configurations supported by the MX FPGAs.

### Routing Structure

The MX architecture uses vertical and horizontal routing tracks to interconnect the various logic and I/O modules. These routing tracks are metal interconnects that may be either of continuous length or broken into pieces called segments. Varying segment lengths allows the interconnect of over 90% of design tracks to occur with only two antifuse connections. Segments can be joined together at the ends using antifuses to increase their lengths up to the full length of the track. All interconnects can be accomplished with a maximum of four antifuses.

### Horizontal Routing

Horizontal channels are located between the rows of modules and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third at the row length is considered a long horizontal segment. A typical channel is shown in Figure 8 on page 9. Non-dedicated horizontal routing tracks are used to route signal nets; dedicated routing tracks are used for global clock networks and for power and ground tie-off tracks.

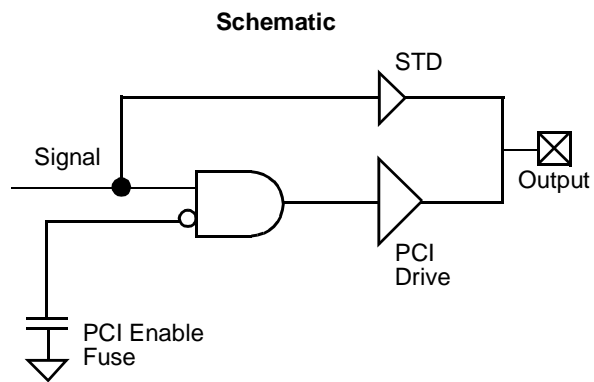
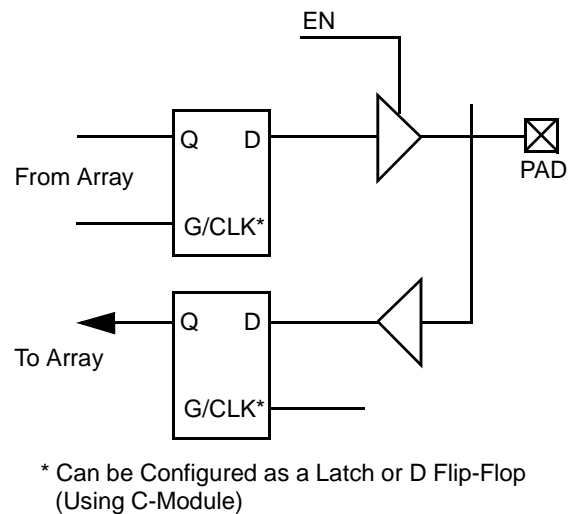


Figure 6 • 42MX I/O Module

### Vertical Routing

Another set of routing tracks run vertically through the module. There are three types of vertical tracks: input, output, and long, which are also divided into one or more segments. Each segment in an input track is dedicated to the input of a particular module; each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during



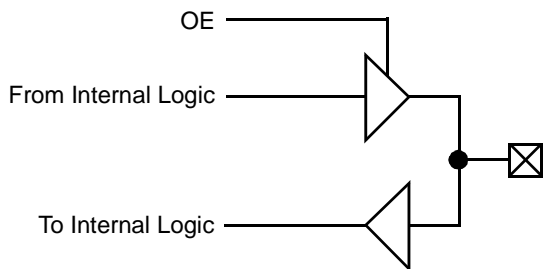


Figure 7 • 40MX I/O Module

routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array, where edge effects occur. Long vertical tracks contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 8.

**Antifuse Structures**

An antifuse is a “normally open” structure as opposed to the normally connected fuse structure used in PROMs or PALs. The use of antifuses to implement a programmable logic device results in highly testable structures as well as efficient programming algorithms. The structure is highly-testable because there are no pre-existing connections; therefore, temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed and individual circuit structures to be tested, which can be done before and after programming. For example, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

**Clock Networks**

The 40MX devices have one global clock distribution network (CLK). Two low-skew, high-fanout clock distribution networks are provided in each 42MX device. These networks are referred to as *CLK0* and *CLK1*. Each network has a clock module (CLKMOD) that selects the source of the clock signal and may be driven as follows:

- Externally from the CLKA pad
- Externally from the CLKB pad
- Internally from the CLKINTA input
- Internally from the CLKINTB input

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel.

The user controls the clock module by selecting one of two clock macros from the macro library. The macro CLKBUF is used to connect one of the two external clock pins to a clock network, and the macro CLKINT is used to connect an

internally-generated clock signal to a clock network. Since both clock networks are identical, it does not matter whether CLK0 or CLK1 is being used. The clock input pads can also be used as normal I/Os, bypassing the clock networks (Figure 9).

The A42MX36 device has four additional register control resources, called quadrant clock networks (Figure 10 on page 10). Each quadrant clock provides a local, high-fanout resource to the contiguous logic modules within its quadrant of the device. Quadrant clock signals can originate from specific I/O pins or from the internal array and can be used as a secondary register clock, register clear, or output enable.

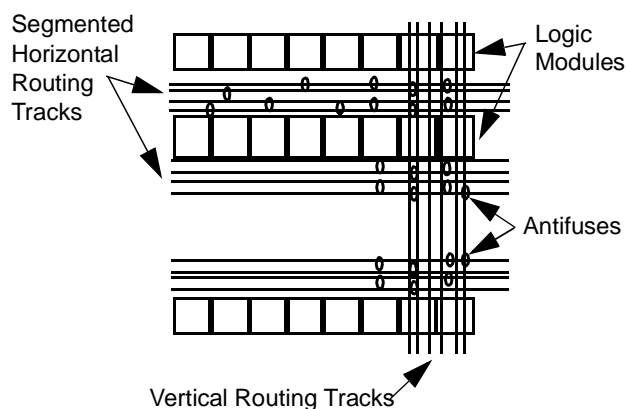


Figure 8 • Routing Structure

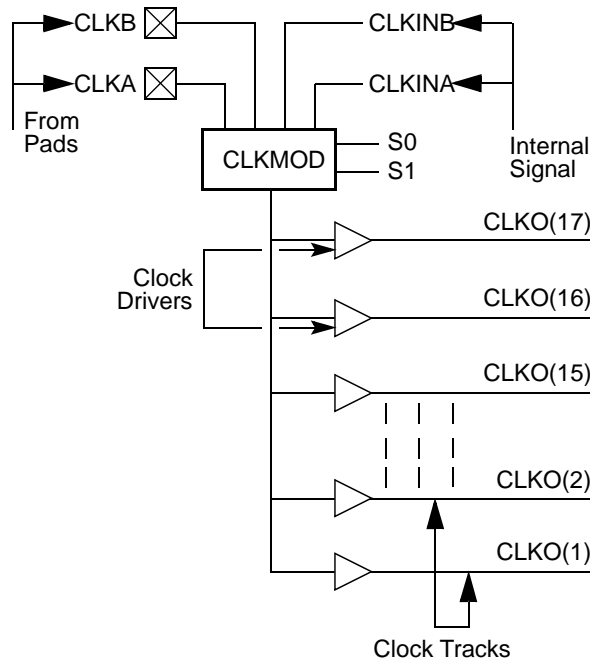


Figure 9 • Clock Networks

**Test Circuitry**

All devices contain Actel's ActionProbe test circuitry which test and debug a design once it is programmed into a device. Once a device has been programmed, the ActionProbe test circuitry allows the designer to probe any internal node during device operation to aid in debugging a design. In addition, 42MX devices contain IEEE Standard 1149.1 boundary scan test circuitry.

**IEEE Standard 1149.1 Boundary Scan Testing (BST)**

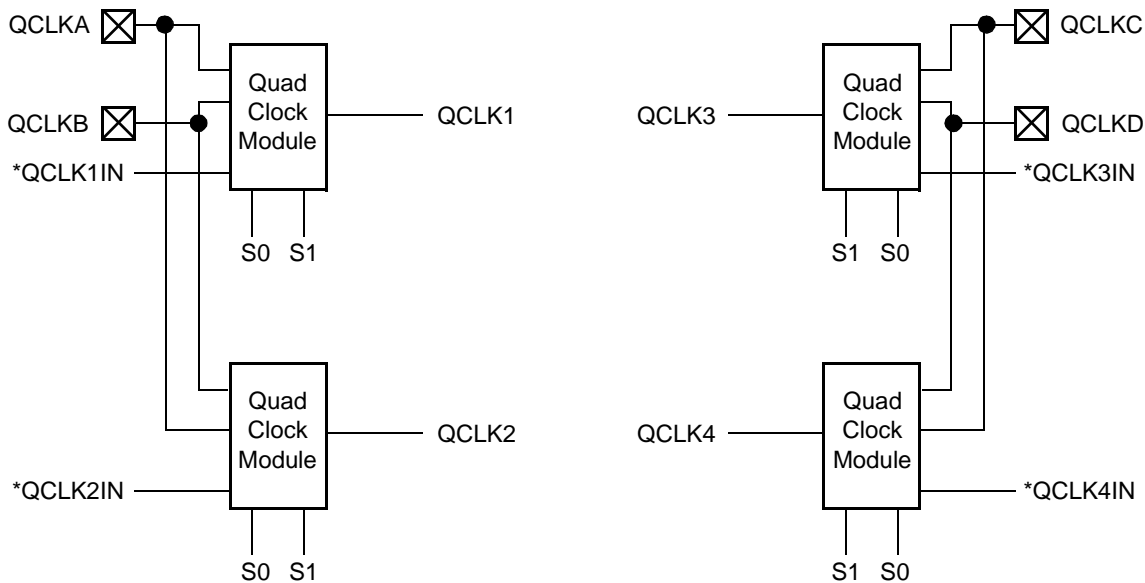
IEEE Standard 1149.1 defines a four-pin Test Access Port (TAP) interface for testing integrated circuits in a system. The 42MX family provides five BST pins: Test Data In (TDI), Test Data Out (TDO), Test Clock (TCK), and Test Mode Select Test Reset (TRST) (42MX24A only). Devices are configured in a test "chain" where BST data can be transmitted serially between devices via TDO-to-TDI

interconnections. The TMS and TCK signals are shared among all devices in the test chain so that all components operate in the same state.

The 42MX family implements a subset of the IEEE Standard 1149.1 BST instruction in addition to a private instruction, which allows the use of Actel's ActionProbe facility with BST. Refer to the IEEE Standard 1149.1 specification for detailed information regarding BST.

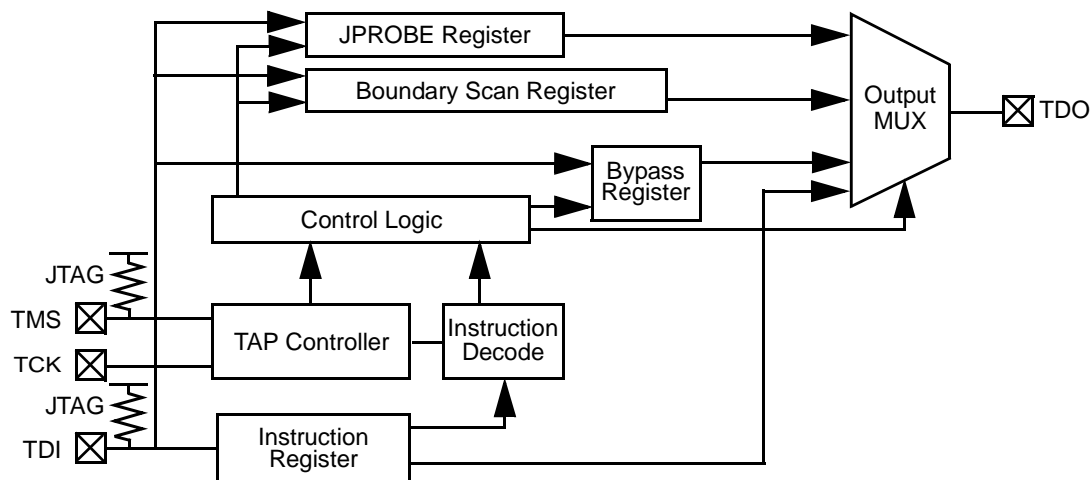
**Boundary Scan Circuitry**

The 42MX boundary scan circuitry consists of a Test Access Port (TAP) controller, test instruction register, a JPROBE register, a bypass register, and a boundary scan register. [Figure 11 on page 11](#) shows a block diagram of the 42MX boundary scan circuitry.



*\*QCLK1IN, QCLK2IN, QCLK3IN, and QCLK4IN are internally-generated signals.*

**Figure 10 • Quadrant Clock Network**



**Figure 11 • 42MX IEEE 1149.1 Boundary Scan Circuitry**

When a device is operating in BST mode, four I/O pins are used for the TDI, TDO, TMS, and TCK signals. An active reset (nTRST) pin is not supported; however, the 42MX device contain power-on circuitry that resets the boundary scan circuitry upon power-up. Table 1 summarizes the functions of the IEEE 1149.1 BST signals.

**Table 1 • IEEE 1149.1 BST Signals**

| Signal | Name             | Function   |
|--------|------------------|--|
| TDI    | Test Data In     | Serial data input for BST instructions and data. Data is shifted in on the rising edge of TCK. |
| TDO    | Test Data Out    | Serial data output for BST instructions and test data.   |
| TMS    | Test Mode Select | Serial data input for BST mode. Data is shifted in on the rising edge of TCK.                  |
| TCK    | Test Clock       | Clock signal to shift the BST data into the device.  |

**JTAG**

All SX-A devices are IEEE 1149.1 (JTAG) compliant. SX-A devices offer superior diagnostic and testing capabilities by providing JTAG and probing capabilities. These functions are controlled through the special JTAG pins in conjunction with the program fuse.

**JTAG fuse programmed:**

- TCK must be terminated—logical high or low doesn't matter (to avoid floating input)
- TDI, TMS may float or at logical high (internal pull-up is present)
- TDO may float or connect to TDI of another device (it's an output)

**JTAG fuse not programmed:**

- TCK, TDI, TDO, TMS are user I/O. If not used, they will be configured as tristated output.

**BST Instructions**

Boundary scan testing within the 42MX devices is controlled by a Test Access Port (TAP) state machine. The TAP controller drives the three-bit instruction register, a bypass register, and the boundary scan data registers within the device. The TAP controller uses the TMS signal to control the testing of the device. The BST mode is determined by the bitstream entered on the TMS pin. Table 2 describes the test instructions supported by the 42MX devices.

**Reset**

The TMS pin is equipped with an internal pull-up resistor. This allows the TAP controller to remain in or return to the Test-Logic-Reset state when there is no input or when a logical 1 is on the TMS pin. To reset the controller, TMS must be HIGH for at least five TCK cycles.

**Table 2 • BST Instructions**

| Test Mode           | Code | Description  |
|---------------------|------|--|
| EXTTEST             | 000  | Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins. |
| SAMPLE/<br>PRELOAD  | 001  | Allows a snapshot of the signals at the device pins to be captured and examined during device operation.   |
| JPROBE              | 011  | A private instruction allowing the user to connect Actel's Micro Probe registers to the test chain.  |
| USER<br>INSTRUCTION | 100  | Allows the user to build application-specific instructions such as RAM READ and RAM WRITE.   |
| HIGH Z              | 101  | Refer to the IEEE Standard 1149.1 specification.   |
| CLAMP               | 110  | Refer to the IEEE Standard 1149.1 specification.   |
| BYPASS              | 111  | Enables the bypass register between the TDI and TDO pins. The test data passes through the selected device to adjacent devices in the test chain.                      |

## 5.0V Operating Conditions and Mixed 5.0V/3.3V Operating Conditions

### Absolute Maximum Ratings<sup>1</sup>

#### Free Air Temperature Range

| Symbol            | Parameter           | Limits                 | Units |
|-------------------|---------------------|------------------------|-------|
| $V_{CCA}/V_{CCI}$ | DC Supply Voltage   | -0.5 to +7.0           | V     |
| $V_I$             | Input Voltage       | -0.5 to $V_{CC} + 0.5$ | V     |
| $V_O$             | Output Voltage      | -0.5 to $V_{CC} + 0.5$ | V     |
| $T_{STG}$         | Storage Temperature | -65 to +150            | °C    |

#### Notes:

- Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.
- Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than  $V_{CCA} + 0.5V$  or less than  $GND - 0.5V$ , the internal protection diode will be forward-biased and can draw excessive current.

### Recommended Operating Conditions

| Parameter                      | Commercial   | Industrial | Military    | Units      |
|--------------------------------|--------------|------------|-------------|------------|
| Temperature Range <sup>1</sup> | 0 to +70     | -40 to +85 | -55 to +125 | °C         |
| Power Supply Tolerance         | ±5           | ±10        | ±10         | % $V_{CC}$ |
| $V_{CCI}$                      | 4.75 to 5.25 | 4.5 to 5.5 | 4.5 to 5.5  | V          |
| $V_{CCA}$                      | 4.75 to 5.25 | 4.5 to 5.5 | 4.5 to 5.5  | V          |
| $V_{CCI}$ <sup>2</sup>         | 3.14 to 3.47 | 3.0 to 3.6 | 3.0 to 3.6  | V          |

#### Notes:

- Ambient temperature ( $T_A$ ) is used for commercial and industrial; case temperature ( $T_C$ ) is used for military.
- Operating condition for I/Os in mixed voltage mode.

### Electrical Specifications

| Symbol                | Parameter                                     | Commercial   |                 | Commercial ‘-F’ |                 | Industrial |                 | Military |                 | Units |
|-----------------------|---|--|-----------------|-----------------|-----------------|------------|-----------------|----------|-----------------|-------|
|                       |   | Min.   | Max.            | Min.            | Max.            | Min.       | Max.            | Min.     | Max.            |       |
| $V_{OH}$ <sup>1</sup> | ( $I_{OH} = -10$ mA) <sup>2</sup> TTL         | 2.4  |                 | 2.4             |                 |            |                 |          |                 | V     |
|                       | ( $I_{OH} = -6$ mA) TTL                       |  |                 |                 |                 |            |                 |          |                 | V     |
|                       | ( $I_{OH} = -4$ mA) TTL                       |  |                 |                 |                 | 3.7        |                 | 3.7      |                 | V     |
| $V_{OL}$ <sup>1</sup> | ( $I_{OL} = 10$ mA) <sup>2</sup> TTL          |  | 0.5             |                 | 0.5             |            |                 |          |                 | V     |
|                       | ( $I_{OL} = 6$ mA) TTL                        |  |                 |                 |                 | 0.40       |                 | 0.40     |                 | V     |
| $V_{IL}$              |   | -0.3   | 0.8             | -0.3            | 0.8             | -0.3       | 0.8             | -0.3     | 0.8             | V     |
| $V_{IH}$              |   | 2.0  | $V_{CCI} + 0.3$ | 2.0             | $V_{CCI} + 0.3$ | 2.0        | $V_{CCI} + 0.3$ | 2.0      | $V_{CCI} + 0.3$ | V     |
| $I_{IL}$              | ( $V_{IN} = 0.5$ )                            |  | -10             |                 | -10             |            | -10             |          | -10             | µA    |
| $I_{IH}$              | ( $V_{IN} = 2.7$ )                            |  | -10             |                 | -10             |            | -10             |          | -10             | µA    |
|                       | Input Transition Time $t_R, t_F$ <sup>2</sup> |  | 500             |                 | 500             |            | 500             |          | 500             | ns    |
|                       | $C_{IO}$ I/O Capacitance <sup>2,3</sup>       |  | 10              |                 | 10              |            | 10              |          | 10              | pF    |
|                       | Standby Current, $I_{CC}$ <sup>4</sup>        |  | Notes 5 & 6     |                 | 25.0            |            | Notes 6 & 7     |          | 25              | mA    |
|                       | $I_{CC(D)}$ Dynamic $V_{CCI}$ Supply Current  | See the “Power Dissipation” section on <a href="#">page 18</a> . |                 |                 |                 |            |                 |          |                 |       |
|                       | Low Power Mode Standby Current                |  | Note 8          |                 | $I_{CC} - 0.5$  |            | $I_{CC} - 0.5$  |          | $I_{CC} - 0.5$  | mA    |

#### Notes:

- Only one output tested at a time.  $V_{CCI} = \text{min}$ .
- Not tested, for information only.
- Includes worst-case 84-pin PLCC package capacitance.  $V_{OUT} = 0$  V,  $f = 1$  MHz.
- All outputs unloaded. All inputs =  $V_{CCI}$  or GND.  $I_{CC}$  limit includes  $I_{PP}$  and  $I_{SV}$  during normal operation.
- A40MX02 and A40MX04  $I_{CC} = 3$  mA, A42MX09  $I_{CC} = 5$  mA, A42MX16  $I_{CC} = 6$  mA, A42MX24, A42MX24A, and A42MX36  $I_{CC} = 25$  mA.
- $I_{CC} \text{ Max} = 2$  mA is available by special request. Contact your local Actel Sales representative for additional information.
- A40MX02 and A40MX04  $I_{CC} = 10$  mA, A42MX09, A42MX16, A42MX24, A42MX24A, and A42MX36  $I_{CC} = 25$  mA.
- In Low Power Mode, A42MX09  $I_{CC} = 50$  µA; A42MX16, A42MX24, and A42MX36  $I_{CC} = 100$  µA. A40MX02 and A40MX04 = N/A.

### 3.3V Operating Conditions

#### Absolute Maximum Ratings<sup>1</sup>

**V<sub>CC</sub> = V<sub>CCA</sub> and V<sub>CCI</sub>**

**Free Air Temperature Range**

| Symbol           | Parameter                            | Limits                        | Units |
|------------------|--------------------------------------|-------------------------------|-------|
| V <sub>CC</sub>  | DC Supply Voltage                    | -0.5 to +7.0                  | V     |
| V <sub>I</sub>   | Input Voltage                        | -0.5 to V <sub>CC</sub> + 0.5 | V     |
| V <sub>O</sub>   | Output Voltage                       | -0.5 to V <sub>CC</sub> + 0.5 | V     |
| I <sub>IO</sub>  | I/O Source Sink Current <sup>2</sup> | ±20                           | mA    |
| T <sub>STG</sub> | Storage Temperature                  | -65 to +150                   | °C    |

**Notes:**

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.
2. Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V<sub>CC</sub> + 0.5V or less than GND - 0.5V, the internal protection diodes will forward-bias and can draw excessive current.

#### Recommended Operating Conditions

| Parameter                      | Commercial | Industrial | Military    | Units |
|--------------------------------|------------|------------|-------------|-------|
| Temperature Range <sup>1</sup> | 0 to +70   | -40 to +85 | -55 to +125 | °C    |
| Power Supply Tolerance         | ±5         | ±10        | ±10         | %V    |
| V <sub>CCI</sub>               | 3.0 to 3.6 | 3.0 to 3.6 | 3.0 to 3.6  | V     |
| V <sub>CCA</sub>               | 3.0 to 3.6 | 3.0 to 3.6 | 3.0 to 3.6  | V     |

**Note:**

1. Ambient temperature (T<sub>A</sub>) is used for commercial, and industrial; case temperature (T<sub>C</sub>) is used for military.

#### Electrical Specifications

| Parameter  | Commercial                                      |                       | Commercial ‘-F’       |                       | Industrial            |                       | Military              |                       | Units |
|--|---|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-------|
|  | Min.  | Max.                  | Min.                  | Max.                  | Min.                  | Max.                  | Min.                  | Max.                  |       |
| V <sub>OH</sub> <sup>1</sup>                                       | (I <sub>OH</sub> = -4 mA)                       |                       | 2.15                  |                       | 2.15                  |                       | 2.4                   |                       | V     |
|  | (I <sub>OH</sub> = -3.2 mA)                     |                       | 2.4                   |                       | 2.4                   |                       |                       |                       | V     |
| V <sub>OL</sub> <sup>1</sup>                                       | (I <sub>OL</sub> = 6 mA)                        |                       | 0.4                   |                       | 0.4                   |                       | 0.48                  |                       | V     |
| V <sub>IL</sub>  | -0.3  | 0.8                   | -0.3                  | 0.8                   | -0.3                  | 0.8                   | -0.3                  | 0.8                   | V     |
| V <sub>IH</sub>  | 2.0   | V <sub>CC</sub> + 0.3 | 2.0                   | V <sub>CC</sub> + 0.3 | 2.0                   | V <sub>CC</sub> + 0.3 | 2.0                   | V <sub>CC</sub> + 0.3 | V     |
| I <sub>IL</sub>  |   |                       | -10                   |                       | -10                   |                       | -10                   |                       | µA    |
| I <sub>IH</sub>  |   |                       | -10                   |                       | -10                   |                       | -10                   |                       | µA    |
| Input Transition Time t <sub>R</sub> , t <sub>F</sub> <sup>2</sup> |   |                       | 500                   |                       | 500                   |                       | 500                   |                       | ns    |
| C <sub>IO</sub> I/O Capacitance <sup>2, 3</sup>                    |   |                       | 10                    |                       | 10                    |                       | 10                    |                       | pF    |
| Standby Current, I <sub>CC</sub> <sup>4</sup>                      |   |                       | Notes 5 & 6           |                       | 25                    |                       | Notes 6 & 7           |                       | mA    |
| I <sub>CC(D)</sub> Dynamic V <sub>CC</sub> Supply Current          | See the “Power Dissipation” section on page 18. |                       |                       |                       |                       |                       |                       |                       |       |
| Low Power Mode Standby Current                                     | Note 8  |                       | I <sub>CC</sub> - 5.0 |                       | I <sub>CC</sub> - 5.0 |                       | I <sub>CC</sub> - 5.0 |                       | mA    |

**Notes:**

1. Only one output IV curve tested at a time. V<sub>CC</sub> = min.
2. Not tested, for information only.
3. Includes worst-case 84-pin PLCC package capacitance. V<sub>OUT</sub> = 0 V, f = 1 MHz.
4. All outputs unloaded. All inputs = V<sub>CC</sub> or GND.
5. A40MX02 and A40MX04 I<sub>CC</sub> = 3 mA, A42MX09 I<sub>CC</sub> = 5 mA, A42MX16 I<sub>CC</sub> = 6 mA, A42MX24 and A42MX36 I<sub>CC</sub> = 25 mA.
6. I<sub>CC</sub> Max = 1.5mA is available by special request. Contact your Actel Sales representative for additional information.
7. A40MX02 and A40MX04 I<sub>CC</sub> = 10 mA, A42MX09, A42MX16, A42MX24, and A42MX36 I<sub>CC</sub> = 25 mA.
8. In Low Power Mode, A42MX09 I<sub>CC</sub> = 15 µA; A42MX16, A42MX24, A42MX36 I<sub>CC</sub> = 50 µA. A40MX02 and A40MX04 = N/A.

## Output Drive Characteristics for 5.0V PCI Signaling

MX PCI device I/O drivers were designed specifically for high-performance PCI systems. Figure 12 on page 17 shows the typical output drive characteristics of the MX devices. MX output drivers are compliant with the PCI Local Bus Specification.

### DC Specification (5.0V PCI Signaling)<sup>1</sup>

| Symbol           | Parameter                  | Condition  | PCI     |                       | MX      |                       | Units |
|------------------|----------------------------|--|---------|-----------------------|---------|-----------------------|-------|
|                  |                            |  | Minimum | Maximum               | Minimum | Maximum               |       |
| V <sub>CC</sub>  | Supply Voltage             |  | 4.75    | 5.25                  | 4.75    | 5.25 <sup>2</sup>     | V     |
| V <sub>IH</sub>  | Input High Voltage         |  | 2.0     | V <sub>CC</sub> + 0.5 | 2.0     | V <sub>CC</sub> + 0.3 | V     |
| V <sub>IL</sub>  | Input Low Voltage          |  | -0.5    | 0.8                   | -0.3    | 0.8                   | V     |
| I <sub>IH</sub>  | Input High Leakage Current | V <sub>IN</sub> = 2.7                                |         | 70                    | —       | 10                    | μA    |
| I <sub>IL</sub>  | Input Low Leakage Current  | V <sub>IN</sub> =0.5                                 |         | -70                   | —       | -10                   | μA    |
| V <sub>OH</sub>  | Output High Voltage        | I <sub>OUT</sub> = -2 mA<br>I <sub>OUT</sub> = -6 mA | 2.4     |                       | 3.84    |                       | V     |
| V <sub>OL</sub>  | Output Low Voltage         | I <sub>OUT</sub> = 3 mA,<br>6 mA                     |         | 0.55                  | —       | 0.33                  | V     |
| C <sub>IN</sub>  | Input Pin Capacitance      |  |         | 10                    | —       | 10                    | pF    |
| C <sub>CLK</sub> | CLK Pin Capacitance        |  | 5       | 12                    | —       | 10                    | pF    |
| L <sub>PIN</sub> | Pin Inductance             |  |         | 20                    | —       | < 8 nH <sup>3</sup>   | nH    |

**Notes:**

1. PCI Local Bus Specification Section 4.2.1.1.
2. Maximum rating for V<sub>CC</sub> -0.5V to 7.0V.
3. Dependent upon the chosen package. PCI recommends QFP and BGA packaging to reduce pin inductance and capacitance.

### AC Specifications (5.0V PCI Signaling)<sup>1</sup>

| Symbol          | Parameter             | Condition                 | PCI                                 |         | MX      |         | Units |
|-----------------|-----------------------|---------------------------|-------------------------------------|---------|---------|---------|-------|
|                 |                       |                           | Minimum                             | Maximum | Minimum | Maximum |       |
| I <sub>CL</sub> | Low Clamp Current     | -5 < V <sub>IN</sub> ≤ -1 | -25 + (V <sub>IN</sub> + 1) / 0.015 |         | -60     | -10     | mA    |
| Slew (r)        | Output Rise Slew Rate | 0.4V to 2.4V load         | 1                                   | 5       | 1.8     | 2.8     | V/ns  |
| Slew (f)        | Output Fall Slew Rate | 2.4V to 0.4V load         | 1                                   | 5       | 2.8     | 4.3     | V/ns  |

**Note:**

1. PCI Local Bus Specification Section 4.2.1.2.

## Output Drive Characteristics for 3.3V PCI Signaling

### DC Specification (3.3V PCI Signaling)<sup>1</sup>

| Symbol           | Parameter                  | Condition                        | PCI     |                       | MX      |                       | Units |
|------------------|----------------------------|----------------------------------|---------|-----------------------|---------|-----------------------|-------|
|                  |                            |                                  | Minimum | Maximum               | Minimum | Maximum               |       |
| V <sub>CC</sub>  | Supply Voltage             |                                  | 3.0     | 3.6                   | 3.0     | 3.6                   | V     |
| V <sub>IH</sub>  | Input High Voltage         |                                  | 0.5     | V <sub>CC</sub> + 0.5 | 0.5     | V <sub>CC</sub> + 0.3 | V     |
| V <sub>IL</sub>  | Input Low Voltage          |                                  | -0.5    | 0.8                   | -0.3    | 0.8                   | V     |
| I <sub>IH</sub>  | Input High Leakage Current | V <sub>IN</sub> = 2.7            |         | 70                    |         | 10                    | μA    |
| I <sub>IL</sub>  | Input Leakage Current      |                                  |         | -70                   |         | -10                   | μA    |
| V <sub>OH</sub>  | Output High Voltage        | I <sub>OUT</sub> = -2 mA         | 0.9     |                       | 3.3     |                       | V     |
| V <sub>OL</sub>  | Output Low Voltage         | I <sub>OUT</sub> = 3 mA,<br>6 mA |         | 0.1                   |         | 0.1 V <sub>CC</sub>   | V     |
| C <sub>IN</sub>  | Input Pin Capacitance      |                                  |         | 10                    |         | 10                    | pF    |
| C <sub>CLK</sub> | CLK Pin Capacitance        |                                  | 5       | 12                    |         | 10                    | pF    |
| L <sub>PIN</sub> | Pin Inductance             |                                  |         | 20                    |         | < 8 nH <sup>3</sup>   | nH    |

**Notes:**

1. PCI Local Bus Specification Section 4.2.2.1.
2. Maximum rating for V<sub>CC</sub> -0.5V to 7.0V.
3. Dependent upon the chosen package. PCI recommends QFP and BGA packaging to reduce pin inductance and capacitance.

### AC Specifications for (3.3V PCI Signaling)<sup>1</sup>

| Symbol          | Parameter             | Condition                 | PCI                                   |         | MX      |         | Units |
|-----------------|-----------------------|---------------------------|---------------------------------------|---------|---------|---------|-------|
|                 |                       |                           | Minimum                               | Maximum | Minimum | Maximum |       |
| I <sub>CL</sub> | Low Clamp Current     | -5 < V <sub>IN</sub> ≤ -1 | -25 + (V <sub>IN</sub> + 1)<br>/0.015 |         | -60     | -10     | mA    |
| Slew (r)        | Output Rise Slew Rate | 0.2V to 0.6V load         | 1                                     | 4       | 1.8     | 2.8     | V/ns  |
| Slew (f)        | Output Fall Slew Rate | 0.6V to 0.2V load         | 1                                     | 4       | 2.8     | 4.0     | V/ns  |

**Note:**

1. PCI Local Bus Specification Section 4.2.2.2.



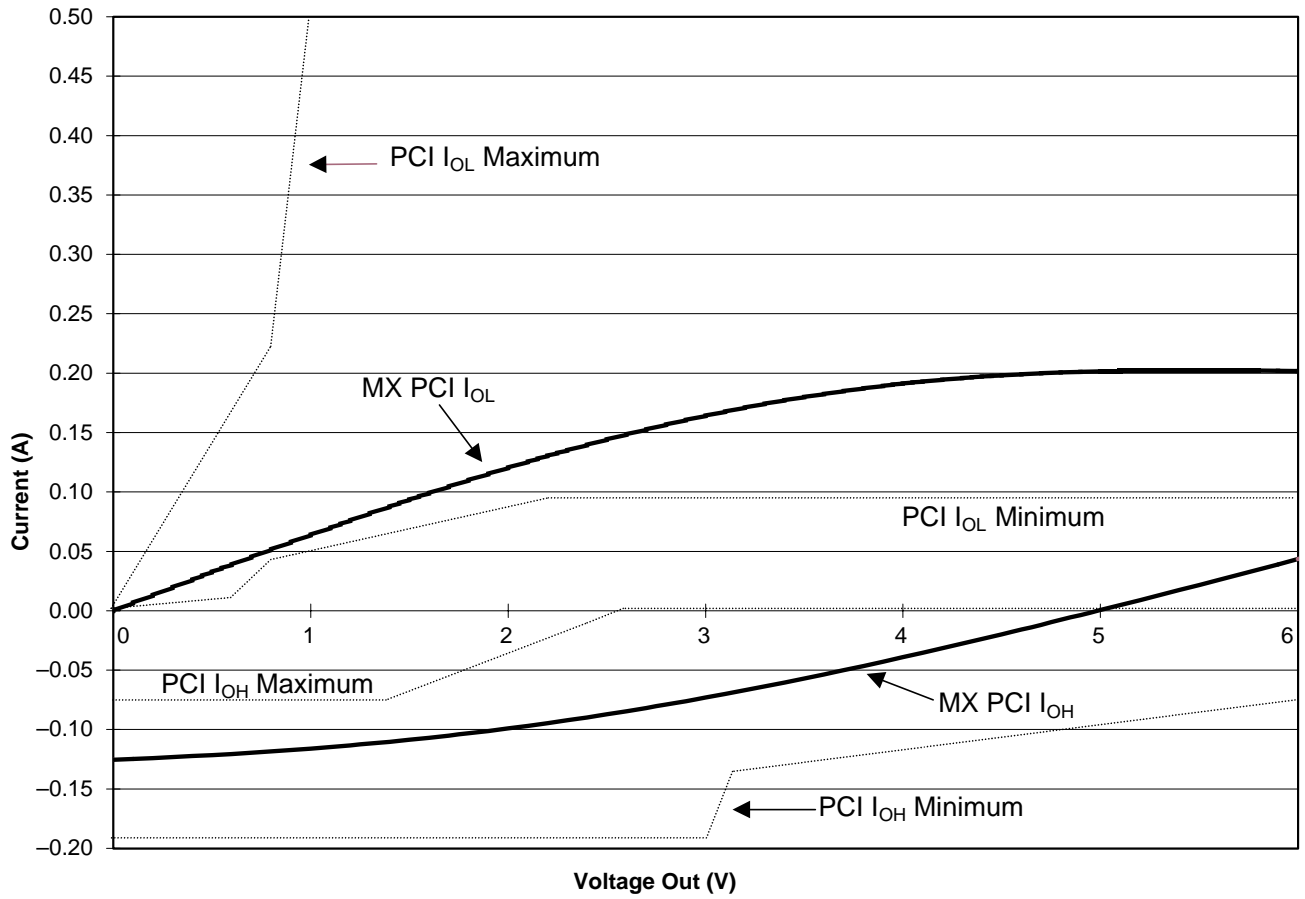


Figure 12 • Typical Output Drive Characteristics (Based upon measured data)

## Package Thermal Characteristics

The device junction-to-case thermal characteristic is  $\theta_{jc}$ , and the junction-to-ambient air characteristic is  $\theta_{ja}$ . The thermal characteristics for  $\theta_{ja}$  are shown with two different air flow rates. Ambient temperature ( $T_A$ ) is used for commercial and industrial; case temperature ( $T_C$ ) is used for military.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a PQFP 160-pin package at commercial temperature is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. commercial temp.}}{\theta_{ja} \text{ (°C/W)}} = \frac{150^\circ\text{C} - 70^\circ\text{C}}{32^\circ\text{C/W}} = 2.5\text{ W}$$

| Plastic Packages                 | Pin Count | $\theta_{jc}$ | $\theta_{ja}$ |            |
|----------------------------------|-----------|---------------|---------------|------------|
|                                  |           |               | Still Air     | 300 ft/min |
| Plastic Quad Flat Pack           | 100       | 12            | 34°C/W        | 31°C/W     |
| Plastic Quad Flat Pack           | 160       | 10            | 32°C/W        | 24°C/W     |
| Plastic Quad Flat Pack           | 208       | 8             | 30°C/W        | 23°C/W     |
| Plastic Quad Flat Pack           | 240       | 3.5           | 19°C/W        | 16°C/W     |
| Plastic Leaded Chip Carrier      | 44        | 16            | 43°C/W        | 31°C/W     |
| Plastic Leaded Chip Carrier      | 68        | 13            | 36°C/W        | 25°C/W     |
| Plastic Leaded Chip Carrier      | 84        | 12            | 32°C/W        | 22°C/W     |
| Thin Plastic Quad Flat Pack      | 176       | 11            | 28°C/W        | 21°C/W     |
| Very Thin Plastic Quad Flat Pack | 80        | 12            | 39°C/W        | 33°C/W     |
| Very Thin Plastic Quad Flat Pack | 100       | 10            | 38°C/W        | 32°C/W     |
| Plastic Ball Grid Array          | 272       | 3             | 20°C/W        | 14.5°C/W   |

| Ceramic Packages       | Pin Count | $\theta_{jc}$ | $\theta_{ja}$ |
|------------------------|-----------|---------------|---------------|
|                        |           |               | Still Air     |
| Ceramic Quad Flat Pack | 208       | 6.3           | 22°C/W        |
| Ceramic Quad Flat Pack | 256       | 6.2           | 20°C/W        |

## Power Dissipation

### General Power Equation

$$P = [I_{CC\text{standby}} + I_{CC\text{active}}] * V_{CCI} + I_{OL} * V_{OL} * N + I_{OH} * (V_{CCI} - V_{OH}) * M$$

where:

$I_{CC\text{standby}}$  is the current flowing when no inputs or outputs are changing.

$I_{CC\text{active}}$  is the current flowing due to CMOS switching.

$I_{OL}$ ,  $I_{OH}$  are TTL sink/source currents.

$V_{OL}$ ,  $V_{OH}$  are TTL level output voltages.

N equals the number of outputs driving TTL loads to  $V_{OL}$ .

M equals the number of outputs driving TTL loads to  $V_{OH}$ .

Accurate values for N and M are difficult to determine because they depend on the family type, on design details, and on the system I/O. The power can be divided into two components: static and active.

### Static Power Component

Actel FPGAs have small static power components that result in power dissipation lower than PALs or CPLDs. By integrating multiple PALs/CPLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated for commercial, worst-case conditions:

| $I_{CC}$ | $V_{CCA}$ | Power   |
|----------|-----------|---------|
| 2 mA     | 5.25 V    | 10.5 mW |

The static power dissipation by TTL loads depends on the number of outputs driving HIGH or LOW, and on the DC load current. Again, this number is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33V will generate 42 mW with all outputs driving LOW, and 140 mW with all outputs driving HIGH. The actual dissipation will average somewhere in between, as I/Os switch states with time.

**Active Power Component**

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency-dependent and a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs. An additional component of the active power dissipation is the totem pole current in the CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

**Equivalent Capacitance**

The power dissipated by a CMOS circuit can be expressed by the equation:

$$\text{Power } (\mu\text{W}) = C_{\text{EQ}} * V_{\text{CCA}}^2 * F \tag{1}$$

where:

$C_{\text{EQ}}$  = Equivalent capacitance expressed in picofarads (pF)

$V_{\text{CCA}}$  = Power supply in volts (V)

$F$  = Switching frequency in megahertz (MHz)

Equivalent capacitance is calculated by measuring  $I_{\text{CCactive}}$  at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of  $V_{\text{CC}}$ . Equivalent capacitance is frequency-independent, so the results can be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

**$C_{\text{EQ}}$  Values for Actel MX FPGAs**

|   |      |
|---|------|
| Modules ( $C_{\text{EQM}}$ )                          | 3.5  |
| Input Buffers ( $C_{\text{EQI}}$ )                    | 6.9  |
| Output Buffers ( $C_{\text{EQO}}$ )                   | 18.2 |
| Routed Array Clock Buffer Loads ( $C_{\text{EQCR}}$ ) | 1.4  |

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. The equation below shows a piece-wise linear summation over all components.

$$\begin{aligned} \text{Power} = & V_{\text{CCA}}^2 * [(m * C_{\text{EQM}} * f_m)_{\text{Modules}} + \\ & (n * C_{\text{EQI}} * f_n)_{\text{Inputs}} + (p * (C_{\text{EQO}} + C_L) * f_p)_{\text{Outputs}} + \\ & 0.5 * (q_1 * C_{\text{EQCR}} * f_{q1})_{\text{routed\_Clk1}} + (r_1 * f_{q1})_{\text{routed\_Clk1}} + \\ & 0.5 * (q_2 * C_{\text{EQCR}} * f_{q2})_{\text{routed\_Clk2}} + (r_2 * f_{q2})_{\text{routed\_Clk2}} \end{aligned} \tag{2}$$

where:

- $m$  = Number of logic modules switching at frequency  $f_m$
- $n$  = Number of input buffers switching at frequency  $f_n$
- $p$  = Number of output buffers switching at frequency  $f_p$
- $q_1$  = Number of clock loads on the first routed array clock
- $q_2$  = Number of clock loads on the second routed array clock
- $r_1$  = Fixed capacitance due to first routed array clock
- $r_2$  = Fixed capacitance due to second routed array clock
- $C_{\text{EQM}}$  = Equivalent capacitance of logic modules in pF
- $C_{\text{EQI}}$  = Equivalent capacitance of input buffers in pF
- $C_{\text{EQO}}$  = Equivalent capacitance of output buffers in pF
- $C_{\text{EQCR}}$  = Equivalent capacitance of routed array clock in pF
- $C_L$  = Output load capacitance in p
- $f_m$  = Average logic module switching rate in MHz
- $f_n$  = Average input buffer switching rate in MHz
- $f_p$  = Average output buffer switching rate in MHz
- $f_{q1}$  = Average first routed array clock rate in MHz
- $f_{q2}$  = Average second routed array clock rate in MHz

**Fixed Capacitance Values for MX FPGAs (pF)**

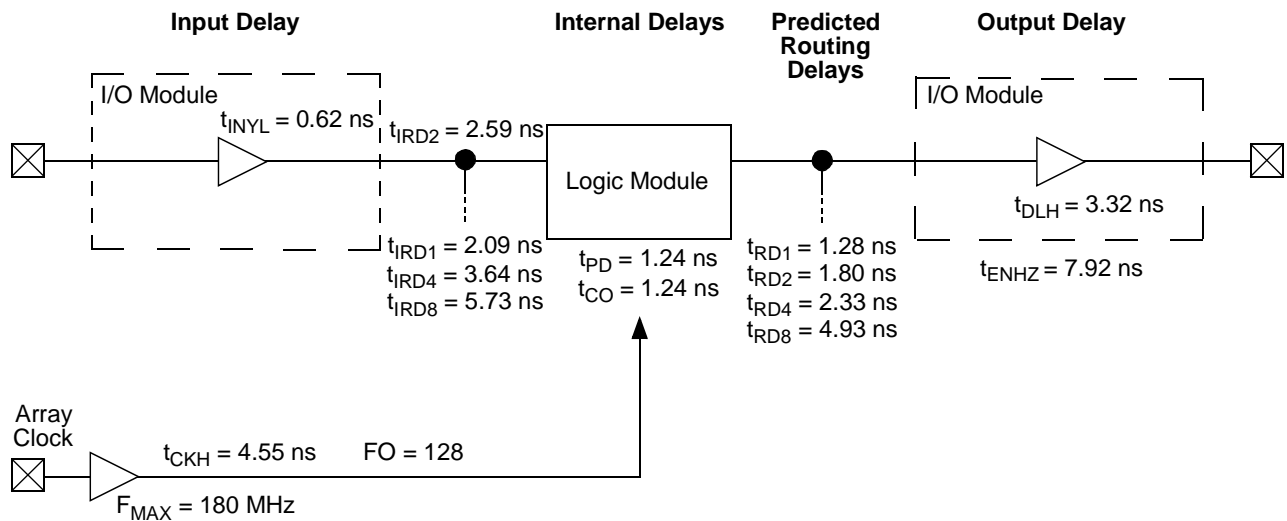
| Device Type | $r_1$<br>routed_Clk1 | $r_2$<br>routed_Clk2 |
|-------------|----------------------|----------------------|
| A40MX02     | 41.4                 | N/A                  |
| A40MX04     | 68.6                 | N/A                  |
| A42MX09     | 118                  | 118                  |
| A42MX16     | 165                  | 165                  |
| A42MX24     | 185                  | 185                  |
| A42MX36     | 220                  | 220                  |

**Determining Average Switching Frequency**

To determine the switching frequency for a design, the data input values to the circuit must be clearly understood. The following guidelines represent worst-case scenarios; these can be used to generally predict the upper limits of power dissipation.

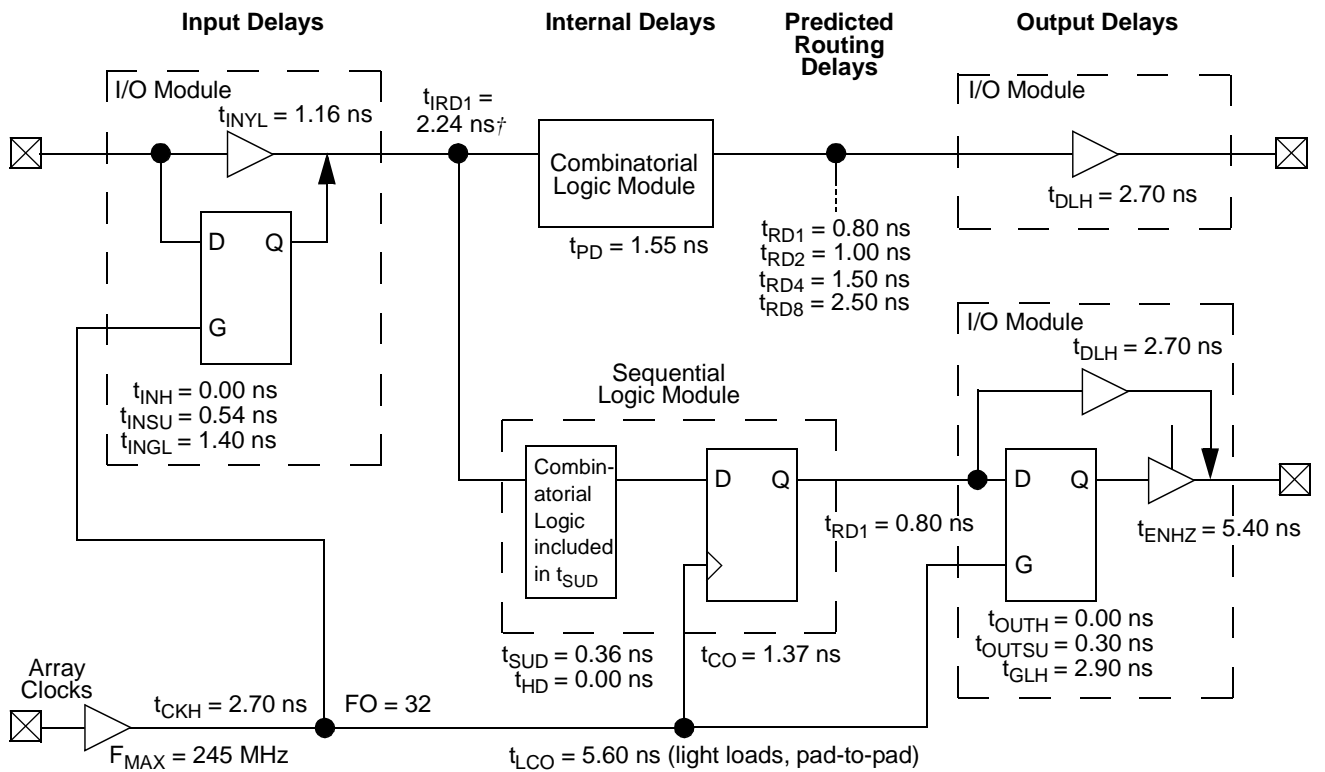
|   |   |                              |
|---|---|------------------------------|
| Logic Modules (m)                                 | = | 80% of Combinatorial Modules |
| Inputs Switching (n)                              | = | # of Inputs/4                |
| Outputs Switching (p)                             | = | # of Outputs/4               |
| First Routed Array Clock Loads (q <sub>1</sub> )  | = | 40% of Sequential Modules    |
| Second Routed Array Clock Loads (q <sub>2</sub> ) | = | 40% of Sequential Modules    |
| Load Capacitance (C <sub>L</sub> )                | = | 35 pF                        |

|   |   |                              |
|---|---|------------------------------|
| Logic Modules (m)   | = | 80% of Combinatorial Modules |
| Average Logic Module Switching Rate (f <sub>m</sub> )     | = | F/10                         |
| Average Input Switching Rate (f <sub>n</sub> )            | = | F/5                          |
| Average Output Switching Rate (f <sub>p</sub> )           | = | F/10                         |
| Average First Routed Array Clock Rate (f <sub>q1</sub> )  | = | F                            |
| Average Second Routed Array Clock Rate (f <sub>q2</sub> ) | = | F/2                          |

**40MX Timing Model\***


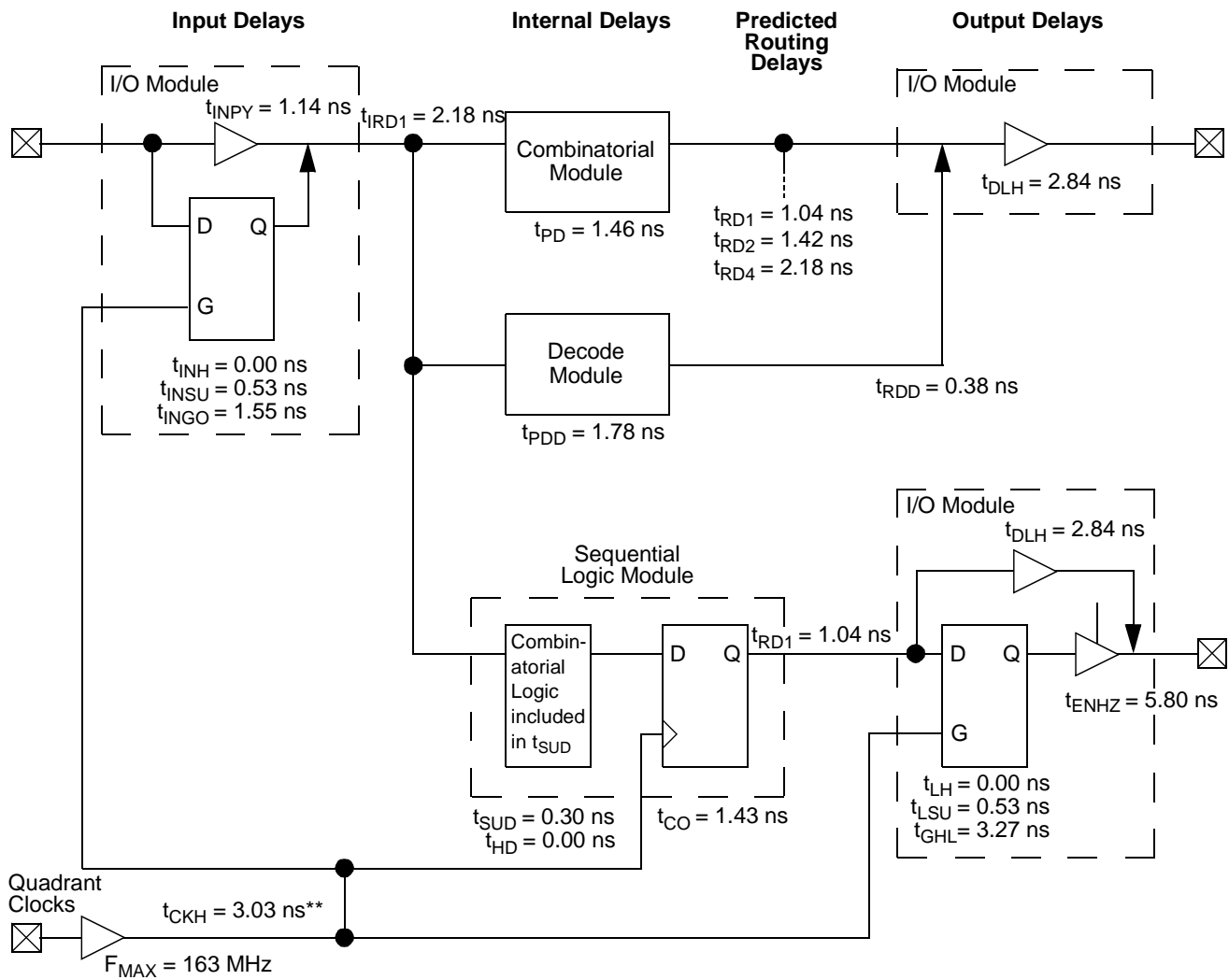
\* Values are shown for 40MX '-3' speed devices at 5.0V worst-case commercial conditions.

42MX Timing Model\*



\*Values are shown for A42MX09 '2' at 5.0V worst-case commercial conditions

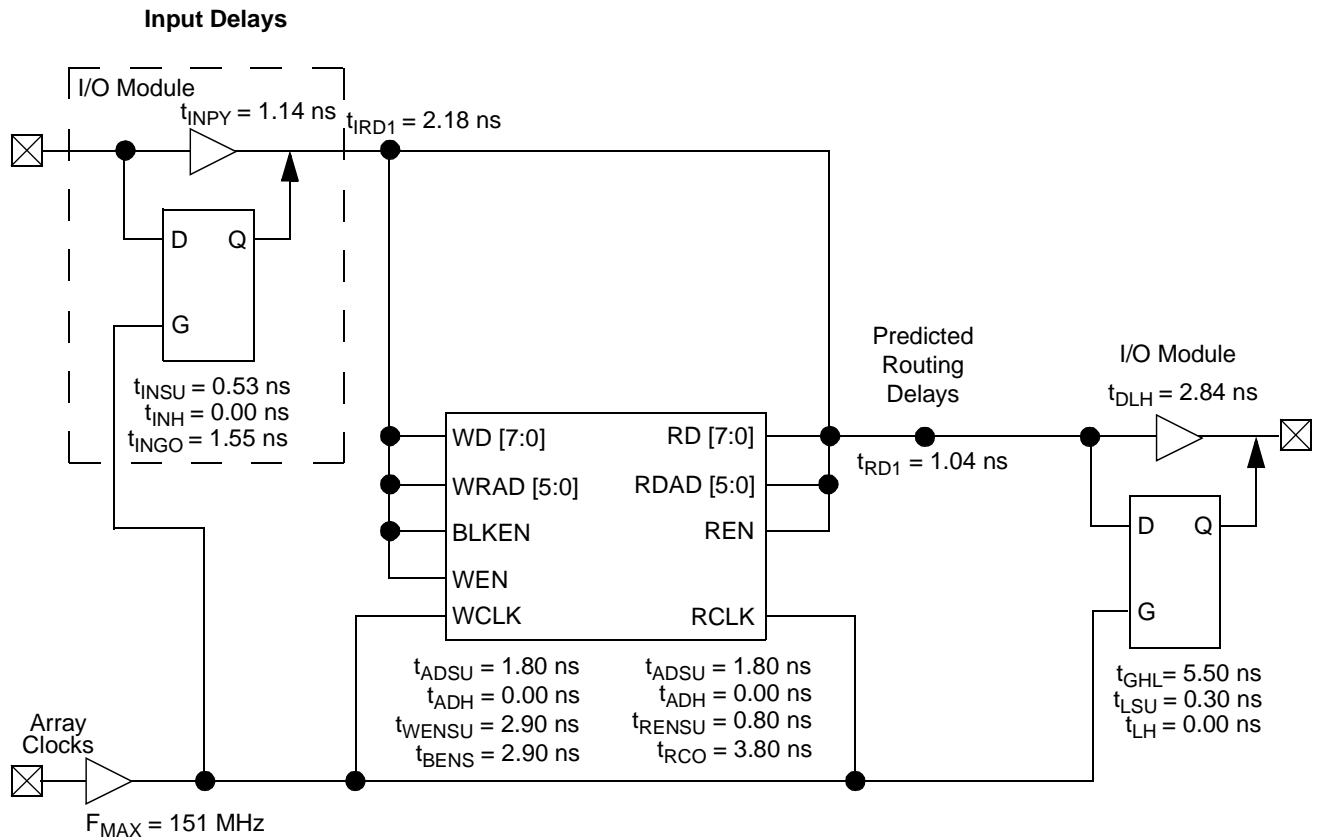
† Input module predicted routing delay

**42MX Timing Model (Logic Functions using Quadrant Clocks)\***


\* Preliminary values are shown for A42MX36 '-2' at 5.0V worst-case commercial conditions

\*\* Load-dependent

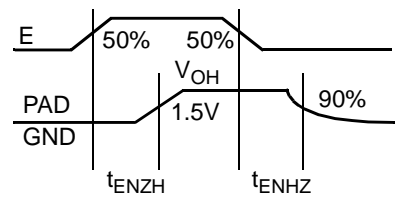
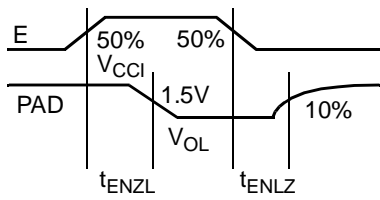
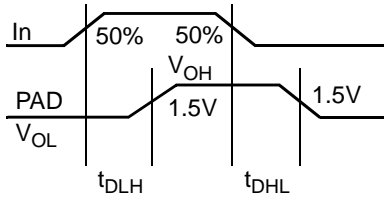
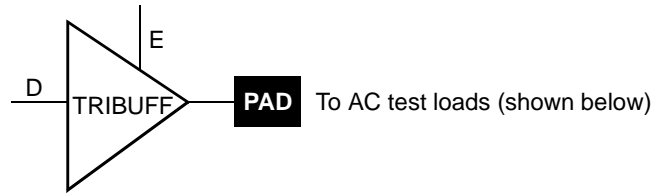
42MX Timing Model (SRAM Functions)\*



\*Values are shown for A42MX36 '-2' at 5.0V worst-case commercial conditions.

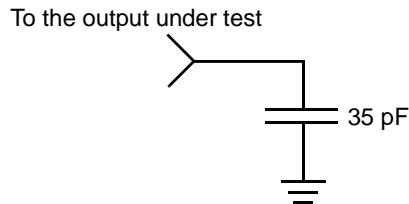
## Parameter Measurement

### Output Buffer Delays

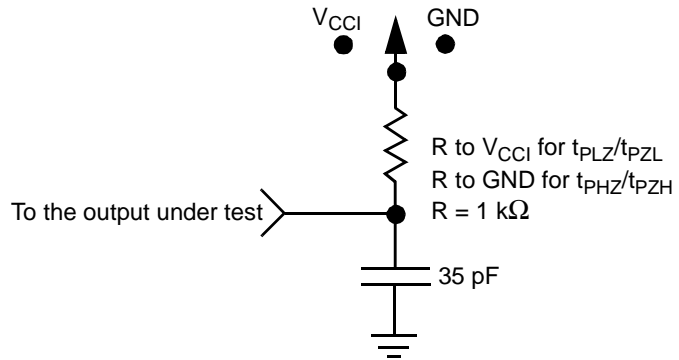


### AC Test Loads

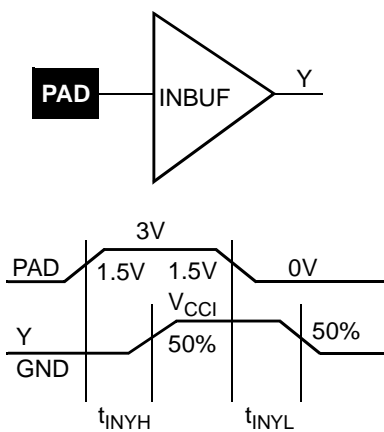
**Load 1**  
(Used to measure propagation delay)



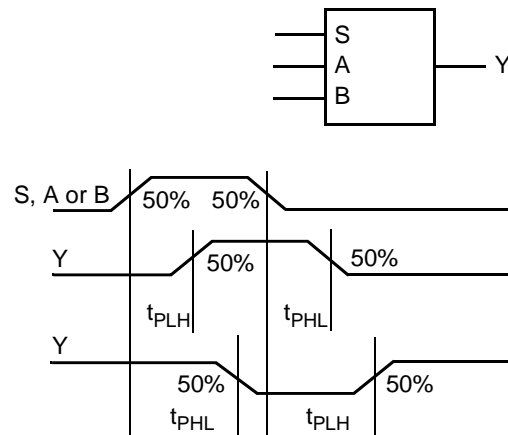
**Load 2**  
(Used to measure rising/falling edges)



### Input Buffer Delays



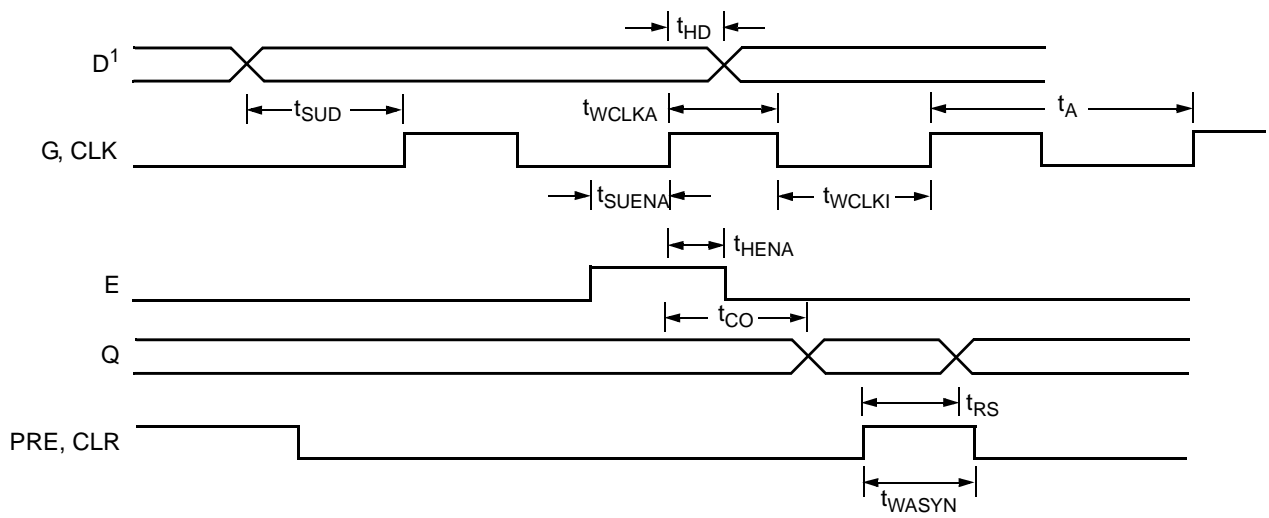
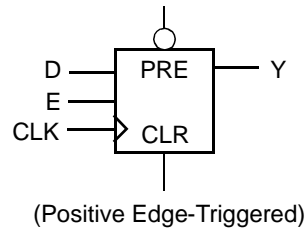
### Module Delays



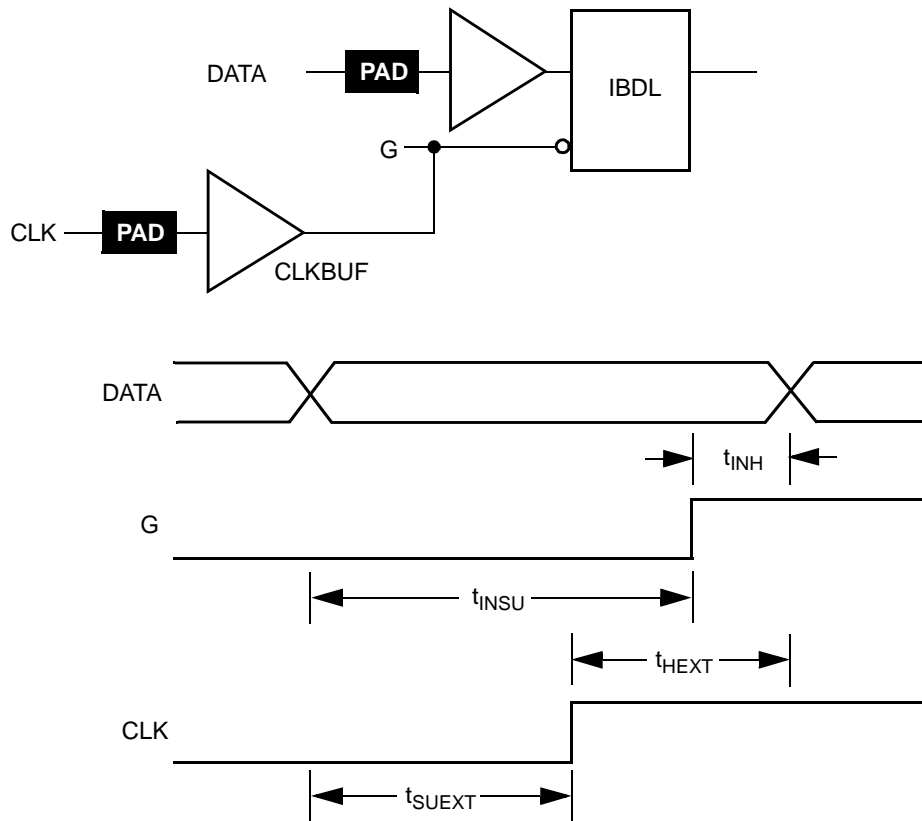
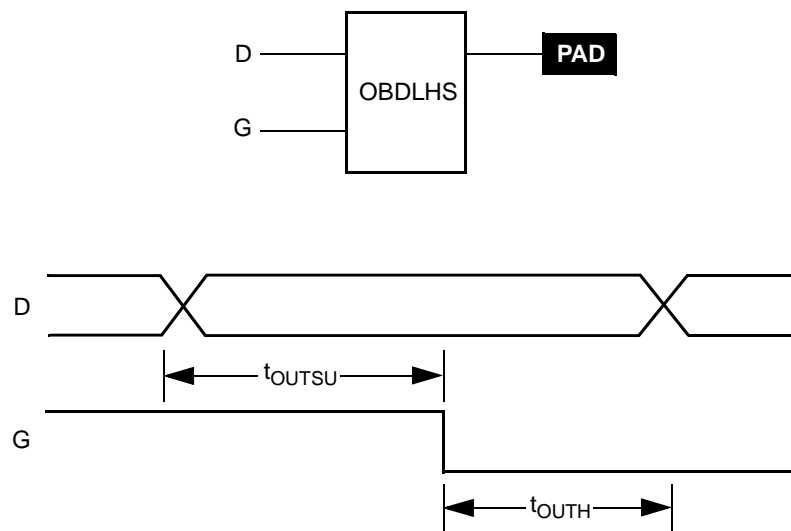


## Sequential Module Timing Characteristics

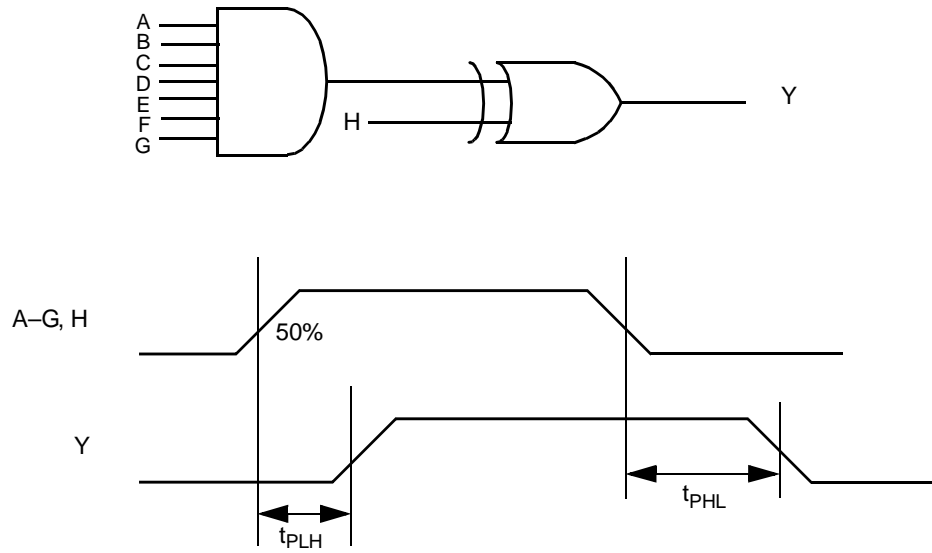
### Flip-Flops and Latches



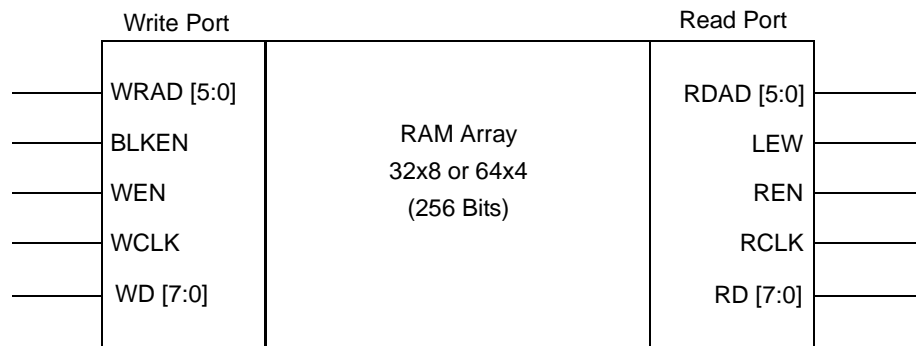
**Note:**  $D$  represents all data functions involving  $A$ ,  $B$ , and  $S$  for multiplexed flip-flops.

**Sequential Timing Characteristics (continued)**
**Input Buffer Latches**

**Output Buffer Latches**


**Decode Module Timing**

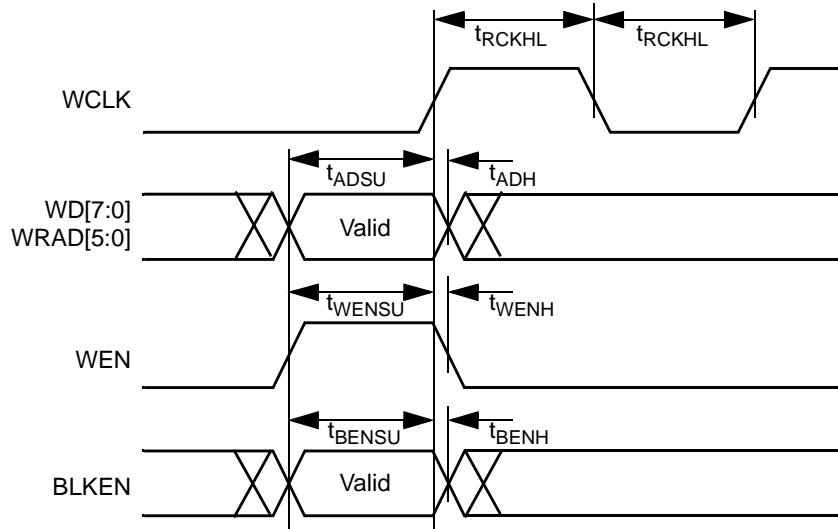


**SRAM Timing Characteristics**



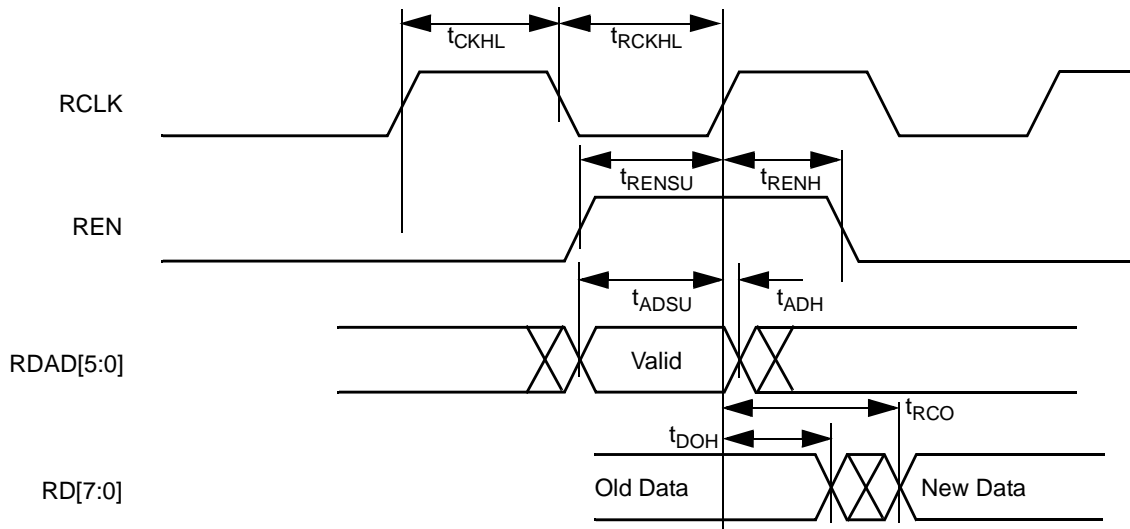
## Dual-Port SRAM Timing Waveforms

### 42MX SRAM Write Operation



*Note: Identical timing for falling edge clock.*

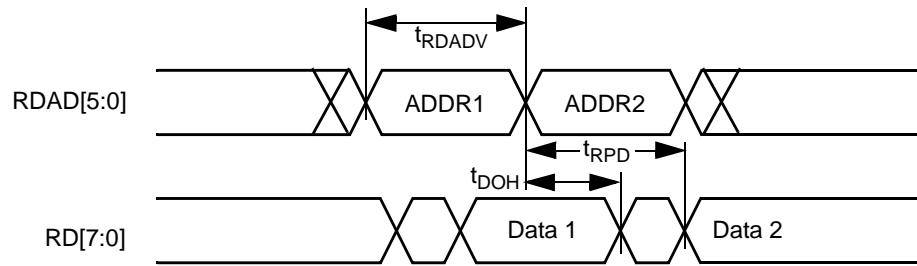
### 42MX SRAM Synchronous Read Operation



*Note: Identical timing for falling edge clock.*

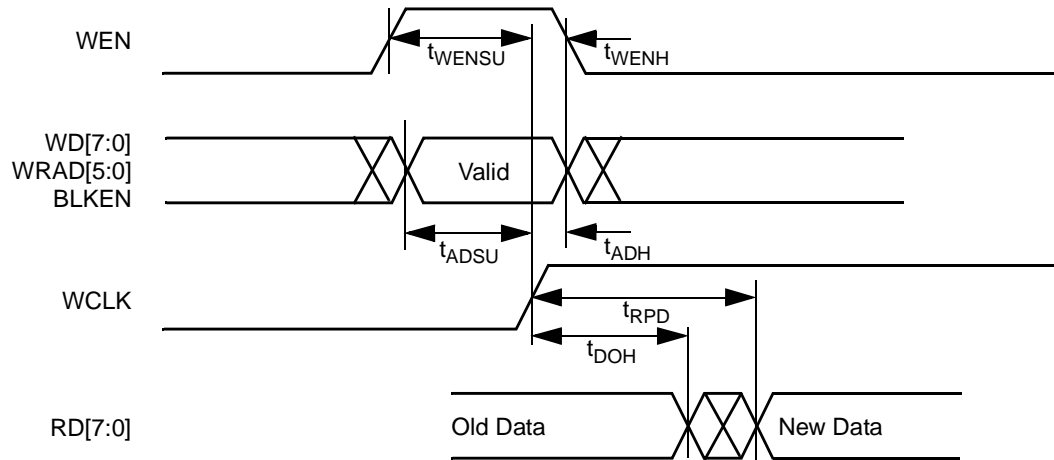
**42MX SRAM Asynchronous Read Operation—Type 1**

(Read Address Controlled)



**42MX SRAM Asynchronous Read Operation—Type 2**

(Write Address Controlled)



### Predictable Performance: Tight Delay Distributions

Propagation delay between logic modules depends on the resistive and capacitive loading of the routing tracks, the interconnect elements, and the module inputs being driven. Propagation delay increases as the length of routing tracks, the number of interconnect elements, or the number of inputs increases.

From a design perspective, the propagation delay can be statistically correlated or modeled by the fanout (number of loads) driven by a module. Higher fanout usually requires some paths to have longer routing tracks.

The MX FPGAs deliver a tight fanout delay distribution, which is achieved in two ways: by decreasing the delay of the interconnect elements and by decreasing the number of interconnect elements per path.

Actel's patented antifuse offers a very low resistive/capacitive interconnect. The antifuses, fabricated in 0.45 μ lithography, offer nominal levels of 100 ¾ resistance and 7.0 femtofarad (fF) capacitance per antifuse.

MX fanout distribution is also tight due to the low number of antifuses required for each interconnect path. The proprietary architecture limits the number of antifuses per path to a maximum of four, with 90 percent of interconnects using only two antifuses.

### Timing Characteristics

Device timing characteristics fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all MX devices. For mixed voltage of the A42MX devices, the timing numbers are defined in the 3.3V section for I/Os while for the internal logic resources, the timing numbers are defined in the 5.0V section. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after place-and-route of the user's design is complete. Delay values may then be determined by using the Designer Series utility or by performing simulation with post-layout delays.

### Critical Nets and Typical Nets

Propagation delays in this data sheet apply to typical nets. The abundant routing resources in the MX architecture allows for deterministic timing using Actel's Designer Series development tools, which include TDPR, a timing-driven place-and-route tool. Using Timer, the designer can specify timing-critical nets and system clock frequency. Using these timing specifications, the place-and-route software optimizes the layout of the design to meet the user's specifications.

### Long Tracks

Some nets in the design use long tracks, which are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes four antifuse connections, which increase capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require long tracks. Long tracks add approximately a 3 ns to a 6 ns delay, which is represented statistically in higher fanout (FO=8) routing delays in the data sheet specifications section, beginning on page 34.

### Timing Derating

A timing derating factor of 0.45 is used to reflect best-case processing. Note that this factor is relative to the standard speed timing parameters and must be multiplied by the appropriate voltage and temperature derating factors for a given application.

### Timing Derating Factors

#### Commercial to Industrial

|                              | Industrial |      |
|------------------------------|------------|------|
|                              | Min.       | Max. |
| (Commercial Specification) x | 0.69       | 1.11 |

#### Commercial Worst-Case to Typical

|                                      | Commercial Typical<br>(T <sub>J</sub> = 25°C, V <sub>CC</sub> = 5.0V) |
|--------------------------------------|---|
| (Commercial, Worst-Case Condition) x | 0.85  |

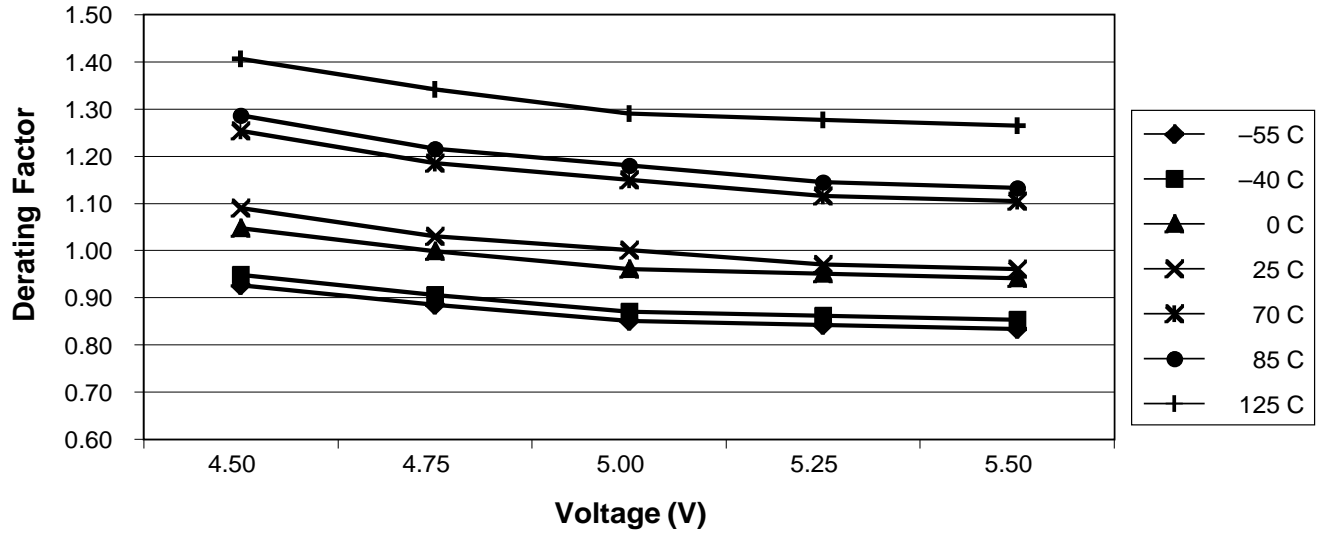
*Note:* This derating factor applies to all routing and propagation delays.

**42MX Temperature and Voltage Derating Factors**

(Normalized to  $T_J = 25^\circ\text{C}$ ,  $V_{CCA}/V_{CCI} = 5.0\text{V}$ )

| 42MX Voltage | Temperature |       |      |      |      |      |       |
|--------------|-------------|-------|------|------|------|------|-------|
|              | -55°C       | -40°C | 0°C  | 25°C | 70°C | 85°C | 125°C |
| 4.50         | 0.93        | 0.95  | 1.05 | 1.09 | 1.25 | 1.29 | 1.41  |
| 4.75         | 0.88        | 0.90  | 1.00 | 1.03 | 1.18 | 1.22 | 1.34  |
| 5.00         | 0.85        | 0.87  | 0.96 | 1.00 | 1.15 | 1.18 | 1.29  |
| 5.25         | 0.84        | 0.86  | 0.95 | 0.97 | 1.12 | 1.14 | 1.28  |
| 5.50         | 0.83        | 0.85  | 0.94 | 0.96 | 1.10 | 1.13 | 1.26  |

(Normalized to  $T_J = 25^\circ\text{C}$ ,  $V_{CCA}/V_{CCI} = 5.0\text{V}$ )



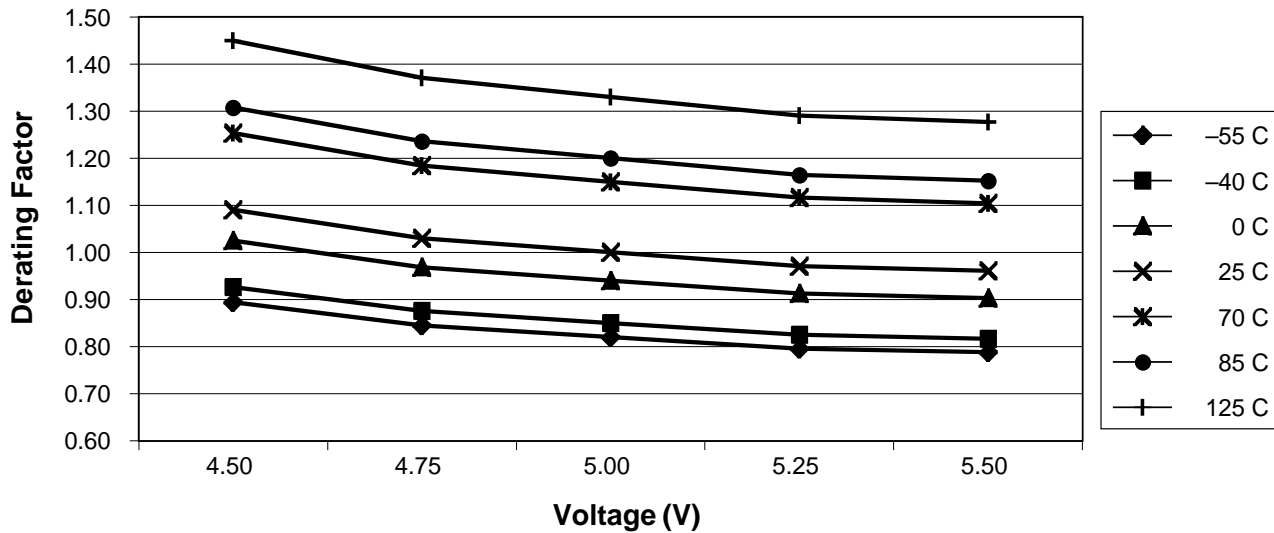
*Note:* This derating factor applies to all routing and propagation delays.

### 40MX Temperature and Voltage Derating Factors

(Normalized to  $T_J = 25^\circ\text{C}$ ,  $V_{CCA}/V_{CCI} = 5.0\text{V}$ )

| 40MX Voltage | Temperature |       |      |      |      |      |       |
|--------------|-------------|-------|------|------|------|------|-------|
|              | -55°C       | -40°C | 0°C  | 25°C | 70°C | 85°C | 125°C |
| 4.50         | 0.89        | 0.93  | 1.02 | 1.09 | 1.25 | 1.31 | 1.45  |
| 4.75         | 0.84        | 0.88  | 0.97 | 1.03 | 1.18 | 1.24 | 1.37  |
| 5.00         | 0.82        | 0.85  | 0.94 | 1.00 | 1.15 | 1.20 | 1.33  |
| 5.25         | 0.80        | 0.82  | 0.91 | 0.97 | 1.12 | 1.16 | 1.29  |
| 5.50         | 0.79        | 0.82  | 0.90 | 0.96 | 1.10 | 1.15 | 1.28  |

40MX Junction Temperature and Voltage Derating Curves  
(Normalized to  $T_J = 25^\circ\text{C}$ ,  $V_{CCA}/V_{CCI} = 5.0\text{V}$ )



Note: This derating factor applies to all routing and propagation delays.



## PCI System Timing Specification

Table 3 and Table 4 list the critical PCI timing parameters and the corresponding timing parameter for the MX PCI-compliant devices.

## PCI Models

Actel provides synthesizable VHDL and Verilog-HDL models for a PCI Target interface, a PCI Target and Target+DMA Master interface. Contact your Actel sales representative for more details.

**Table 3 • Clock Specification for 33 MHz PCI**

| Symbol            | Parameter      | PCI  |      | A42MX24 |      | A42MX36 |      | Units |
|-------------------|----------------|------|------|---------|------|---------|------|-------|
|                   |                | Min. | Max. | Min.    | Max. | Min.    | Max. |       |
| T <sub>CYC</sub>  | CLK Cycle Time | 30   | —    | 4.0     | —    | 4.0     | —    | ns    |
| T <sub>HIGH</sub> | CLK High Time  | 11   | —    | 1.9     | —    | 1.9     | —    | ns    |
| T <sub>LOW</sub>  | CLK Low Time   | 11   | —    | 1.9     | —    | 1.9     | —    | ns    |

**Table 4 • Timing Parameters for 33 MHz PCI**

| Symbol                | Parameter                               | PCI    |      | A42MX24 |                  | A42MX36 |                  | Units |
|-----------------------|---|--------|------|---------|------------------|---------|------------------|-------|
|                       |   | Min.   | Max. | Min.    | Max.             | Min.    | Max.             |       |
| T <sub>VAL</sub>      | CLK to Signal Valid—Bused Signals       | 2      | 11   | 2.0     | 9.0              | 2.0     | 9.0              | ns    |
| T <sub>VAL(PTP)</sub> | CLK to Signal Valid—Point-to-Point      | 2      | 12   | 2.0     | 9.0              | 2.0     | 9.0              | ns    |
| T <sub>ON</sub>       | Float to Active                         | 2      | —    | 2.0     | 4.0              | 2.0     | 4.0              | ns    |
| T <sub>OFF</sub>      | Active to Float                         | —      | 28   | —       | 8.3 <sup>1</sup> | —       | 8.3 <sup>1</sup> | ns    |
| T <sub>SU</sub>       | Input Set-Up Time to CLK—Bused Signals  | 7      | —    | 1.5     | —                | 1.5     | —                | ns    |
| T <sub>SU(PTP)</sub>  | Input Set-Up Time to CLK—Point-to-Point | 10, 12 | —    | 1.5     | —                | 1.5     | —                | ns    |
| T <sub>H</sub>        | Input Hold to CLK                       | 0      | —    | 0       | —                | 0       | —                | ns    |

**Note:**

1. T<sub>OFF</sub> is system dependent. MX PCI devices have 7.4 ns turn-off time, reflection is typically an additional 10 ns.

**A40MX02 Timing Characteristics (Nominal 5.0V Operation)**
**(Worst-Case Commercial Conditions, V<sub>CC</sub> = 4.75V, T<sub>J</sub> = 70°C)**

|  |  | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      |       |
|--|--|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
| Parameter  | Description                                  | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. | Units |
| <b>Logic Module Propagation Delays</b>                   |  |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>PD1</sub>   | Single Module                                |            | 1.2  |            | 1.4  |            | 1.6  |             | 1.9  |            | 2.7  | ns    |
| t <sub>PD2</sub>   | Dual-Module Macros                           |            | 2.7  |            | 3.1  |            | 3.5  |             | 4.1  |            | 5.7  | ns    |
| t <sub>CO</sub>  | Sequential Clock-to-Q                        |            | 1.2  |            | 1.4  |            | 1.6  |             | 1.9  |            | 2.7  | ns    |
| t <sub>GO</sub>  | Latch G-to-Q                                 |            | 1.2  |            | 1.4  |            | 1.6  |             | 1.9  |            | 2.7  | ns    |
| t <sub>RS</sub>  | Flip-Flop (Latch) Reset-to-Q                 |            | 1.2  |            | 1.4  |            | 1.6  |             | 1.9  |            | 2.7  | ns    |
| <b>Logic Module Predicted Routing Delays<sup>1</sup></b> |  |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>RD1</sub>   | FO=1 Routing Delay                           |            | 1.3  |            | 1.5  |            | 1.7  |             | 2.0  |            | 2.8  | ns    |
| t <sub>RD2</sub>   | FO=2 Routing Delay                           |            | 1.8  |            | 2.1  |            | 2.4  |             | 2.8  |            | 3.9  | ns    |
| t <sub>RD3</sub>   | FO=3 Routing Delay                           |            | 2.3  |            | 2.7  |            | 3.0  |             | 3.6  |            | 5.0  | ns    |
| t <sub>RD4</sub>   | FO=4 Routing Delay                           |            | 2.9  |            | 3.3  |            | 3.7  |             | 4.4  |            | 6.1  | ns    |
| t <sub>RD8</sub>   | FO=8 Routing Delay                           |            | 4.9  |            | 5.7  |            | 6.5  |             | 7.6  |            | 10.6 | ns    |
| <b>Logic Module Sequential Timing<sup>2</sup></b>        |  |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>SUD</sub>   | Flip-Flop (Latch) Data Input Set-Up          | 3.1        |      | 3.5        |      | 4.0        |      | 4.7         |      | 6.6        |      | ns    |
| t <sub>HD</sub> <sup>3</sup>                             | Flip-Flop (Latch) Data Input Hold            | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>SUENA</sub>                                       | Flip-Flop (Latch) Enable Set-Up              | 3.1        |      | 3.5        |      | 4.0        |      | 4.7         |      | 6.6        |      | ns    |
| t <sub>HENA</sub>  | Flip-Flop (Latch) Enable Hold                | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>WCLKA</sub>                                       | Flip-Flop (Latch) Clock Active Pulse Width   | 3.3        |      | 3.8        |      | 4.3        |      | 5.0         |      | 7.0        |      | ns    |
| t <sub>WASYN</sub>                                       | Flip-Flop (Latch) Asynchronous Pulse Width   | 3.3        |      | 3.8        |      | 4.3        |      | 5.0         |      | 7.0        |      | ns    |
| t <sub>A</sub>   | Flip-Flop Clock Input Period                 | 4.8        |      | 5.6        |      | 6.3        |      | 7.5         |      | 10.4       |      | ns    |
| f <sub>MAX</sub>   | Flip-Flop (Latch) Clock Frequency (FO = 128) |            | 181  |            | 168  |            | 154  |             | 134  |            | 80   | MHz   |

**Notes:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Series or later Timer to check the hold time for this macro.

**A40MX02 Timing Characteristics (Nominal 5.0V Operation) (continued)****(Worst-Case Commercial Conditions,  $V_{CC} = 4.75V$ ,  $T_J = 70^\circ C$ )**

| Parameter Description                                    |                          |          | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      | Units |
|--|--------------------------|----------|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
|  |                          |          | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. |       |
| <b>Input Module Propagation Delays</b>                   |                          |          |            |      |            |      |            |      |             |      |            |      |       |
| $t_{INYH}$   | Pad-to-Y HIGH            |          | 0.7        |      | 0.8        |      | 0.9        |      | 1.1         |      | 1.5        | ns   |       |
| $t_{INYL}$   | Pad-to-Y LOW             |          | 0.6        |      | 0.7        |      | 0.8        |      | 1.0         |      | 1.3        | ns   |       |
| <b>Input Module Predicted Routing Delays<sup>1</sup></b> |                          |          |            |      |            |      |            |      |             |      |            |      |       |
| $t_{IRD1}$   | FO=1 Routing Delay       |          | 2.1        |      | 2.4        |      | 2.2        |      | 3.2         |      | 4.5        | ns   |       |
| $t_{IRD2}$   | FO=2 Routing Delay       |          | 2.6        |      | 3.0        |      | 3.4        |      | 4.0         |      | 5.6        | ns   |       |
| $t_{IRD3}$   | FO=3 Routing Delay       |          | 3.1        |      | 3.6        |      | 4.1        |      | 4.8         |      | 6.7        | ns   |       |
| $t_{IRD4}$   | FO=4 Routing Delay       |          | 3.6        |      | 4.2        |      | 4.8        |      | 5.6         |      | 7.8        | ns   |       |
| $t_{IRD8}$   | FO=8 Routing Delay       |          | 5.7        |      | 6.6        |      | 7.5        |      | 8.8         |      | 12.4       | ns   |       |
| <b>Global Clock Network</b>                              |                          |          |            |      |            |      |            |      |             |      |            |      |       |
| $t_{CKH}$  | Input Low to HIGH        | FO = 16  | 4.6        |      | 5.3        |      | 6.0        |      | 7.0         |      | 9.8        | ns   |       |
|  |                          | FO = 128 | 4.6        |      | 5.3        |      | 6.0        |      | 7.0         |      | 9.8        |      |       |
| $t_{CKL}$  | Input High to LOW        | FO = 16  | 4.8        |      | 5.6        |      | 6.3        |      | 7.4         |      | 10.4       | ns   |       |
|  |                          | FO = 128 | 4.8        |      | 5.6        |      | 6.3        |      | 7.4         |      | 10.4       |      |       |
| $t_{PWH}$  | Minimum Pulse Width HIGH | FO = 16  | 2.2        |      | 2.6        |      | 2.9        |      | 3.4         |      | 4.8        | ns   |       |
|  |                          | FO = 128 | 2.4        |      | 2.7        |      | 3.1        |      | 3.6         |      | 5.1        |      |       |
| $t_{PWL}$  | Minimum Pulse Width LOW  | FO = 16  | 2.2        |      | 2.6        |      | 2.9        |      | 3.4         |      | 4.8        | ns   |       |
|  |                          | FO = 128 | 2.4        |      | 2.7        |      | 3.01       |      | 3.6         |      | 5.1        |      |       |
| $t_{CKSW}$   | Maximum Skew             | FO = 16  |            | 0.4  |            | 0.5  |            | 0.5  |             | 0.6  |            | 0.8  | ns    |
|  |                          | FO = 128 |            | 0.5  |            | 0.6  |            | 0.7  |             | 0.8  |            | 1.2  |       |
| $t_P$  | Minimum Period           | FO = 16  | 4.7        |      | 5.4        |      | 6.1        |      | 7.2         |      | 10.0       | ns   |       |
|  |                          | FO = 128 | 4.8        |      | 5.6        |      | 6.3        |      | 7.5         |      | 10.4       |      |       |
| $f_{MAX}$  | Maximum Frequency        | FO = 16  |            | 188  |            | 175  |            | 160  |             | 139  |            | 83   | MHz   |
|  |                          | FO = 128 |            | 181  |            | 168  |            | 154  |             | 134  |            | 80   |       |

**Note:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

**A40MX02 Timing Characteristics (Nominal 5.0V Operation) (continued)**
**(Worst-Case Commercial Conditions,  $V_{CC} = 4.75V$ ,  $T_J = 70^\circ C$ )**

| Parameter Description                        | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      | Units |
|--|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
|  | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. |       |
| <b>TTL Output Module Timing<sup>1</sup></b>  |            |      |            |      |            |      |             |      |            |      |       |
| $t_{DLH}$ Data-to-Pad HIGH                   |            | 3.3  |            | 3.8  |            | 4.3  |             | 5.1  |            | 7.2  | ns    |
| $t_{DHL}$ Data-to-Pad LOW                    |            | 4.0  |            | 4.6  |            | 5.2  |             | 6.1  |            | 8.6  | ns    |
| $t_{ENZH}$ Enable Pad Z to HIGH              |            | 3.7  |            | 4.3  |            | 4.9  |             | 5.8  |            | 8.0  | ns    |
| $t_{ENZL}$ Enable Pad Z to LOW               |            | 4.7  |            | 5.4  |            | 6.1  |             | 7.2  |            | 10.1 | ns    |
| $t_{ENHZ}$ Enable Pad HIGH to Z              |            | 7.9  |            | 9.1  |            | 10.4 |             | 12.2 |            | 17.1 | ns    |
| $t_{ENLZ}$ Enable Pad LOW to Z               |            | 5.9  |            | 6.8  |            | 7.7  |             | 9.0  |            | 12.6 | ns    |
| $d_{TLH}$ Delta LOW to HIGH                  |            | 0.02 |            | 0.02 |            | 0.03 |             | 0.03 |            | 0.04 | ns/pF |
| $d_{THL}$ Delta HIGH to LOW                  |            | 0.03 |            | 0.03 |            | 0.03 |             | 0.04 |            | 0.06 | ns/pF |
| <b>CMOS Output Module Timing<sup>1</sup></b> |            |      |            |      |            |      |             |      |            |      |       |
| $t_{DLH}$ Data-to-Pad HIGH                   |            | 3.9  |            | 4.5  |            | 5.1  |             | 6.05 |            | 8.5  | ns    |
| $t_{DHL}$ Data-to-Pad LOW                    |            | 3.4  |            | 3.9  |            | 4.4  |             | 5.2  |            | 7.3  | ns    |
| $t_{ENZH}$ Enable Pad Z to HIGH              |            | 3.4  |            | 3.9  |            | 4.4  |             | 5.2  |            | 7.3  | ns    |
| $t_{ENZL}$ Enable Pad Z to LOW               |            | 4.9  |            | 5.6  |            | 6.4  |             | 7.5  |            | 10.5 | ns    |
| $t_{ENHZ}$ Enable Pad HIGH to Z              |            | 7.9  |            | 9.1  |            | 10.4 |             | 12.2 |            | 17.0 | ns    |
| $t_{ENLZ}$ Enable Pad LOW to Z               |            | 5.9  |            | 6.8  |            | 7.7  |             | 9.0  |            | 12.6 | ns    |
| $d_{TLH}$ Delta LOW to HIGH                  |            | 0.03 |            | 0.04 |            | 0.04 |             | 0.05 |            | 0.07 | ns/pF |
| $d_{THL}$ Delta HIGH to LOW                  |            | 0.02 |            | 0.02 |            | 0.03 |             | 0.03 |            | 0.04 | ns/pF |

**Note:**

1. Delays based on 35 pF loading.

**A40MX02 Timing Characteristics (Nominal 3.3V Operation)****(Worst-Case Commercial Conditions,  $V_{CC} = 3.0V$ ,  $T_J = 70^{\circ}C$ )**

|  |  | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      |       |
|--|--|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
| Parameter  | Description                                  | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. | Units |
| <b>Logic Module Propagation Delays</b>                   |  |            |      |            |      |            |      |             |      |            |      |       |
| $t_{PD1}$  | Single Module                                |            | 1.7  |            | 2.0  |            | 2.3  |             | 2.7  |            | 3.7  | ns    |
| $t_{PD2}$  | Dual-Module Macros                           |            | 3.7  |            | 4.3  |            | 4.9  |             | 5.7  |            | 8.0  | ns    |
| $t_{CO}$   | Sequential Clock-to-Q                        |            | 1.7  |            | 2.0  |            | 2.3  |             | 2.7  |            | 3.7  | ns    |
| $t_{GO}$   | Latch G-to-Q                                 |            | 1.7  |            | 2.0  |            | 2.3  |             | 2.7  |            | 3.7  | ns    |
| $t_{RS}$   | Flip-Flop (Latch) Reset-to-Q                 |            | 1.7  |            | 2.0  |            | 2.3  |             | 2.7  |            | 3.7  | ns    |
| <b>Logic Module Predicted Routing Delays<sup>1</sup></b> |  |            |      |            |      |            |      |             |      |            |      |       |
| $t_{RD1}$  | FO=1 Routing Delay                           |            | 2.0  |            | 2.2  |            | 2.5  |             | 3.0  |            | 4.2  | ns    |
| $t_{RD2}$  | FO=2 Routing Delay                           |            | 2.7  |            | 3.1  |            | 3.5  |             | 4.1  |            | 5.7  | ns    |
| $t_{RD3}$  | FO=3 Routing Delay                           |            | 3.4  |            | 3.9  |            | 4.4  |             | 5.2  |            | 7.3  | ns    |
| $t_{RD4}$  | FO=4 Routing Delay                           |            | 4.2  |            | 4.8  |            | 5.4  |             | 6.3  |            | 8.9  | ns    |
| $t_{RD8}$  | FO=8 Routing Delay                           |            | 7.1  |            | 8.2  |            | 9.2  |             | 10.9 |            | 15.2 | ns    |
| <b>Logic Module Sequential Timing<sup>2</sup></b>        |  |            |      |            |      |            |      |             |      |            |      |       |
| $t_{SUD}$  | Flip-Flop (Latch) Data Input Set-Up          | 4.3        |      | 4.9        |      | 5.6        |      | 6.6         |      | 9.2        |      | ns    |
| $t_{HD}^3$   | Flip-Flop (Latch) Data Input Hold            | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| $t_{SUENA}$  | Flip-Flop (Latch) Enable Set-Up              | 4.3        |      | 4.9        |      | 5.6        |      | 6.6         |      | 9.2        |      | ns    |
| $t_{HENA}$   | Flip-Flop (Latch) Enable Hold                | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| $t_{WCLKA}$  | Flip-Flop (Latch) Clock Active Pulse Width   | 4.6        |      | 5.3        |      | 6.0        |      | 7.0         |      | 9.8        |      | ns    |
| $t_{WASYN}$  | Flip-Flop (Latch) Asynchronous Pulse Width   | 4.6        |      | 5.3        |      | 6.0        |      | 7.0         |      | 9.8        |      | ns    |
| $t_A$  | Flip-Flop Clock Input Period                 | 6.8        |      | 7.8        |      | 8.9        |      | 10.4        |      | 14.6       |      | ns    |
| $f_{MAX}$  | Flip-Flop (Latch) Clock Frequency (FO = 128) |            | 109  |            | 101  |            | 92   |             | 80   |            | 48   | MHz   |

**Notes:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Series or later Timer to check the hold time for this macro.

**A40MX02 Timing Characteristics (Nominal 3.3V Operation) (continued)**
**(Worst-Case Commercial Conditions,  $V_{CC} = 3.0V$ ,  $T_J = 70^\circ C$ )**

| Parameter Description                                    |                             |          | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      | Units |
|--|-----------------------------|----------|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
|  |                             |          | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. |       |
| <b>Input Module Propagation Delays</b>                   |                             |          |            |      |            |      |            |      |             |      |            |      |       |
| $t_{INYH}$   | Pad-to-Y HIGH               |          |            | 1.0  |            | 1.1  |            | 1.3  |             | 1.5  |            | 2.1  | ns    |
| $t_{INYL}$   | Pad-to-Y LOW                |          |            | 0.9  |            | 1.0  |            | 1.1  |             | 1.3  |            | 1.9  | ns    |
| <b>Input Module Predicted Routing Delays<sup>1</sup></b> |                             |          |            |      |            |      |            |      |             |      |            |      |       |
| $t_{IRD1}$   | FO=1 Routing Delay          |          |            | 2.9  |            | 3.4  |            | 3.8  |             | 4.5  |            | 6.3  | ns    |
| $t_{IRD2}$   | FO=2 Routing Delay          |          |            | 3.6  |            | 4.2  |            | 4.8  |             | 5.6  |            | 7.8  | ns    |
| $t_{IRD3}$   | FO=3 Routing Delay          |          |            | 4.4  |            | 5.0  |            | 5.7  |             | 6.7  |            | 9.4  | ns    |
| $t_{IRD4}$   | FO=4 Routing Delay          |          |            | 5.1  |            | 5.9  |            | 6.7  |             | 7.8  |            | 11.0 | ns    |
| $t_{IRD8}$   | FO=8 Routing Delay          |          |            | 8.0  |            | 9.26 |            | 10.5 |             | 12.6 |            | 17.3 | ns    |
| <b>Global Clock Network</b>                              |                             |          |            |      |            |      |            |      |             |      |            |      |       |
| $t_{CKH}$  | Input LOW to HIGH           | FO = 16  |            | 6.4  |            | 7.4  |            | 8.3  |             | 9.8  |            | 13.7 | ns    |
|  |                             | FO = 128 |            | 6.4  |            | 7.4  |            | 8.3  |             | 9.8  |            | 13.7 |       |
| $t_{CKL}$  | Input HIGH to LOW           | FO = 16  |            | 6.7  |            | 7.8  |            | 8.8  |             | 10.4 |            | 14.5 | ns    |
|  |                             | FO = 128 |            | 6.7  |            | 7.8  |            | 8.8  |             | 10.4 |            | 14.5 |       |
| $t_{PWH}$  | Minimum Pulse Width<br>HIGH | FO = 16  | 3.1        |      | 3.6        |      | 4.1        |      | 4.8         |      | 6.7        | ns   |       |
|  |                             | FO = 128 | 3.3        |      | 3.8        |      | 4.3        |      | 5.1         |      | 7.1        |      |       |
| $t_{PWL}$  | Minimum Pulse Width<br>LOW  | FO = 16  | 3.1        |      | 3.6        |      | 4.1        |      | 4.8         |      | 6.7        | ns   |       |
|  |                             | FO = 128 | 3.3        |      | 3.8        |      | 4.3        |      | 5.1         |      | 7.1        |      |       |
| $t_{CKSW}$   | Maximum Skew                | FO = 16  |            | 0.6  |            | 0.6  |            | 0.7  |             | 0.8  |            | 1.2  | ns    |
|  |                             | FO = 128 |            | 0.8  |            | 0.9  |            | 1.0  |             | 1.2  |            | 1.6  |       |
| $t_P$  | Minimum Period              | FO = 16  | 6.5        |      | 7.5        |      | 8.5        |      | 10.1        |      | 14.1       | ns   |       |
|  |                             | FO = 128 | 6.8        |      | 7.8        |      | 8.9        |      | 10.4        |      | 14.6       |      |       |
| $f_{MAX}$  | Maximum Frequency           | FO = 16  |            | 113  |            | 105  |            | 96   |             | 83   |            | 50   | MHz   |
|  |                             | FO = 128 |            | 109  |            | 101  |            | 92   |             | 80   |            | 48   |       |

**Note:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

**A40MX02 Timing Characteristics (Nominal 3.3V Operation) (continued)****(Worst-Case Commercial Conditions,  $V_{CC} = 3.0V$ ,  $T_J = 70^{\circ}C$ )**

| Parameter Description                        |                      | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      | Units |
|--|----------------------|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
|  |                      | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. |       |
| <b>TTL Output Module Timing<sup>1</sup></b>  |                      |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>DLH</sub>                             | Data-to-Pad HIGH     |            | 4.7  |            | 5.4  |            | 6.1  |             | 7.2  |            | 10.0 | ns    |
| t <sub>DHL</sub>                             | Data-to-Pad LOW      |            | 5.6  |            | 6.4  |            | 7.3  |             | 8.6  |            | 12.0 | ns    |
| t <sub>ENZH</sub>                            | Enable Pad Z to HIGH |            | 5.2  |            | 6.0  |            | 6.8  |             | 8.1  |            | 11.3 | ns    |
| t <sub>ENZL</sub>                            | Enable Pad Z to LOW  |            | 6.6  |            | 7.6  |            | 8.6  |             | 10.1 |            | 14.1 | ns    |
| t <sub>ENHZ</sub>                            | Enable Pad HIGH to Z |            | 11.1 |            | 12.8 |            | 14.5 |             | 17.1 |            | 23.9 | ns    |
| t <sub>ENLZ</sub>                            | Enable Pad LOW to Z  |            | 8.2  |            | 9.5  |            | 10.7 |             | 12.6 |            | 17.7 | ns    |
| d <sub>TLH</sub>                             | Delta LOW to HIGH    |            | 0.03 |            | 0.03 |            | 0.04 |             | 0.04 |            | 0.06 | ns/pF |
| d <sub>THL</sub>                             | Delta HIGH to LOW    |            | 0.04 |            | 0.04 |            | 0.05 |             | 0.06 |            | 0.08 | ns/pF |
| <b>CMOS Output Module Timing<sup>1</sup></b> |                      |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>DLH</sub>                             | Data-to-Pad HIGH     |            | 5.5  |            | 6.4  |            | 7.2  |             | 8.5  |            | 11.9 | ns    |
| t <sub>DHL</sub>                             | Data-to-Pad LOW      |            | 4.8  |            | 5.5  |            | 6.2  |             | 7.3  |            | 10.2 | ns    |
| t <sub>ENZH</sub>                            | Enable Pad Z to HIGH |            | 4.7  |            | 5.5  |            | 6.2  |             | 7.3  |            | 10.2 | ns    |
| t <sub>ENZL</sub>                            | Enable Pad Z to LOW  |            | 6.8  |            | 7.9  |            | 8.9  |             | 10.5 |            | 14.7 | ns    |
| t <sub>ENHZ</sub>                            | Enable Pad HIGH to Z |            | 11.1 |            | 12.8 |            | 14.5 |             | 17.1 |            | 23.9 | ns    |
| t <sub>ENLZ</sub>                            | Enable Pad LOW to Z  |            | 8.2  |            | 9.5  |            | 10.7 |             | 12.6 |            | 17.7 | ns    |
| d <sub>TLH</sub>                             | Delta LOW to HIGH    |            | 0.05 |            | 0.05 |            | 0.06 |             | 0.07 |            | 0.10 | ns/pF |
| d <sub>THL</sub>                             | Delta HIGH to LOW    |            | 0.03 |            | 0.03 |            | 0.04 |             | 0.04 |            | 0.06 | ns/pF |

**Note:**

1. Delays based on 35 pF loading.

**A40MX04 Timing Characteristics (Nominal 5.0V Operation)**
**(Worst-Case Commercial Conditions, V<sub>CC</sub> = 4.75V, T<sub>J</sub> = 70°C)**

|  |  | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      |       |
|--|--|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
| Parameter  | Description                                  | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. | Units |
| <b>Logic Module Propagation Delays</b>                   |  |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>PD1</sub>   | Single Module                                |            | 1.2  |            | 1.4  |            | 1.6  |             | 1.9  |            | 2.7  | ns    |
| t <sub>PD2</sub>   | Dual-Module Macros                           |            | 2.3  |            | 3.1  |            | 3.5  |             | 4.1  |            | 5.7  | ns    |
| t <sub>CO</sub>  | Sequential Clock-to-Q                        |            | 1.2  |            | 1.4  |            | 1.6  |             | 1.9  |            | 2.7  | ns    |
| t <sub>GO</sub>  | Latch G-to-Q                                 |            | 1.2  |            | 1.4  |            | 1.6  |             | 1.9  |            | 2.7  | ns    |
| t <sub>RS</sub>  | Flip-Flop (Latch) Reset-to-Q                 |            | 1.2  |            | 1.4  |            | 1.6  |             | 1.9  |            | 2.7  | ns    |
| <b>Logic Module Predicted Routing Delays<sup>1</sup></b> |  |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>RD1</sub>   | FO=1 Routing Delay                           |            | 1.2  |            | 1.6  |            | 1.8  |             | 2.1  |            | 3.0  | ns    |
| t <sub>RD2</sub>   | FO=2 Routing Delay                           |            | 1.9  |            | 2.2  |            | 2.5  |             | 2.9  |            | 4.1  | ns    |
| t <sub>RD3</sub>   | FO=3 Routing Delay                           |            | 2.4  |            | 2.8  |            | 3.2  |             | 3.7  |            | 5.2  | ns    |
| t <sub>RD4</sub>   | FO=4 Routing Delay                           |            | 2.9  |            | 3.4  |            | 3.9  |             | 4.5  |            | 6.3  | ns    |
| t <sub>RD8</sub>   | FO=8 Routing Delay                           |            | 5.0  |            | 5.8  |            | 6.6  |             | 7.8  |            | 10.9 | ns    |
| <b>Logic Module Sequential Timing<sup>2</sup></b>        |  |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>SUD</sub>   | Flip-Flop (Latch) Data Input Set-Up          | 3.1        |      | 3.5        |      | 4.0        |      | 4.7         |      | 6.6        |      | ns    |
| t <sub>HD</sub> <sup>3</sup>                             | Flip-Flop (Latch) Data Input Hold            | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>SUENA</sub>                                       | Flip-Flop (Latch) Enable Set-Up              | 3.1        |      | 3.5        |      | 4.0        |      | 4.7         |      | 6.6        |      | ns    |
| t <sub>HENA</sub>  | Flip-Flop (Latch) Enable Hold                | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>WCLKA</sub>                                       | Flip-Flop (Latch) Clock Active Pulse Width   | 3.3        |      | 3.8        |      | 4.3        |      | 5.0         |      | 7.0        |      | ns    |
| t <sub>WASYN</sub>                                       | Flip-Flop (Latch) Asynchronous Pulse Width   | 3.3        |      | 3.8        |      | 4.3        |      | 5.0         |      | 7.0        |      | ns    |
| t <sub>A</sub>   | Flip-Flop Clock Input Period                 | 4.8        |      | 5.6        |      | 6.3        |      | 7.5         |      | 10.4       |      | ns    |
| f <sub>MAX</sub>   | Flip-Flop (Latch) Clock Frequency (FO = 128) |            | 181  |            | 167  |            | 154  |             | 134  |            | 80   | MHz   |

**Notes:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Series or later Timer to check the hold time for this macro.



**A40MX04 Timing Characteristics (Nominal 5.0V Operation) (continued)****(Worst-Case Commercial Conditions,  $V_{CC} = 4.75V$ ,  $T_J = 70^\circ C$ )**

| Parameter Description                                    |                          |          | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      | Units |
|--|--------------------------|----------|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
|  |                          |          | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. |       |
| <b>Input Module Propagation Delays</b>                   |                          |          |            |      |            |      |            |      |             |      |            |      |       |
| $t_{INYH}$   | Pad-to-Y HIGH            |          | 0.7        |      | 0.8        |      | 0.9        |      | 1.1         |      | 1.5        | ns   |       |
| $t_{INYL}$   | Pad-to-Y LOW             |          | 0.6        |      | 0.7        |      | 0.8        |      | 1.0         |      | 1.3        | ns   |       |
| <b>Input Module Predicted Routing Delays<sup>1</sup></b> |                          |          |            |      |            |      |            |      |             |      |            |      |       |
| $t_{IRD1}$   | FO=1 Routing Delay       |          | 2.1        |      | 2.4        |      | 2.2        |      | 3.2         |      | 4.5        | ns   |       |
| $t_{IRD2}$   | FO=2 Routing Delay       |          | 2.6        |      | 3.0        |      | 3.4        |      | 4.0         |      | 5.6        | ns   |       |
| $t_{IRD3}$   | FO=3 Routing Delay       |          | 3.1        |      | 3.6        |      | 4.1        |      | 4.8         |      | 6.7        | ns   |       |
| $t_{IRD4}$   | FO=4 Routing Delay       |          | 3.6        |      | 4.2        |      | 4.8        |      | 5.6         |      | 7.8        | ns   |       |
| $t_{IRD8}$   | FO=8 Routing Delay       |          | 5.7        |      | 6.6        |      | 7.5        |      | 8.8         |      | 12.4       | ns   |       |
| <b>Global Clock Network</b>                              |                          |          |            |      |            |      |            |      |             |      |            |      |       |
| $t_{CKH}$  | Input LOW to HIGH        | FO = 16  | 4.6        |      | 5.3        |      | 6.0        |      | 7.1         |      | 9.9        | ns   |       |
|  |                          | FO = 128 | 4.6        |      | 5.3        |      | 6.0        |      | 7.1         |      | 9.9        |      |       |
| $t_{CKL}$  | Input HIGH to LOW        | FO = 16  | 4.8        |      | 5.6        |      | 6.3        |      | 7.5         |      | 10.4       | ns   |       |
|  |                          | FO = 128 | 4.8        |      | 5.6        |      | 6.3        |      | 7.5         |      | 10.4       |      |       |
| $t_{PWH}$  | Minimum Pulse Width HIGH | FO = 16  | 2.2        |      | 2.6        |      | 2.9        |      | 3.4         |      | 4.8        | ns   |       |
|  |                          | FO = 128 | 2.4        |      | 2.7        |      | 3.1        |      | 3.6         |      | 5.1        |      |       |
| $t_{PWL}$  | Minimum Pulse Width LOW  | FO = 16  | 2.2        |      | 2.6        |      | 2.9        |      | 3.4         |      | 4.8        | ns   |       |
|  |                          | FO = 128 | 2.4        |      | 2.7        |      | 3.1        |      | 3.6         |      | 5.1        |      |       |
| $t_{CKSW}$   | Maximum Skew             | FO = 16  |            | 0.4  |            | 0.5  |            | 0.5  |             | 0.6  |            | 0.8  | ns    |
|  |                          | FO = 128 |            | 0.5  |            | 0.6  |            | 0.7  |             | 0.8  |            | 1.2  |       |
| $t_P$  | Minimum Period           | FO = 16  | 4.7        |      | 5.4        |      | 6.1        |      | 7.2         |      | 10.1       | ns   |       |
|  |                          | FO = 128 | 4.8        |      | 5.6        |      | 6.3        |      | 7.5         |      | 10.4       |      |       |
| $f_{MAX}$  | Maximum Frequency        | FO = 16  |            | 188  |            | 175  |            | 160  |             | 139  |            | 83   | MHz   |
|  |                          | FO = 128 |            | 181  |            | 168  |            | 154  |             | 134  |            | 80   |       |

**Note:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

**A40MX04 Timing Characteristics (Nominal 5.0V Operation) (continued)**
**(Worst-Case Commercial Conditions,  $V_{CC} = 4.75V$ ,  $T_J = 70^\circ C$ )**

| Parameter Description                        | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      | Units |
|--|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
|  | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. |       |
| <b>TTL Output Module Timing<sup>1</sup></b>  |            |      |            |      |            |      |             |      |            |      |       |
| $t_{DLH}$ Data-to-Pad HIGH                   |            | 3.3  |            | 3.8  |            | 4.3  |             | 5.1  |            | 7.2  | ns    |
| $t_{DHL}$ Data-to-Pad LOW                    |            | 4.0  |            | 4.6  |            | 5.2  |             | 6.1  |            | 8.6  | ns    |
| $t_{ENZH}$ Enable Pad Z to HIGH              |            | 3.7  |            | 4.3  |            | 4.9  |             | 5.8  |            | 8.1  | ns    |
| $t_{ENZL}$ Enable Pad Z to LOW               |            | 4.7  |            | 5.4  |            | 6.1  |             | 7.2  |            | 10.1 | ns    |
| $t_{ENHZ}$ Enable Pad HIGH to Z              |            | 7.9  |            | 9.1  |            | 10.4 |             | 12.2 |            | 17.1 | ns    |
| $t_{ENLZ}$ Enable Pad LOW to Z               |            | 5.9  |            | 6.8  |            | 7.7  |             | 9.0  |            | 12.6 | ns    |
| $d_{TLH}$ Delta LOW to HIGH                  |            | 0.02 |            | 0.02 |            | 0.03 |             | 0.03 |            | 0.04 | ns/pF |
| $d_{THL}$ Delta HIGH to LOW                  |            | 0.02 |            | 0.03 |            | 0.03 |             | 0.04 |            | 0.06 | ns/pF |
| <b>CMOS Output Module Timing<sup>1</sup></b> |            |      |            |      |            |      |             |      |            |      |       |
| $t_{DLH}$ Data-to-Pad HIGH                   |            | 3.9  |            | 4.5  |            | 5.1  |             | 6.1  |            | 8.5  | ns    |
| $t_{DHL}$ Data-to-Pad LOW                    |            | 3.4  |            | 3.9  |            | 4.4  |             | 5.2  |            | 7.3  | ns    |
| $t_{ENZH}$ Enable Pad Z to HIGH              |            | 3.4  |            | 3.9  |            | 4.4  |             | 5.2  |            | 7.3  | ns    |
| $t_{ENZL}$ Enable Pad Z to LOW               |            | 4.9  |            | 5.6  |            | 6.4  |             | 7.5  |            | 10.5 | ns    |
| $t_{ENHZ}$ Enable Pad HIGH to Z              |            | 7.9  |            | 9.1  |            | 10.4 |             | 12.2 |            | 17.1 | ns    |
| $t_{ENLZ}$ Enable Pad LOW to Z               |            | 5.0  |            | 6.8  |            | 7.7  |             | 9.0  |            | 12.6 | ns    |
| $d_{TLH}$ Delta LOW to HIGH                  |            | 0.03 |            | 0.04 |            | 0.04 |             | 0.05 |            | 0.07 | ns/pF |
| $d_{THL}$ Delta HIGH to LOW                  |            | 0.02 |            | 0.02 |            | 0.03 |             | 0.03 |            | 0.04 | ns/pF |

**Note:**

1. Delays based on 35 pF loading.

**A40MX04 Timing Characteristics (Nominal 3.3V Operation)****(Worst-Case Commercial Conditions,  $V_{CC} = 3.0V$ ,  $T_J = 70^\circ C$ )**

|  |  | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      |       |
|--|--|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
| Parameter Description                                    |  | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. | Units |
| <b>Logic Module Propagation Delays</b>                   |  |            |      |            |      |            |      |             |      |            |      |       |
| $t_{PD1}$  | Single Module                                |            | 1.7  |            | 2.0  |            | 2.3  |             | 2.7  |            | 3.7  | ns    |
| $t_{PD2}$  | Dual-Module Macros                           |            | 3.7  |            | 4.3  |            | 4.9  |             | 5.7  |            | 8.0  | ns    |
| $t_{CO}$   | Sequential Clock-to-Q                        |            | 1.7  |            | 2.0  |            | 2.3  |             | 2.7  |            | 3.7  | ns    |
| $t_{GO}$   | Latch G-to-Q                                 |            | 1.7  |            | 2.0  |            | 2.3  |             | 2.7  |            | 3.7  | ns    |
| $t_{RS}$   | Flip-Flop (Latch) Reset-to-Q                 |            | 1.7  |            | 2.0  |            | 2.3  |             | 2.7  |            | 3.7  | ns    |
| <b>Logic Module Predicted Routing Delays<sup>1</sup></b> |  |            |      |            |      |            |      |             |      |            |      |       |
| $t_{RD1}$  | FO=1 Routing Delay                           |            | 1.9  |            | 2.2  |            | 2.5  |             | 3.0  |            | 4.2  | ns    |
| $t_{RD2}$  | FO=2 Routing Delay                           |            | 2.7  |            | 3.1  |            | 3.5  |             | 4.1  |            | 5.7  | ns    |
| $t_{RD3}$  | FO=3 Routing Delay                           |            | 3.4  |            | 3.9  |            | 4.4  |             | 5.2  |            | 7.3  | ns    |
| $t_{RD4}$  | FO=4 Routing Delay                           |            | 4.1  |            | 4.8  |            | 5.4  |             | 6.3  |            | 8.9  | ns    |
| $t_{RD8}$  | FO=8 Routing Delay                           |            | 7.1  |            | 8.1  |            | 9.2  |             | 10.9 |            | 15.2 | ns    |
| <b>Logic Module Sequential Timing<sup>2</sup></b>        |  |            |      |            |      |            |      |             |      |            |      |       |
| $t_{SUD}$  | Flip-Flop (Latch) Data Input Set-Up          | 4.3        |      | 5.0        |      | 5.6        |      | 6.6         |      | 9.2        |      | ns    |
| $t_{HD}^3$   | Flip-Flop (Latch) Data Input Hold            | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| $t_{SUENA}$  | Flip-Flop (Latch) Enable Set-Up              | 4.3        |      | 5.0        |      | 5.6        |      | 6.6         |      | 9.2        |      | ns    |
| $t_{HENA}$   | Flip-Flop (Latch) Enable Hold                | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| $t_{WCLKA}$  | Flip-Flop (Latch) Clock Active Pulse Width   | 4.6        |      | 5.3        |      | 5.6        |      | 7.0         |      | 9.8        |      | ns    |
| $t_{WASYN}$  | Flip-Flop (Latch) Asynchronous Pulse Width   | 4.6        |      | 5.3        |      | 5.6        |      | 7.0         |      | 9.8        |      | ns    |
| $t_A$  | Flip-Flop Clock Input Period                 | 6.8        |      | 7.8        |      | 8.9        |      | 10.4        |      | 14.6       |      | ns    |
| $f_{MAX}$  | Flip-Flop (Latch) Clock Frequency (FO = 128) |            | 109  |            | 101  |            | 92   |             | 80   |            | 48   | MHz   |

**Notes:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
2. Set-up times assume fanout of 3. Further testing information can be obtained from the Timer utility.
3. The hold time for the DFME1A macro may be greater than 0 ns. Use the Series or later Timer to check the hold time for this macro.

**A40MX04 Timing Characteristics (Nominal 3.3V Operation) (continued)**
**(Worst-Case Commercial Conditions,  $V_{CC} = 3.0V$ ,  $T_J = 70^\circ C$ )**

|  |                             |          | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      |       |
|--|-----------------------------|----------|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
| Parameter Description                                    |                             |          | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. | Units |
| <b>Input Module Propagation Delays</b>                   |                             |          |            |      |            |      |            |      |             |      |            |      |       |
| $t_{INYH}$   | Pad-to-Y HIGH               |          |            | 1.0  |            | 1.1  |            | 1.3  |             | 1.5  |            | 2.1  | ns    |
| $t_{INYL}$   | Pad-to-Y LOW                |          |            | 0.9  |            | 1.0  |            | 1.1  |             | 1.3  |            | 1.9  | ns    |
| <b>Input Module Predicted Routing Delays<sup>1</sup></b> |                             |          |            |      |            |      |            |      |             |      |            |      |       |
| $t_{IRD1}$   | FO=1 Routing Delay          |          |            | 2.9  |            | 3.34 |            | 3.8  |             | 4.5  |            | 6.3  | ns    |
| $t_{IRD2}$   | FO=2 Routing Delay          |          |            | 3.6  |            | 4.2  |            | 4.8  |             | 5.6  |            | 7.8  | ns    |
| $t_{IRD3}$   | FO=3 Routing Delay          |          |            | 4.4  |            | 5.0  |            | 5.7  |             | 6.7  |            | 9.4  | ns    |
| $t_{IRD4}$   | FO=4 Routing Delay          |          |            | 5.1  |            | 5.9  |            | 6.7  |             | 7.8  |            | 11.0 | ns    |
| $t_{IRD8}$   | FO=8 Routing Delay          |          |            | 8.0  |            | 9.3  |            | 10.5 |             | 12.4 |            | 17.2 | ns    |
| <b>Global Clock Network</b>                              |                             |          |            |      |            |      |            |      |             |      |            |      |       |
| $t_{CKH}$  | Input LOW to HIGH           | FO = 16  |            | 6.4  |            | 7.4  |            | 8.4  |             | 9.9  |            | 13.8 | ns    |
|  |                             | FO = 128 |            | 6.4  |            | 7.4  |            | 8.4  |             | 9.9  |            | 13.8 |       |
| $t_{CKL}$  | Input HIGH to LOW           | FO = 16  |            | 6.8  |            | 7.8  |            | 8.9  |             | 10.4 |            | 14.6 | ns    |
|  |                             | FO = 128 |            | 6.8  |            | 7.8  |            | 8.9  |             | 10.4 |            | 14.6 |       |
| $t_{PWH}$  | Minimum Pulse Width<br>HIGH | FO = 16  | 3.1        |      | 3.6        |      | 4.1        |      | 4.8         |      | 6.7        |      | ns    |
|  |                             | FO = 128 | 3.3        |      | 3.8        |      | 4.3        |      | 5.1         |      | 7.1        |      |       |
| $t_{PWL}$  | Minimum Pulse Width<br>LOW  | FO = 16  | 3.1        |      | 3.6        |      | 4.1        |      | 4.8         |      | 6.7        |      | ns    |
|  |                             | FO = 128 | 3.3        |      | 3.8        |      | 4.3        |      | 5.1         |      | 7.1        |      |       |
| $t_{CKSW}$   | Maximum Skew                | FO = 16  |            | 0.6  |            | 0.6  |            | 0.7  |             | 0.8  |            | 1.2  | ns    |
|  |                             | FO = 128 |            | 0.8  |            | 0.9  |            | 1.0  |             | 1.2  |            | 1.6  |       |
| $t_P$  | Minimum Period              | FO = 16  | 6.5        |      | 7.5        |      | 8.5        |      | 10.1        |      | 14.1       |      | ns    |
|  |                             | FO = 128 | 6.8        |      | 7.8        |      | 8.9        |      | 10.4        |      | 14.6       |      |       |
| $f_{MAX}$  | Maximum Frequency           | FO = 16  |            | 113  |            | 105  |            | 96   |             | 83   |            | 50   | MHz   |
|  |                             | FO = 128 |            | 109  |            | 101  |            | 92   |             | 80   |            | 48   |       |

**Note:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

**A40MX04 Timing Characteristics (Nominal 3.3V Operation) (continued)****(Worst-Case Commercial Conditions,  $V_{CC} = 3.0V$ ,  $T_J = 70^{\circ}C$ )**

| Parameter Description                        |                      | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      | Units |
|--|----------------------|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
|  |                      | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. |       |
| <b>TTL Output Module Timing<sup>1</sup></b>  |                      |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>DLH</sub>                             | Data-to-Pad HIGH     |            | 4.7  |            | 5.4  |            | 6.1  |             | 7.2  |            | 10.0 | ns    |
| t <sub>DHL</sub>                             | Data-to-Pad LOW      |            | 5.6  |            | 6.4  |            | 7.3  |             | 8.6  |            | 12.0 | ns    |
| t <sub>ENZH</sub>                            | Enable Pad Z to HIGH |            | 5.2  |            | 6.0  |            | 6.9  |             | 8.1  |            | 11.3 | ns    |
| t <sub>ENZL</sub>                            | Enable Pad Z to LOW  |            | 6.6  |            | 7.6  |            | 8.6  |             | 10.1 |            | 14.1 | ns    |
| t <sub>ENHZ</sub>                            | Enable Pad HIGH to Z |            | 11.1 |            | 12.8 |            | 14.5 |             | 17.1 |            | 23.9 | ns    |
| t <sub>ENLZ</sub>                            | Enable Pad LOW to Z  |            | 8.2  |            | 9.5  |            | 10.7 |             | 12.6 |            | 17.7 | ns    |
| d <sub>TLH</sub>                             | Delta LOW to HIGH    |            | 0.03 |            | 0.03 |            | 0.04 |             | 0.04 |            | 0.06 | ns/pF |
| d <sub>THL</sub>                             | Delta HIGH to LOW    |            | 0.04 |            | 0.04 |            | 0.05 |             | 0.06 |            | 0.08 | ns/pF |
| <b>CMOS Output Module Timing<sup>1</sup></b> |                      |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>DLH</sub>                             | Data-to-Pad HIGH     |            | 5.5  |            | 6.4  |            | 7.2  |             | 8.5  |            | 11.9 | ns    |
| t <sub>DHL</sub>                             | Data-to-Pad LOW      |            | 4.8  |            | 5.5  |            | 6.2  |             | 7.3  |            | 10.2 | ns    |
| t <sub>ENZH</sub>                            | Enable Pad Z to HIGH |            | 4.7  |            | 5.5  |            | 6.2  |             | 7.3  |            | 10.2 | ns    |
| t <sub>ENZL</sub>                            | Enable Pad Z to LOW  |            | 6.8  |            | 7.9  |            | 8.9  |             | 10.5 |            | 14.7 | ns    |
| t <sub>ENHZ</sub>                            | Enable Pad HIGH to Z |            | 11.1 |            | 12.8 |            | 14.5 |             | 17.1 |            | 23.9 | ns    |
| t <sub>ENLZ</sub>                            | Enable Pad LOW to Z  |            | 8.2  |            | 9.5  |            | 10.7 |             | 12.6 |            | 17.7 | ns    |
| d <sub>TLH</sub>                             | Delta LOW to HIGH    |            | 0.05 |            | 0.05 |            | 0.06 |             | 0.07 |            | 0.10 | ns/pF |
| d <sub>THL</sub>                             | Delta HIGH to LOW    |            | 0.03 |            | 0.03 |            | 0.04 |             | 0.04 |            | 0.06 | ns/pF |

**Note:**

1. Delays based on 35 pF loading.

**A42MX09 Timing Characteristics (Nominal 5.0V Operation)**
**(Worst-Case Commercial Conditions,  $V_{CC} = 4.75V$ ,  $T_J = 70^\circ C$ )**

|  |  | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      |       |
|--|--|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
| Parameter  | Description                                | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. | Units |
| <b>Logic Module Propagation Delays<sup>1</sup></b>       |  |            |      |            |      |            |      |             |      |            |      |       |
| $t_{PD1}$  | Single Module                              |            | 1.2  |            | 1.3  |            | 1.5  |             | 1.8  |            | 2.5  | ns    |
| $t_{CO}$   | Sequential Clock-to-Q                      |            | 1.3  |            | 1.4  |            | 1.6  |             | 1.9  |            | 2.7  | ns    |
| $t_{GO}$   | Latch G-to-Q                               |            | 1.2  |            | 1.4  |            | 1.6  |             | 1.8  |            | 2.6  | ns    |
| $t_{RS}$   | Flip-Flop (Latch) Reset-to-Q               |            | 1.2  |            | 1.6  |            | 1.8  |             | 2.1  |            | 2.9  | ns    |
| <b>Logic Module Predicted Routing Delays<sup>2</sup></b> |  |            |      |            |      |            |      |             |      |            |      |       |
| $t_{RD1}$  | FO=1 Routing Delay                         |            | 0.7  |            | 0.8  |            | 0.9  |             | 1.0  |            | 1.4  | ns    |
| $t_{RD2}$  | FO=2 Routing Delay                         |            | 0.9  |            | 1.0  |            | 1.2  |             | 1.4  |            | 1.9  | ns    |
| $t_{RD3}$  | FO=3 Routing Delay                         |            | 1.2  |            | 1.3  |            | 1.5  |             | 1.7  |            | 2.4  | ns    |
| $t_{RD4}$  | FO=4 Routing Delay                         |            | 1.4  |            | 1.5  |            | 1.7  |             | 2.0  |            | 2.9  | ns    |
| $t_{RD8}$  | FO=8 Routing Delay                         |            | 2.3  |            | 2.6  |            | 2.9  |             | 3.4  |            | 4.8  | ns    |
| <b>Logic Module Sequential Timing<sup>3, 4</sup></b>     |  |            |      |            |      |            |      |             |      |            |      |       |
| $t_{SUD}$  | Flip-Flop (Latch) Data Input Set-Up        | 0.3        |      | 0.4        |      | 0.4        |      | 0.5         |      | 0.7        |      | ns    |
| $t_{HD}$   | Flip-Flop (Latch) Data Input Hold          | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| $t_{SUENA}$  | Flip-Flop (Latch) Enable Set-Up            | 0.4        |      | 0.5        |      | 0.5        |      | 0.6         |      | 0.8        |      | ns    |
| $t_{HENA}$   | Flip-Flop (Latch) Enable Hold              | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| $t_{WCLKA}$  | Flip-Flop (Latch) Clock Active Pulse Width | 3.4        |      | 3.8        |      | 4.3        |      | 5.0         |      | 7.0        |      | ns    |
| $t_{WASYN}$  | Flip-Flop (Latch) Asynchronous Pulse Width | 4.5        |      | 4.9        |      | 5.6        |      | 6.6         |      | 9.2        |      | ns    |
| $t_A$  | Flip-Flop Clock Input Period               | 3.5        |      | 3.8        |      | 4.3        |      | 5.1         |      | 7.1        |      | ns    |
| $t_{INH}$  | Input Buffer Latch Hold                    | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| $t_{INSU}$   | Input Buffer Latch Set-Up                  | 0.3        |      | 0.3        |      | 0.4        |      | 0.4         |      | 0.6        |      | ns    |
| $t_{OUTH}$   | Output Buffer Latch Hold                   | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| $t_{OUTSU}$  | Output Buffer Latch Set-Up                 | 0.3        |      | 0.3        |      | 0.4        |      | 0.4         |      | 0.6        |      | ns    |
| $f_{MAX}$  | Flip-Flop (Latch) Clock Frequency          |            | 268  |            | 244  |            | 224  |             | 195  |            | 117  | MHz   |

**Notes:**

1. For dual-module macros, use  $t_{PD1} + t_{RD1} + t_{PDn}$ ,  $t_{CO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

**A42MX09 Timing Characteristics (Nominal 5.0V Operation) (continued)****(Worst-Case Commercial Conditions,  $V_{CC} = 4.75V$ ,  $T_J = 70^\circ C$ )**

| Parameter Description                                    | '-3' Speed                     |          | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      | Units |
|--|--------------------------------|----------|------------|------|------------|------|-------------|------|------------|------|-------|
|  | Min.                           | Max.     | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. |       |
| <b>Input Module Propagation Delays</b>                   |                                |          |            |      |            |      |             |      |            |      |       |
| $t_{INYH}$   | Pad-to-Y HIGH                  | 1.0      | 1.2        | 1.3  | 1.6        | 2.2  | ns          |      |            |      |       |
| $t_{INYL}$   | Pad-to-Y LOW                   | 0.8      | 0.9        | 1.0  | 1.2        | 1.7  | ns          |      |            |      |       |
| $t_{INGH}$   | G to Y HIGH                    | 1.3      | 1.4        | 1.6  | 1.9        | 2.7  | ns          |      |            |      |       |
| $t_{INGL}$   | G to Y LOW                     | 1.3      | 1.4        | 1.6  | 1.9        | 2.7  | ns          |      |            |      |       |
| <b>Input Module Predicted Routing Delays<sup>1</sup></b> |                                |          |            |      |            |      |             |      |            |      |       |
| $t_{IRD1}$   | FO=1 Routing Delay             | 2.0      | 2.2        | 2.5  | 3.0        | 4.2  | ns          |      |            |      |       |
| $t_{IRD2}$   | FO=2 Routing Delay             | 2.3      | 2.5        | 2.9  | 3.4        | 4.7  | ns          |      |            |      |       |
| $t_{IRD3}$   | FO=3 Routing Delay             | 2.5      | 2.8        | 3.2  | 3.7        | 5.2  | ns          |      |            |      |       |
| $t_{IRD4}$   | FO=4 Routing Delay             | 2.8      | 3.1        | 3.5  | 4.1        | 5.7  | ns          |      |            |      |       |
| $t_{IRD8}$   | FO=8 Routing Delay             | 3.7      | 4.1        | 4.7  | 5.5        | 7.7  | ns          |      |            |      |       |
| <b>Global Clock Network</b>                              |                                |          |            |      |            |      |             |      |            |      |       |
| $t_{CKH}$  | Input LOW to HIGH              | FO = 32  | 2.4        | 2.7  | 3.0        | 3.6  | 5.0         | ns   |            |      |       |
|  |                                | FO = 256 | 2.7        | 3.0  | 3.4        | 4.0  | 5.5         | ns   |            |      |       |
| $t_{CKL}$  | Input HIGH to LOW              | FO = 32  | 3.5        | 3.9  | 4.4        | 5.2  | 7.3         | ns   |            |      |       |
|  |                                | FO = 256 | 3.9        | 4.3  | 4.9        | 5.7  | 8.0         | ns   |            |      |       |
| $t_{PWH}$  | Minimum Pulse Width<br>HIGH    | FO = 32  | 1.2        | 1.4  | 1.5        | 1.8  | 2.5         | ns   |            |      |       |
|  |                                | FO = 256 | 1.3        | 1.5  | 1.7        | 2.0  | 2.7         | ns   |            |      |       |
| $t_{PWL}$  | Minimum Pulse Width<br>LOW     | FO = 32  | 1.2        | 1.4  | 1.5        | 1.8  | 2.5         | ns   |            |      |       |
|  |                                | FO = 256 | 1.3        | 1.5  | 1.7        | 2.0  | 2.7         | ns   |            |      |       |
| $t_{CKSW}$   | Maximum Skew                   | FO = 32  | 0.3        | 0.3  | 0.4        | 0.5  | 0.6         | ns   |            |      |       |
|  |                                | FO = 256 | 0.3        | 0.3  | 0.4        | 0.5  | 0.6         | ns   |            |      |       |
| $t_{SUEXT}$  | Input Latch External<br>Set-Up | FO = 32  | 0.0        | 0.0  | 0.0        | 0.0  | 0.0         | ns   |            |      |       |
|  |                                | FO = 256 | 0.0        | 0.0  | 0.0        | 0.0  | 0.0         | ns   |            |      |       |
| $t_{HEXT}$   | Input Latch External Hold      | FO = 32  | 2.3        | 2.6  | 3.0        | 3.5  | 4.9         | ns   |            |      |       |
|  |                                | FO = 256 | 2.2        | 2.4  | 3.3        | 3.9  | 5.5         | ns   |            |      |       |
| $t_P$  | Minimum Period                 | FO = 32  | 3.4        | 3.7  | 4.0        | 4.7  | 7.8         | ns   |            |      |       |
|  |                                | FO = 256 | 3.7        | 4.1  | 4.5        | 5.2  | 8.6         | ns   |            |      |       |
| $f_{MAX}$  | Maximum Frequency              | FO = 32  | 296        | 269  | 247        | 215  | 129         | MHz  |            |      |       |
|  |                                | FO = 256 | 268        | 244  | 224        | 195  | 117         | MHz  |            |      |       |

**Note:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

**A42MX09 Timing Characteristics (Nominal 5.0V Operation) (continued)**
**(Worst-Case Commercial Conditions, V<sub>CC</sub> = 4.75V, T<sub>J</sub> = 70°C)**

| Parameter Description  | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      | Units |
|--|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
|  | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. |       |
| <b>TTL Output Module Timing<sup>1</sup></b>                            |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>DLH</sub> Data-to-Pad HIGH                                      |            | 2.5  |            | 2.7  |            | 3.1  |             | 3.6  |            | 5.1  | ns    |
| t <sub>DHL</sub> Data-to-Pad LOW                                       |            | 2.9  |            | 3.2  |            | 3.6  |             | 4.3  |            | 6.0  | ns    |
| t <sub>ENZH</sub> Enable Pad Z to HIGH                                 |            | 2.6  |            | 2.9  |            | 3.3  |             | 3.9  |            | 5.5  | ns    |
| t <sub>ENZL</sub> Enable Pad Z to LOW                                  |            | 2.9  |            | 3.2  |            | 3.7  |             | 4.3  |            | 6.1  | ns    |
| t <sub>ENHZ</sub> Enable Pad HIGH to Z                                 |            | 4.9  |            | 5.4  |            | 6.2  |             | 7.3  |            | 10.2 | ns    |
| t <sub>ENLZ</sub> Enable Pad LOW to Z                                  |            | 5.3  |            | 5.9  |            | 6.7  |             | 7.9  |            | 11.1 | ns    |
| t <sub>GLH</sub> G-to-Pad HIGH   |            | 2.6  |            | 2.9  |            | 3.3  |             | 3.8  |            | 5.3  | ns    |
| t <sub>GHL</sub> G-to-Pad LOW  |            | 2.6  |            | 2.9  |            | 3.3  |             | 3.8  |            | 5.3  | ns    |
| t <sub>LSU</sub> I/O Latch Set-Up                                      | 0.5        |      | 0.5        |      | 0.6        |      | 0.7         |      | 1.0        |      | ns    |
| t <sub>LH</sub> I/O Latch Hold   | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>LCO</sub> I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading |            | 5.2  |            | 5.8  |            | 6.6  |             | 7.7  |            | 10.8 | ns    |
| t <sub>ACO</sub> Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading     |            | 7.4  |            | 8.2  |            | 9.3  |             | 10.9 |            | 15.3 | ns    |
| d <sub>TLH</sub> Capacity Loading, LOW to HIGH                         |            | 0.03 |            | 0.03 |            | 0.03 |             | 0.04 |            | 0.06 | ns/pF |
| d <sub>THL</sub> Capacity Loading, HIGH to LOW                         |            | 0.04 |            | 0.04 |            | 0.04 |             | 0.05 |            | 0.07 | ns/pF |
| <b>CMOS Output Module Timing<sup>1</sup></b>                           |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>DLH</sub> Data-to-Pad HIGH                                      |            | 2.4  |            | 2.7  |            | 3.1  |             | 3.6  |            | 5.1  | ns    |
| t <sub>DHL</sub> Data-to-Pad LOW                                       |            | 2.9  |            | 3.2  |            | 3.6  |             | 4.3  |            | 6.0  | ns    |
| t <sub>ENZH</sub> Enable Pad Z to HIGH                                 |            | 2.7  |            | 2.9  |            | 3.3  |             | 3.9  |            | 5.5  | ns    |
| t <sub>ENZL</sub> Enable Pad Z to LOW                                  |            | 2.9  |            | 3.2  |            | 3.7  |             | 4.3  |            | 6.1  | ns    |
| t <sub>ENHZ</sub> Enable Pad HIGH to Z                                 |            | 4.9  |            | 5.4  |            | 6.2  |             | 7.3  |            | 10.2 | ns    |
| t <sub>ENLZ</sub> Enable Pad LOW to Z                                  |            | 5.3  |            | 5.9  |            | 6.7  |             | 7.9  |            | 11.1 | ns    |
| t <sub>GLH</sub> G-to-Pad HIGH   |            | 4.2  |            | 4.6  |            | 5.2  |             | 6.1  |            | 8.6  | ns    |
| t <sub>GHL</sub> G-to-Pad LOW  |            | 4.2  |            | 4.6  |            | 5.2  |             | 6.1  |            | 8.6  | ns    |
| t <sub>LSU</sub> I/O Latch Set-Up                                      | 0.5        |      | 0.5        |      | 0.6        |      | 0.7         |      | 1.0        |      | ns    |
| t <sub>LH</sub> I/O Latch Hold   | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>LCO</sub> I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading |            | 5.2  |            | 5.8  |            | 6.6  |             | 7.7  |            | 10.8 | ns    |
| t <sub>ACO</sub> Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading     |            | 7.4  |            | 8.2  |            | 9.3  |             | 10.9 |            | 15.3 | ns    |
| d <sub>TLH</sub> Capacity Loading, LOW to HIGH                         |            | 0.03 |            | 0.03 |            | 0.03 |             | 0.04 |            | 0.06 | ns/pF |
| d <sub>THL</sub> Capacity Loading, HIGH to LOW                         |            | 0.04 |            | 0.04 |            | 0.04 |             | 0.05 |            | 0.07 | ns/pF |

**Note:**

1. Delays based on 35 pF loading.



## A42MX09 Timing Characteristics (Nominal 3.3V Operation)

(Worst-Case Commercial Conditions,  $V_{CC} = 3.0V$ ,  $T_J = 70^\circ C$ )

|  |  | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      |       |
|--|--|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
| Parameter  | Description                                | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. | Units |
| <b>Logic Module Propagation Delays<sup>1</sup></b>       |  |            |      |            |      |            |      |             |      |            |      |       |
| $t_{PD1}$  | Single Module                              |            | 1.6  |            | 1.8  |            | 2.1  |             | 2.5  |            | 3.5  | ns    |
| $t_{CO}$   | Sequential Clock-to-Q                      |            | 1.8  |            | 2.0  |            | 2.3  |             | 2.7  |            | 3.8  | ns    |
| $t_{GO}$   | Latch G-to-Q                               |            | 1.7  |            | 1.9  |            | 2.1  |             | 2.5  |            | 3.5  | ns    |
| $t_{RS}$   | Flip-Flop (Latch) Reset-to-Q               |            | 2.0  |            | 2.2  |            | 2.5  |             | 2.9  |            | 4.1  | ns    |
| <b>Logic Module Predicted Routing Delays<sup>2</sup></b> |  |            |      |            |      |            |      |             |      |            |      |       |
| $t_{RD1}$  | FO=1 Routing Delay                         |            | 1.0  |            | 1.1  |            | 1.2  |             | 1.4  |            | 2.0  | ns    |
| $t_{RD2}$  | FO=2 Routing Delay                         |            | 1.3  |            | 1.4  |            | 1.6  |             | 1.9  |            | 2.7  | ns    |
| $t_{RD3}$  | FO=3 Routing Delay                         |            | 1.6  |            | 1.8  |            | 2.0  |             | 2.4  |            | 3.3  | ns    |
| $t_{RD4}$  | FO=4 Routing Delay                         |            | 1.9  |            | 2.1  |            | 2.4  |             | 2.9  |            | 4.0  | ns    |
| $t_{RD8}$  | FO=8 Routing Delay                         |            | 3.2  |            | 3.6  |            | 4.1  |             | 4.8  |            | 6.7  | ns    |
| <b>Logic Module Sequential Timing<sup>3,4</sup></b>      |  |            |      |            |      |            |      |             |      |            |      |       |
| $t_{SUD}$  | Flip-Flop (Latch) Data Input Set-Up        | 0.5        |      | 0.5        |      | 0.6        |      | 0.7         |      | 0.9        |      | ns    |
| $t_{HD}$   | Flip-Flop (Latch) Data Input Hold          | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| $t_{SUENA}$  | Flip-Flop (Latch) Enable Set-Up            | 0.6        |      | 0.6        |      | 0.7        |      | 0.8         |      | 1.2        |      | ns    |
| $t_{HENA}$   | Flip-Flop (Latch) Enable Hold              | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| $t_{WCLKA}$  | Flip-Flop (Latch) Clock Active Pulse Width | 4.7        |      | 5.3        |      | 6.0        |      | 7.0         |      | 9.8        |      | ns    |
| $t_{WASYN}$  | Flip-Flop (Latch) Asynchronous Pulse Width | 6.2        |      | 6.9        |      | 7.8        |      | 9.2         |      | 12.9       |      | ns    |
| $t_A$  | Flip-Flop Clock Input Period               | 5.0        |      | 5.6        |      | 6.2        |      | 7.1         |      | 9.9        |      | ns    |
| $t_{INH}$  | Input Buffer Latch Hold                    | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| $t_{INSU}$   | Input Buffer Latch Set-Up                  | 0.3        |      | 0.3        |      | 0.3        |      | 0.4         |      | 0.6        |      | ns    |
| $t_{OUTH}$   | Output Buffer Latch Hold                   | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| $t_{OUTSU}$  | Output Buffer Latch Set-Up                 | 0.3        |      | 0.3        |      | 0.3        |      | 0.4         |      | 0.6        |      | ns    |
| $f_{MAX}$  | Flip-Flop (Latch) Clock Frequency          |            | 161  |            | 146  |            | 135  |             | 117  |            | 70   | MHz   |

**Notes:**

- For dual-module macros, use  $t_{PD1} + t_{RD1} + t_{PDn}$ ,  $t_{CO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
- Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
- Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

**A42MX09 Timing Characteristics (Nominal 3.3V Operation) (continued)**
**(Worst-Case Commercial Conditions,  $V_{CC} = 3.0V$ ,  $T_J = 70^{\circ}C$ )**

|  |                                |          | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      |       |
|--|--------------------------------|----------|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
| Parameter  | Description                    |          | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. | Units |
| <b>Input Module Propagation Delays</b>                   |                                |          |            |      |            |      |            |      |             |      |            |      |       |
| $t_{INYH}$   | Pad-to-Y HIGH                  |          |            | 1.5  |            | 1.6  |            | 1.8  |             | 2.17 |            | 3.0  | ns    |
| $t_{INYL}$   | Pad-to-Y LOW                   |          |            | 1.2  |            | 1.3  |            | 1.4  |             | 1.7  |            | 2.4  | ns    |
| $t_{INGH}$   | G to Y HIGH                    |          |            | 1.8  |            | 2.0  |            | 2.3  |             | 2.7  |            | 3.7  | ns    |
| $t_{INGL}$   | G to Y LOW                     |          |            | 1.8  |            | 2.0  |            | 2.3  |             | 2.7  |            | 3.7  | ns    |
| <b>Input Module Predicted Routing Delays<sup>1</sup></b> |                                |          |            |      |            |      |            |      |             |      |            |      |       |
| $t_{IRD1}$   | FO=1 Routing Delay             |          |            | 2.8  |            | 3.2  |            | 3.6  |             | 4.2  |            | 5.9  | ns    |
| $t_{IRD2}$   | FO=2 Routing Delay             |          |            | 3.2  |            | 3.5  |            | 4.0  |             | 4.7  |            | 6.6  | ns    |
| $t_{IRD3}$   | FO=3 Routing Delay             |          |            | 3.5  |            | 3.9  |            | 4.4  |             | 5.2  |            | 7.3  | ns    |
| $t_{IRD4}$   | FO=4 Routing Delay             |          |            | 3.9  |            | 4.3  |            | 4.9  |             | 5.7  |            | 8.0  | ns    |
| $t_{IRD8}$   | FO=8 Routing Delay             |          |            | 5.2  |            | 5.8  |            | 6.6  |             | 7.7  |            | 10.8 | ns    |
| <b>Global Clock Network</b>                              |                                |          |            |      |            |      |            |      |             |      |            |      |       |
| $t_{CKH}$  | Input LOW to HIGH              | FO = 32  |            | 4.1  |            | 4.5  |            | 5.1  |             | 6.0  |            | 8.4  | ns    |
|  |                                | FO = 256 |            | 4.5  |            | 5.0  |            | 5.6  |             | 6.7  |            | 9.3  | ns    |
| $t_{CKL}$  | Input HIGH to LOW              | FO = 32  |            | 5.0  |            | 5.5  |            | 6.2  |             | 7.3  |            | 10.2 | ns    |
|  |                                | FO = 256 |            | 5.4  |            | 6.0  |            | 6.8  |             | 8.0  |            | 11.2 | ns    |
| $t_{PWH}$  | Minimum Pulse Width<br>HIGH    | FO = 32  | 1.7        |      | 1.9        |      | 2.1        |      | 2.5         |      | 3.5        |      | ns    |
|  |                                | FO = 256 | 1.9        |      | 2.1        |      | 2.3        |      | 2.7         |      | 3.8        |      | ns    |
| $t_{PWL}$  | Minimum Pulse Width<br>LOW     | FO = 32  | 1.7        |      | 1.9        |      | 2.1        |      | 2.5         |      | 3.5        |      | ns    |
|  |                                | FO = 256 | 1.9        |      | 2.1        |      | 2.3        |      | 2.7         |      | 3.8        |      | ns    |
| $t_{CKSW}$   | Maximum Skew                   | FO = 32  |            | 0.4  |            | 0.5  |            | 0.5  |             | 0.6  |            | 0.9  | ns    |
|  |                                | FO = 256 |            | 0.4  |            | 0.5  |            | 0.5  |             | 0.6  |            | 0.9  | ns    |
| $t_{SUEXT}$  | Input Latch External<br>Set-Up | FO = 32  | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
|  |                                | FO = 256 | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| $t_{HEXT}$   | Input Latch External Hold      | FO = 32  | 3.3        |      | 3.7        |      | 4.2        |      | 4.9         |      | 6.9        |      | ns    |
|  |                                | FO = 256 | 3.7        |      | 4.1        |      | 4.6        |      | 5.5         |      | 7.6        |      | ns    |
| $t_P$  | Minimum Period                 | FO = 32  | 5.6        |      | 6.2        |      | 6.7        |      | 7.8         |      | 12.9       |      | ns    |
|  |                                | FO = 256 | 6.1        |      | 6.8        |      | 7.4        |      | 8.5         |      | 14.2       |      | ns    |
| $f_{MAX}$  | Maximum Frequency              | FO = 32  |            | 177  |            | 161  |            | 148  |             | 129  |            | 77   | MHz   |
|  |                                | FO = 256 |            | 161  |            | 146  |            | 135  |             | 117  |            | 70   | MHz   |

**Note:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

**A42MX09 Timing Characteristics (Nominal 3.3V Operation) (continued)****(Worst-Case Commercial Conditions,  $V_{CC} = 3.0V$ ,  $T_J = 70^\circ C$ )**

|  |  | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      |       |
|--|--|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
| Parameter                                    | Description  | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. | Units |
| <b>TTL Output Module Timing<sup>1</sup></b>  |  |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>DLH</sub>                             | Data-to-Pad HIGH   |            | 3.4  |            | 3.8  |            | 4.3  |             | 5.1  |            | 7.1  | ns    |
| t <sub>DHL</sub>                             | Data-to-Pad LOW  |            | 4.0  |            | 4.5  |            | 5.1  |             | 6.1  |            | 8.3  | ns    |
| t <sub>ENZH</sub>                            | Enable Pad Z to HIGH                                     |            | 3.7  |            | 4.1  |            | 4.6  |             | 5.5  |            | 7.6  | ns    |
| t <sub>ENZL</sub>                            | Enable Pad Z to LOW                                      |            | 4.1  |            | 4.5  |            | 5.1  |             | 6.1  |            | 8.5  | ns    |
| t <sub>ENHZ</sub>                            | Enable Pad HIGH to Z                                     |            | 6.9  |            | 7.6  |            | 8.6  |             | 10.2 |            | 14.2 | ns    |
| t <sub>ENLZ</sub>                            | Enable Pad LOW to Z                                      |            | 7.5  |            | 8.3  |            | 9.4  |             | 11.1 |            | 15.5 | ns    |
| t <sub>GLH</sub>                             | G-to-Pad HIGH  |            | 5.8  |            | 6.5  |            | 7.3  |             | 8.6  |            | 12.0 | ns    |
| t <sub>GHL</sub>                             | G-to-Pad LOW   |            | 5.8  |            | 6.5  |            | 7.3  |             | 8.6  |            | 12.0 | ns    |
| t <sub>LSU</sub>                             | I/O Latch Set-Up   | 0.7        |      | 0.8        |      | 0.9        |      | 1.0         |      | 1.4        |      | ns    |
| t <sub>LH</sub>                              | I/O Latch Hold   | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>LCO</sub>                             | I/O Latch Clock-to-Out (Pad-to-Pad),<br>64 Clock Loading |            | 8.7  |            | 9.7  |            | 10.9 |             | 12.9 |            | 18.0 | ns    |
| t <sub>ACO</sub>                             | Array Clock-to-Out (Pad-to-Pad),<br>64 Clock Loading     |            | 12.2 |            | 13.5 |            | 15.4 |             | 18.1 |            | 25.3 | ns    |
| d <sub>TLH</sub>                             | Capacity Loading, LOW to HIGH                            |            | 0.00 |            | 0.00 |            | 0.00 |             | 0.10 |            | 0.01 | ns/pF |
| d <sub>THL</sub>                             | Capacity Loading, HIGH to LOW                            |            | 0.09 |            | 0.10 |            | 0.10 |             | 0.10 |            | 0.10 | ns/pF |
| <b>CMOS Output Module Timing<sup>1</sup></b> |  |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>DLH</sub>                             | Data-to-Pad HIGH   |            | 3.4  |            | 3.8  |            | 5.5  |             | 6.4  |            | 9.0  | ns    |
| t <sub>DHL</sub>                             | Data-to-Pad LOW  |            | 4.1  |            | 4.5  |            | 4.2  |             | 5.0  |            | 7.0  | ns    |
| t <sub>ENZH</sub>                            | Enable Pad Z to HIGH                                     |            | 3.7  |            | 4.1  |            | 4.6  |             | 5.5  |            | 7.6  | ns    |
| t <sub>ENZL</sub>                            | Enable Pad Z to LOW                                      |            | 4.1  |            | 4.5  |            | 5.1  |             | 6.1  |            | 8.5  | ns    |
| t <sub>ENHZ</sub>                            | Enable Pad HIGH to Z                                     |            | 6.9  |            | 7.6  |            | 8.6  |             | 10.2 |            | 14.2 | ns    |
| t <sub>ENLZ</sub>                            | Enable Pad LOW to Z                                      |            | 7.5  |            | 8.3  |            | 9.4  |             | 11.1 |            | 15.5 | ns    |
| t <sub>GLH</sub>                             | G-to-Pad HIGH  |            | 5.8  |            | 6.5  |            | 7.3  |             | 8.6  |            | 12.0 | ns    |
| t <sub>GHL</sub>                             | G-to-Pad LOW   |            | 5.8  |            | 6.5  |            | 7.3  |             | 8.6  |            | 12.0 | ns    |
| t <sub>LSU</sub>                             | I/O Latch Set-Up   | 0.7        |      | 0.8        |      | 0.9        |      | 1.0         |      | 1.4        |      | ns    |
| t <sub>LH</sub>                              | I/O Latch Hold   | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>LCO</sub>                             | I/O Latch Clock-to-Out (Pad-to-Pad),<br>64 Clock Loading |            | 8.7  |            | 9.7  |            | 10.9 |             | 12.9 |            | 18.0 | ns    |
| t <sub>ACO</sub>                             | Array Clock-to-Out (Pad-to-Pad),<br>64 Clock Loading     |            | 12.2 |            | 13.5 |            | 15.4 |             | 18.1 |            | 25.3 | ns    |
| d <sub>TLH</sub>                             | Capacity Loading, LOW to HIGH                            |            | 0.04 |            | 0.04 |            | 0.05 |             | 0.06 |            | 0.08 | ns/pF |
| d <sub>THL</sub>                             | Capacity Loading, HIGH to LOW                            |            | 0.05 |            | 0.05 |            | 0.06 |             | 0.07 |            | 0.10 | ns/pF |

**Note:**

1. Delays based on 35 pF loading.

**A42MX16 Timing Characteristics (Nominal 5.0V Operation)**
**(Worst-Case Commercial Conditions, V<sub>CC</sub> = 4.75V, T<sub>J</sub> = 70°C)**

| Parameter Description   | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      | Units |
|---|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
|   | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. |       |
| <b>Logic Module Propagation Delays<sup>1</sup></b>            |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>PD1</sub> Single Module                                |            | 1.4  |            | 1.5  |            | 1.7  |             | 2.0  |            | 2.8  | ns    |
| t <sub>CO</sub> Sequential Clock-to-Q                         |            | 1.4  |            | 1.6  |            | 1.8  |             | 2.1  |            | 3.0  | ns    |
| t <sub>GO</sub> Latch G-to-Q                                  |            | 1.4  |            | 1.5  |            | 1.7  |             | 2.0  |            | 2.8  | ns    |
| t <sub>RS</sub> Flip-Flop (Latch) Reset-to-Q                  |            | 1.6  |            | 1.7  |            | 2.0  |             | 2.3  |            | 3.3  | ns    |
| <b>Logic Module Predicted Routing Delays<sup>2</sup></b>      |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>RD1</sub> FO=1 Routing Delay                           |            | 0.8  |            | 0.9  |            | 1.0  |             | 1.2  |            | 1.6  | ns    |
| t <sub>RD2</sub> FO=2 Routing Delay                           |            | 1.0  |            | 1.2  |            | 1.3  |             | 1.5  |            | 2.1  | ns    |
| t <sub>RD3</sub> FO=3 Routing Delay                           |            | 1.3  |            | 1.4  |            | 1.6  |             | 1.9  |            | 2.7  | ns    |
| t <sub>RD4</sub> FO=4 Routing Delay                           |            | 1.6  |            | 1.7  |            | 2.0  |             | 2.3  |            | 3.2  | ns    |
| t <sub>RD8</sub> FO=8 Routing Delay                           |            | 2.6  |            | 2.9  |            | 3.2  |             | 3.8  |            | 5.3  | ns    |
| <b>Logic Module Sequential Timing<sup>3,4</sup></b>           |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>SUD</sub> Flip-Flop (Latch) Data Input Set-Up          | 0.3        |      | 0.4        |      | 0.4        |      | 0.5         |      | 0.7        |      | ns    |
| t <sub>HD</sub> Flip-Flop (Latch) Data Input Hold             | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>SUENA</sub> Flip-Flop (Latch) Enable Set-Up            | 0.7        |      | 0.8        |      | 0.9        |      | 1.0         |      | 1.4        |      | ns    |
| t <sub>HENA</sub> Flip-Flop (Latch) Enable Hold               | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>WCLKA</sub> Flip-Flop (Latch) Clock Active Pulse Width | 3.4        |      | 3.8        |      | 4.3        |      | 5.0         |      | 7.1        |      | ns    |
| t <sub>WASYN</sub> Flip-Flop (Latch) Asynchronous Pulse Width | 4.5        |      | 5.0        |      | 5.6        |      | 6.6         |      | 9.2        |      | ns    |
| t <sub>A</sub> Flip-Flop Clock Input Period                   | 6.8        |      | 7.6        |      | 8.6        |      | 10.1        |      | 14.1       |      | ns    |
| t <sub>INH</sub> Input Buffer Latch Hold                      | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>INSU</sub> Input Buffer Latch Set-Up                   | 0.5        |      | 0.5        |      | 0.6        |      | 0.7         |      | 1.0        |      | ns    |
| t <sub>OUTH</sub> Output Buffer Latch Hold                    | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>OUTSU</sub> Output Buffer Latch Set-Up                 | 0.5        |      | 0.5        |      | 0.6        |      | 0.7         |      | 1.0        |      | ns    |
| f <sub>MAX</sub> Flip-Flop (Latch) Clock Frequency            |            | 215  |            | 1955 |            | 1795 |             | 1565 |            | 94   | MHz   |

**Notes:**

1. For dual-module macros, use t<sub>PD1</sub> + t<sub>RD1</sub> + t<sub>PDn</sub>, t<sub>CO</sub> + t<sub>RD1</sub> + t<sub>PDn</sub>, or t<sub>PD1</sub> + t<sub>RD1</sub> + t<sub>SUD</sub>, point and position whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

**A42MX16 Timing Characteristics (Nominal 5.0V Operation) (continued)****(Worst-Case Commercial Conditions,  $V_{CC} = 4.75V$ ,  $T_J = 70^\circ C$ )**

|  |                             |          | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      |       |
|--|-----------------------------|----------|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
| Parameter  | Description                 |          | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. | Units |
| <b>Input Module Propagation Delays</b>                   |                             |          |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>INYH</sub>  | Pad-to-Y HIGH               |          |            | 1.1  |            | 1.2  |            | 1.3  |             | 1.6  |            | 2.2  | ns    |
| t <sub>INYL</sub>  | Pad-to-Y LOW                |          |            | 0.8  |            | 0.9  |            | 1.0  |             | 1.2  |            | 1.7  | ns    |
| t <sub>INGH</sub>  | G to Y HIGH                 |          |            | 1.4  |            | 1.6  |            | 1.8  |             | 2.1  |            | 2.9  | ns    |
| t <sub>INGL</sub>  | G to Y LOW                  |          |            | 1.4  |            | 1.6  |            | 1.8  |             | 2.1  |            | 2.9  | ns    |
| <b>Input Module Predicted Routing Delays<sup>1</sup></b> |                             |          |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>IRD1</sub>  | FO=1 Routing Delay          |          |            | 1.8  |            | 2.0  |            | 2.3  |             | 2.7  |            | 4.0  | ns    |
| t <sub>IRD2</sub>  | FO=2 Routing Delay          |          |            | 2.1  |            | 2.3  |            | 2.6  |             | 3.1  |            | 4.3  | ns    |
| t <sub>IRD3</sub>  | FO=3 Routing Delay          |          |            | 2.3  |            | 2.6  |            | 3.0  |             | 3.5  |            | 4.9  | ns    |
| t <sub>IRD4</sub>  | FO=4 Routing Delay          |          |            | 2.6  |            | 3.0  |            | 3.3  |             | 3.9  |            | 5.4  | ns    |
| t <sub>IRD8</sub>  | FO=8 Routing Delay          |          |            | 3.6  |            | 4.0  |            | 4.6  |             | 5.4  |            | 7.5  | ns    |
| <b>Global Clock Network</b>                              |                             |          |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>CKH</sub>   | Input LOW to HIGH           | FO = 32  |            | 2.6  |            | 2.9  |            | 3.3  |             | 3.9  |            | 5.4  | ns    |
|  |                             | FO = 384 |            | 2.9  |            | 3.2  |            | 3.6  |             | 4.3  |            | 6.0  | ns    |
| t <sub>CKL</sub>   | Input HIGH to LOW           | FO = 32  |            | 3.8  |            | 4.2  |            | 4.8  |             | 5.6  |            | 7.8  | ns    |
|  |                             | FO = 384 |            | 4.5  |            | 5.0  |            | 5.6  |             | 6.6  |            | 9.2  | ns    |
| t <sub>PWH</sub>   | Minimum Pulse Width<br>HIGH | FO = 32  | 3.2        |      | 3.5        |      | 4.0        |      | 4.7         |      | 6.6        |      | ns    |
|  |                             | FO = 384 | 3.7        |      | 4.1        |      | 4.59       |      | 5.4         |      | 7.6        |      | ns    |
| t <sub>PWL</sub>   | Minimum Pulse Width LOW     | FO = 32  | 3.2        |      | 3.5        |      | 4.0        |      | 4.7         |      | 6.6        |      | ns    |
|  |                             | FO = 384 | 3.7        |      | 4.1        |      | 4.6        |      | 5.4         |      | 7.6        |      | ns    |
| t <sub>CKSW</sub>  | Maximum Skew                | FO = 32  |            | 0.3  |            | 0.4  |            | 0.4  |             | 0.5  |            | 0.7  | ns    |
|  |                             | FO = 384 |            | 0.3  |            | 0.4  |            | 0.4  |             | 0.5  |            | 0.7  | ns    |
| t <sub>SUEXT</sub>                                       | Input Latch External Set-Up | FO = 32  | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
|  |                             | FO = 384 | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>HEXT</sub>  | Input Latch External Hold   | FO = 32  | 2.8        |      | 3.1        |      | 5.5        |      | 4.1         |      | 5.7        |      | ns    |
|  |                             | FO = 384 | 3.2        |      | 3.5        |      | 4.0        |      | 4.7         |      | 6.6        |      | ns    |
| t <sub>P</sub>   | Minimum Period              | FO = 32  | 4.2        |      | 4.67       |      | 5.1        |      | 5.8         |      | 9.7        |      | ns    |
|  |                             | FO = 384 | 4.6        |      | 5.1        |      | 5.6        |      | 6.4         |      | 10.7       |      | ns    |
| f <sub>MAX</sub>   | Maximum Frequency           | FO = 32  |            | 237  |            | 215  |            | 198  |             | 172  |            | 103  | MHz   |
|  |                             | FO = 384 |            | 215  |            | 195  |            | 179  |             | 156  |            | 94   | MHz   |

**Note:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

**A42MX16 Timing Characteristics (Nominal 5.0V Operation) (continued)**
**(Worst-Case Commercial Conditions,  $V_{CC} = 4.75V$ ,  $T_J = 70^\circ C$ )**

| Parameter Description  | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      | Units |
|--|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
|  | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. |       |
| <b>TTL Output Module Timing<sup>1</sup></b>                            |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>DLH</sub> Data-to-Pad HIGH                                      |            | 2.5  |            | 2.8  |            | 3.2  |             | 3.7  |            | 5.2  | ns    |
| t <sub>DHL</sub> Data-to-Pad LOW                                       |            | 3.0  |            | 3.3  |            | 3.7  |             | 4.4  |            | 6.1  | ns    |
| t <sub>ENZH</sub> Enable Pad Z to HIGH                                 |            | 2.7  |            | 3.0  |            | 3.4  |             | 4.0  |            | 5.6  | ns    |
| t <sub>ENZL</sub> Enable Pad Z to LOW                                  |            | 3.0  |            | 3.3  |            | 3.8  |             | 4.4  |            | 6.2  | ns    |
| t <sub>ENHZ</sub> Enable Pad HIGH to Z                                 |            | 5.4  |            | 6.0  |            | 6.8  |             | 8.0  |            | 11.2 | ns    |
| t <sub>ENLZ</sub> Enable Pad LOW to Z                                  |            | 5.0  |            | 5.6  |            | 6.3  |             | 7.4  |            | 10.4 | ns    |
| t <sub>GLH</sub> G-to-Pad HIGH   |            | 2.9  |            | 3.2  |            | 3.6  |             | 4.3  |            | 6.0  | ns    |
| t <sub>GHL</sub> G-to-Pad LOW  |            | 2.9  |            | 3.2  |            | 3.6  |             | 4.3  |            | 6.0  | ns    |
| t <sub>LCO</sub> I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading |            | 5.7  |            | 6.3  |            | 7.1  |             | 8.4  |            | 11.9 | ns    |
| t <sub>ACO</sub> Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading     |            | 8.0  |            | 8.9  |            | 10.1 |             | 11.9 |            | 16.7 | ns    |
| d <sub>TLH</sub> Capacitive Loading, LOW to HIGH                       |            | 0.03 |            | 0.03 |            | 0.03 |             | 0.04 |            | 0.06 | ns/pF |
| d <sub>THL</sub> Capacitive Loading, HIGH to LOW                       |            | 0.04 |            | 0.04 |            | 0.04 |             | 0.05 |            | 0.07 | ns/pF |
| <b>CMOS Output Module Timing<sup>1</sup></b>                           |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>DLH</sub> Data-to-Pad HIGH                                      |            | 3.2  |            | 3.6  |            | 4.0  |             | 4.7  |            | 6.6  | ns    |
| t <sub>DHL</sub> Data-to-Pad LOW                                       |            | 2.5  |            | 2.7  |            | 3.1  |             | 3.6  |            | 5.1  | ns    |
| t <sub>ENZH</sub> Enable Pad Z to HIGH                                 |            | 2.7  |            | 3.0  |            | 3.4  |             | 4.0  |            | 5.6  | ns    |
| t <sub>ENZL</sub> Enable Pad Z to LOW                                  |            | 3.0  |            | 3.3  |            | 3.8  |             | 4.4  |            | 6.2  | ns    |
| t <sub>ENHZ</sub> Enable Pad HIGH to Z                                 |            | 5.4  |            | 6.0  |            | 6.8  |             | 8.0  |            | 11.2 | ns    |
| t <sub>ENLZ</sub> Enable Pad LOW to Z                                  |            | 5.0  |            | 5.6  |            | 6.3  |             | 7.4  |            | 10.4 | ns    |
| t <sub>GLH</sub> G-to-Pad HIGH   |            | 5.1  |            | 5.6  |            | 6.4  |             | 7.5  |            | 10.5 | ns    |
| t <sub>GHL</sub> G-to-Pad LOW  |            | 5.1  |            | 5.6  |            | 6.4  |             | 7.5  |            | 10.5 | ns    |
| t <sub>LCO</sub> I/O Latch Clock-to-Out (Pad-to-Pad), 64 Clock Loading |            | 5.7  |            | 6.3  |            | 7.1  |             | 8.4  |            | 11.9 | ns    |
| t <sub>ACO</sub> Array Clock-to-Out (Pad-to-Pad), 64 Clock Loading     |            | 8.0  |            | 8.9  |            | 10.1 |             | 11.9 |            | 16.7 | ns    |
| d <sub>TLH</sub> Capacitive Loading, LOW to HIGH                       |            | 0.03 |            | 0.03 |            | 0.03 |             | 0.04 |            | 0.06 | ns/pF |
| d <sub>THL</sub> Capacitive Loading, HIGH to LOW                       |            | 0.04 |            | 0.04 |            | 0.04 |             | 0.05 |            | 0.07 | ns/pF |

**Note:**

1. Delays based on 35 pF loading.

**A42MX16 Timing Characteristics (Nominal 3.3V Operation)****(Worst-Case Commercial Conditions,  $V_{CC} = 3.0V$ ,  $T_J = 70^\circ C$ )**

|  |  | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      |       |
|--|--|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
| Parameter  | Description                                | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. | Units |
| <b>Logic Module Propagation Delays<sup>1</sup></b>       |  |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>PD1</sub>   | Single Module                              |            | 1.9  |            | 2.1  |            | 2.4  |             | 2.8  |            | 4.0  | ns    |
| t <sub>CO</sub>  | Sequential Clock-to-Q                      |            | 2.0  |            | 2.2  |            | 2.5  |             | 3.0  |            | 4.2  | ns    |
| t <sub>GO</sub>  | Latch G-to-Q                               |            | 1.9  |            | 2.1  |            | 2.4  |             | 2.8  |            | 4.0  | ns    |
| t <sub>RS</sub>  | Flip-Flop (Latch) Reset-to-Q               |            | 2.2  |            | 2.4  |            | 2.8  |             | 3.3  |            | 4.6  | ns    |
| <b>Logic Module Predicted Routing Delays<sup>2</sup></b> |  |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>RD1</sub>   | FO=1 Routing Delay                         |            | 1.1  |            | 1.2  |            | 1.4  |             | 1.6  |            | 2.3  | ns    |
| t <sub>RD2</sub>   | FO=2 Routing Delay                         |            | 1.5  |            | 1.6  |            | 1.8  |             | 2.1  |            | 3.0  | ns    |
| t <sub>RD3</sub>   | FO=3 Routing Delay                         |            | 1.8  |            | 2.0  |            | 2.3  |             | 2.7  |            | 3.8  | ns    |
| t <sub>RD4</sub>   | FO=4 Routing Delay                         |            | 2.2  |            | 2.4  |            | 2.7  |             | 3.2  |            | 4.5  | ns    |
| t <sub>RD8</sub>   | FO=8 Routing Delay                         |            | 3.6  |            | 4.0  |            | 4.5  |             | 5.3  |            | 7.5  | ns    |
| <b>Logic Module Sequential Timing<sup>3, 4</sup></b>     |  |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>SUD</sub>   | Flip-Flop (Latch) Data Input Set-Up        | 0.5        |      | 0.5        |      | 0.6        |      | 0.7         |      | 0.9        |      | ns    |
| t <sub>HD</sub>  | Flip-Flop (Latch) Data Input Hold          | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>SUENA</sub>                                       | Flip-Flop (Latch) Enable Set-Up            | 1.0        |      | 1.1        |      | 1.2        |      | 1.4         |      | 2.0        |      | ns    |
| t <sub>HENA</sub>  | Flip-Flop (Latch) Enable Hold              | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>WCLKA</sub>                                       | Flip-Flop (Latch) Clock Active Pulse Width | 4.8        |      | 5.3        |      | 6.0        |      | 7.1         |      | 9.9        |      | ns    |
| t <sub>WASYN</sub>                                       | Flip-Flop (Latch) Asynchronous Pulse Width | 6.2        |      | 6.9        |      | 7.9        |      | 9.2         |      | 12.9       |      | ns    |
| t <sub>A</sub>   | Flip-Flop Clock Input Period               | 9.5        |      | 10.6       |      | 12.0       |      | 14.1        |      | 19.8       |      | ns    |
| t <sub>INH</sub>   | Input Buffer Latch Hold                    | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>INSU</sub>  | Input Buffer Latch Set-Up                  | 0.7        |      | 0.8        |      | 0.9        |      | 1.01        |      | 1.4        |      | ns    |
| t <sub>OUTH</sub>  | Output Buffer Latch Hold                   | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>OUTSU</sub>                                       | Output Buffer Latch Set-Up                 | 0.7        |      | 0.8        |      | 0.89       |      | 1.01        |      | 1.4        |      | ns    |
| f <sub>MAX</sub>   | Flip-Flop (Latch) Clock Frequency          |            | 129  |            | 117  |            | 108  |             | 94   |            | 56   | MHz   |

**Notes:**

1. For dual-module macros use  $t_{PD1} + t_{RD1} + t_{PDn}$ ,  $t_{CO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

**A42MX16 Timing Characteristics (Nominal 3.3V Operation) (continued)**
**(Worst-Case Commercial Conditions,  $V_{CC} = 3.0V$ ,  $T_J = 70^{\circ}C$ )**

|  |                             |          | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      |       |
|--|-----------------------------|----------|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
| Parameter  | Description                 |          | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. | Units |
| <b>Input Module Propagation Delays</b>                   |                             |          |            |      |            |      |            |      |             |      |            |      |       |
| $t_{INYH}$   | Pad-to-Y HIGH               |          |            | 1.5  |            | 1.6  |            | 1.9  |             | 2.2  |            | 3.1  | ns    |
| $t_{INYL}$   | Pad-to-Y LOW                |          |            | 1.1  |            | 1.3  |            | 1.4  |             | 1.7  |            | 2.4  | ns    |
| $t_{INGH}$   | G to Y HIGH                 |          |            | 2.0  |            | 2.2  |            | 2.5  |             | 2.9  |            | 4.1  | ns    |
| $t_{INGL}$   | G to Y LOW                  |          |            | 2.0  |            | 2.2  |            | 2.5  |             | 2.9  |            | 4.1  | ns    |
| <b>Input Module Predicted Routing Delays<sup>1</sup></b> |                             |          |            |      |            |      |            |      |             |      |            |      |       |
| $t_{IRD1}$   | FO=1 Routing Delay          |          |            | 2.6  |            | 2.9  |            | 3.2  |             | 3.8  |            | 5.3  | ns    |
| $t_{IRD2}$   | FO=2 Routing Delay          |          |            | 2.9  |            | 3.2  |            | 3.7  |             | 4.3  |            | 6.1  | ns    |
| $t_{IRD3}$   | FO=3 Routing Delay          |          |            | 3.3  |            | 3.6  |            | 4.1  |             | 4.9  |            | 6.8  | ns    |
| $t_{IRD4}$   | FO=4 Routing Delay          |          |            | 3.6  |            | 4.0  |            | 4.6  |             | 5.4  |            | 7.6  | ns    |
| $t_{IRD8}$   | FO=8 Routing Delay          |          |            | 5.1  |            | 5.6  |            | 6.4  |             | 7.5  |            | 10.5 | ns    |
| <b>Global Clock Network</b>                              |                             |          |            |      |            |      |            |      |             |      |            |      |       |
| $t_{CKH}$  | Input LOW to HIGH           | FO = 32  |            | 4.4  |            | 4.8  |            | 5.5  |             | 6.5  |            | 9.0  | ns    |
|  |                             | FO = 384 |            | 4.8  |            | 5.3  |            | 6.0  |             | 7.1  |            | 9.9  | ns    |
| $t_{CKL}$  | Input HIGH to LOW           | FO = 32  |            | 5.3  |            | 5.9  |            | 6.7  |             | 7.8  |            | 11.0 | ns    |
|  |                             | FO = 384 |            | 6.2  |            | 6.9  |            | 7.9  |             | 9.2  |            | 12.9 | ns    |
| $t_{PWH}$  | Minimum Pulse Width HIGH    | FO = 32  | 5.7        |      | 6.3        |      | 7.1        |      | 8.4         |      | 11.8       |      | ns    |
|  |                             | FO = 384 | 6.6        |      | 7.4        |      | 8.3        |      | 9.8         |      | 13.7       |      | ns    |
| $t_{PWL}$  | Minimum Pulse Width LOW     | FO = 32  | 5.3        |      | 5.9        |      | 6.7        |      | 7.8         |      | 11.0       |      | ns    |
|  |                             | FO = 384 | 6.2        |      | 6.9        |      | 7.9        |      | 9.2         |      | 12.9       |      | ns    |
| $t_{CKSW}$   | Maximum Skew                | FO = 32  |            | 0.5  |            | 0.5  |            | 0.6  |             | 0.7  |            | 1.0  | ns    |
|  |                             | FO = 384 |            | 2.2  |            | 2.4  |            | 2.7  |             | 3.2  |            | 4.5  | ns    |
| $t_{SUEXT}$  | Input Latch External Set-Up | FO = 32  | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
|  |                             | FO = 384 | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| $t_{HEXT}$   | Input Latch External Hold   | FO = 32  | 3.9        |      | 4.3        |      | 4.9        |      | 5.7         |      | 8.0        |      | ns    |
|  |                             | FO = 384 | 4.5        |      | 4.9        |      | 5.6        |      | 6.6         |      | 9.2        |      | ns    |
| $t_P$  | Minimum Period              | FO = 32  | 7.0        |      | 7.8        |      | 8.4        |      | 9.7         |      | 16.2       |      | ns    |
|  |                             | FO = 384 | 7.7        |      | 8.6        |      | 9.3        |      | 10.7        |      | 17.8       |      | ns    |
| $f_{MAX}$  | Maximum Frequency           | FO = 32  |            | 142  |            | 129  |            | 119  |             | 103  |            | 62   | MHz   |
|  |                             | FO = 384 |            | 129  |            | 117  |            | 108  |             | 94   |            | 56   | MHz   |

**Note:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.



**A42MX16 Timing Characteristics (Nominal 3.3V Operation) (continued)****(Worst-Case Commercial Conditions,  $V_{CC} = 3.0V$ ,  $T_J = 70^\circ C$ )**

| Parameter Description                        | '-3' Speed   |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      | Units |
|--|--|------|------------|------|------------|------|-------------|------|------------|------|-------|
|  | Min.   | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. |       |
| <b>TTL Output Module Timing<sup>1</sup></b>  |  |      |            |      |            |      |             |      |            |      |       |
| t <sub>DLH</sub>                             | Data-to-Pad HIGH   | 3.5  | 3.9        | 4.4  | 5.2        | 7.3  | ns          |      |            |      |       |
| t <sub>DHL</sub>                             | Data-to-Pad LOW  | 4.1  | 4.6        | 5.2  | 6.1        | 8.6  | ns          |      |            |      |       |
| t <sub>ENZH</sub>                            | Enable Pad Z to HIGH                                     | 3.8  | 4.2        | 4.8  | 5.6        | 7.8  | ns          |      |            |      |       |
| t <sub>ENZL</sub>                            | Enable Pad Z to LOW                                      | 4.2  | 4.6        | 5.3  | 6.2        | 8.7  | ns          |      |            |      |       |
| t <sub>ENHZ</sub>                            | Enable Pad HIGH to Z                                     | 7.6  | 8.4        | 9.5  | 11.2       | 15.7 | ns          |      |            |      |       |
| t <sub>ENLZ</sub>                            | Enable Pad LOW to Z                                      | 7.0  | 7.8        | 8.8  | 10.4       | 14.5 | ns          |      |            |      |       |
| t <sub>GLH</sub>                             | G-to-Pad HIGH  | 4.8  | 5.3        | 6.0  | 7.2        | 10.0 | ns          |      |            |      |       |
| t <sub>GHL</sub>                             | G-to-Pad LOW   | 4.8  | 5.3        | 6.0  | 7.2        | 10.0 | ns          |      |            |      |       |
| t <sub>LCO</sub>                             | I/O Latch Clock-to-Out (Pad-to-Pad),<br>64 Clock Loading | 8.0  | 8.9        | 10.1 | 11.9       | 16.7 | ns          |      |            |      |       |
| t <sub>ACO</sub>                             | Array Clock-to-Out (Pad-to-Pad),<br>64 Clock Loading     | 11.3 | 12.5       | 14.2 | 16.7       | 23.3 | ns          |      |            |      |       |
| d <sub>TLH</sub>                             | Capacitive Loading, LOW to HIGH                          | 0.04 | 0.04       | 0.05 | 0.06       | 0.08 | ns/pF       |      |            |      |       |
| d <sub>THL</sub>                             | Capacitive Loading, HIGH to LOW                          | 0.05 | 0.05       | 0.06 | 0.07       | 0.10 | ns/pF       |      |            |      |       |
| <b>CMOS Output Module Timing<sup>1</sup></b> |  |      |            |      |            |      |             |      |            |      |       |
| t <sub>DLH</sub>                             | Data-to-Pad HIGH   | 4.5  | 5.0        | 5.6  | 6.6        | 9.3  | ns          |      |            |      |       |
| t <sub>DHL</sub>                             | Data-to-Pad LOW  | 3.4  | 3.8        | 4.3  | 5.1        | 7.1  | ns          |      |            |      |       |
| t <sub>ENZH</sub>                            | Enable Pad Z to HIGH                                     | 3.8  | 4.2        | 4.8  | 5.6        | 7.8  | ns          |      |            |      |       |
| t <sub>ENZL</sub>                            | Enable Pad Z to LOW                                      | 4.2  | 4.6        | 5.3  | 6.2        | 8.7  | ns          |      |            |      |       |
| t <sub>ENHZ</sub>                            | Enable Pad HIGH to Z                                     | 7.6  | 8.4        | 9.5  | 11.2       | 15.7 | ns          |      |            |      |       |
| t <sub>ENLZ</sub>                            | Enable Pad LOW to Z                                      | 7.0  | 7.8        | 8.8  | 10.4       | 14.5 | ns          |      |            |      |       |
| t <sub>GLH</sub>                             | G-to-Pad HIGH  | 7.1  | 7.9        | 8.9  | 10.5       | 14.7 | ns          |      |            |      |       |
| t <sub>GHL</sub>                             | G-to-Pad LOW   | 7.1  | 7.9        | 8.9  | 10.5       | 14.7 | ns          |      |            |      |       |
| t <sub>LCO</sub>                             | I/O Latch Clock-to-Out (Pad-to-Pad),<br>64 Clock Loading | 8.0  | 8.9        | 10.1 | 11.9       | 16.7 | ns          |      |            |      |       |
| t <sub>ACO</sub>                             | Array Clock-to-Out (Pad-to-Pad),<br>64 Clock Loading     | 11.3 | 12.5       | 14.2 | 16.7       | 23.3 | ns          |      |            |      |       |
| d <sub>TLH</sub>                             | Capacitive Loading, LOW to HIGH                          | 0.04 | 0.04       | 0.05 | 0.06       | 0.08 | ns/pF       |      |            |      |       |
| d <sub>THL</sub>                             | Capacitive Loading, HIGH to LOW                          | 0.05 | 0.05       | 0.06 | 0.07       | 0.10 | ns/pF       |      |            |      |       |

**Note:**

1. Delays based on 35 pF loading.

**A42MX24 Timing Characteristics (Nominal 5.0V Operation)**
**(Worst-Case Commercial Conditions,  $V_{CC} = 4.75V$ ,  $T_J = 70^\circ C$ )**

| Parameter Description                                    | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      | Units |
|--|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
|  | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. |       |
| <b>Logic Module Combinatorial Functions<sup>1</sup></b>  |            |      |            |      |            |      |             |      |            |      |       |
| $t_{PD}$ Internal Array Module Delay                     |            | 1.2  |            | 1.3  |            | 1.5  |             | 1.8  |            | 2.5  | ns    |
| $t_{PDD}$ Internal Decode Module Delay                   |            | 1.4  |            | 1.6  |            | 1.8  |             | 2.1  |            | 3.0  | ns    |
| <b>Logic Module Predicted Routing Delays<sup>2</sup></b> |            |      |            |      |            |      |             |      |            |      |       |
| $t_{RD1}$ FO=1 Routing Delay                             |            | 0.8  |            | 0.9  |            | 1.0  |             | 1.2  |            | 1.7  | ns    |
| $t_{RD2}$ FO=2 Routing Delay                             |            | 1.0  |            | 1.2  |            | 1.3  |             | 1.5  |            | 2.1  | ns    |
| $t_{RD3}$ FO=3 Routing Delay                             |            | 1.3  |            | 1.4  |            | 1.6  |             | 1.9  |            | 2.6  | ns    |
| $t_{RD4}$ FO=4 Routing Delay                             |            | 1.5  |            | 1.7  |            | 1.9  |             | 2.2  |            | 3.1  | ns    |
| $t_{RD5}$ FO=8 Routing Delay                             |            | 2.4  |            | 2.7  |            | 3.0  |             | 3.6  |            | 5.0  | ns    |
| <b>Logic Module Sequential Timing<sup>3, 4</sup></b>     |            |      |            |      |            |      |             |      |            |      |       |
| $t_{CO}$ Flip-Flop Clock-to-Output                       |            | 1.3  |            | 1.4  |            | 1.6  |             | 1.9  |            | 2.7  | ns    |
| $t_{GO}$ Latch Gate-to-Output                            |            | 1.2  |            | 1.3  |            | 1.5  |             | 1.8  |            | 2.5  | ns    |
| $t_{SU}$ Flip-Flop (Latch) Set-Up Time                   | 0.3        |      | 0.4        |      | 0.4        |      | 0.5         |      | 0.7        |      | ns    |
| $t_H$ Flip-Flop (Latch) Hold Time                        | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| $t_{RO}$ Flip-Flop (Latch) Reset-to-Output               |            | 1.4  |            | 1.6  |            | 1.8  |             | 2.1  |            | 2.9  | ns    |
| $t_{SUENA}$ Flip-Flop (Latch) Enable Set-Up              | 0.4        |      | 0.5        |      | 0.5        |      | 0.6         |      | 0.8        |      | ns    |
| $t_{HENA}$ Flip-Flop (Latch) Enable Hold                 | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| $t_{WCLKA}$ Flip-Flop (Latch) Clock Active Pulse Width   | 3.3        |      | 3.7        |      | 4.2        |      | 4.9         |      | 6.9        |      | ns    |
| $t_{WASYN}$ Flip-Flop (Latch) Asynchronous Pulse Width   | 4.4        |      | 4.8        |      | 5.3        |      | 6.5         |      | 9.0        |      | ns    |

**Notes:**

- For dual-module macros, use  $t_{PD1} + t_{RD1} + t_{PDn}$ ,  $t_{CO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
- Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
- Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

**A42MX24 Timing Characteristics (Nominal 5.0V Operation) (continued)****(Worst-Case Commercial Conditions,  $V_{CC} = 4.75V$ ,  $T_J = 70^\circ C$ )**

|  |                                |        | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      |       |
|--|--------------------------------|--------|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
| Parameter  | Description                    |        | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. | Units |
| <b>Input Module Propagation Delays</b>                   |                                |        |            |      |            |      |            |      |             |      |            |      |       |
| $t_{INPY}$   | Input Data Pad-to-Y            |        |            | 1.0  |            | 1.1  |            | 1.3  |             | 1.5  |            | 2.1  | ns    |
| $t_{INGO}$   | Input Latch Gate-to-Output     |        |            | 1.3  |            | 1.4  |            | 1.6  |             | 1.9  |            | 2.6  | ns    |
| $t_{INH}$  | Input Latch Hold               |        | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| $t_{INSU}$   | Input Latch Set-Up             |        | 0.5        |      | 0.5        |      | 0.6        |      | 0.7         |      | 1.0        |      | ns    |
| $t_{ILA}$  | Latch Active Pulse Width       |        | 4.7        |      | 5.2        |      | 5.9        |      | 6.9         |      | 9.7        |      | ns    |
| <b>Input Module Predicted Routing Delays<sup>1</sup></b> |                                |        |            |      |            |      |            |      |             |      |            |      |       |
| $t_{IRD1}$   | FO=1 Routing Delay             |        |            | 1.8  |            | 2.0  |            | 2.3  |             | 2.7  |            | 3.8  | ns    |
| $t_{IRD2}$   | FO=2 Routing Delay             |        |            | 2.1  |            | 2.3  |            | 2.6  |             | 3.1  |            | 4.3  | ns    |
| $t_{IRD3}$   | FO=3 Routing Delay             |        |            | 2.3  |            | 2.5  |            | 2.9  |             | 3.4  |            | 4.8  | ns    |
| $t_{IRD4}$   | FO=4 Routing Delay             |        |            | 2.5  |            | 2.8  |            | 3.2  |             | 3.7  |            | 5.2  | ns    |
| $t_{IRD8}$   | FO=8 Routing Delay             |        |            | 3.4  |            | 3.8  |            | 4.3  |             | 5.1  |            | 7.1  | ns    |
| <b>Global Clock Network</b>                              |                                |        |            |      |            |      |            |      |             |      |            |      |       |
| $t_{CKH}$  | Input LOW to HIGH              | FO=32  |            | 2.6  |            | 2.9  |            | 3.3  |             | 3.9  |            | 5.4  | ns    |
|  |                                | FO=486 |            | 2.9  |            | 3.2  |            | 3.6  |             | 4.3  |            | 5.9  | ns    |
| $t_{CKL}$  | Input HIGH to LOW              | FO=32  |            | 3.7  |            | 4.1  |            | 4.6  |             | 5.4  |            | 7.6  | ns    |
|  |                                | FO=486 |            | 4.3  |            | 4.7  |            | 5.4  |             | 6.3  |            | 8.8  | ns    |
| $t_{PWH}$  | Minimum Pulse Width HIGH       | FO=32  | 2.2        |      | 2.4        |      | 2.7        |      | 3.2         |      | 4.5        |      | ns    |
|  |                                | FO=486 | 2.4        |      | 2.6        |      | 3.0        |      | 3.5         |      | 4.9        |      | ns    |
| $t_{PWL}$  | Minimum Pulse Width LOW        | FO=32  | 2.2        |      | 2.4        |      | 2.7        |      | 3.2         |      | 4.5        |      | ns    |
|  |                                | FO=486 | 2.4        |      | 2.6        |      | 3.0        |      | 3.5         |      | 4.9        |      | ns    |
| $t_{CKSW}$   | Maximum Skew                   | FO=32  |            | 0.5  |            | 0.6  |            | 0.7  |             | 0.8  |            | 1.1  | ns    |
|  |                                | FO=486 |            | 0.5  |            | 0.6  |            | 0.7  |             | 0.8  |            | 1.1  | ns    |
| $t_{SUEXT}$  | Input Latch External Set-Up    | FO=32  | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
|  |                                | FO=486 | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| $t_{HEXT}$   | Input Latch External Hold      | FO=32  | 2.8        |      | 3.1        |      | 3.5        |      | 4.1         |      | 5.7        |      | ns    |
|  |                                | FO=486 | 3.3        |      | 3.7        |      | 4.2        |      | 4.9         |      | 6.9        |      | ns    |
| $t_P$  | Minimum Period ( $1/f_{MAX}$ ) | FO=32  | 4.7        |      | 5.2        |      | 5.7        |      | 6.5         |      | 10.9       |      | ns    |
|  |                                | FO=486 | 5.1        |      | 5.7        |      | 6.2        |      | 7.1         |      | 11.9       |      | ns    |
| $f_{MAX}$  | Maximum Datapath Frequency     | FO=32  |            | 210  |            | 191  |            | 176  |             | 153  |            | 92   | MHz   |
|  |                                | FO=486 |            | 193  |            | 175  |            | 161  |             | 140  |            | 84   | MHz   |

**Note:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

**A42MX24 Timing Characteristics (Nominal 5.0V Operation) (continued)**
**(Worst-Case Commercial Conditions,  $V_{CC} = 4.75V$ ,  $T_J = 70^{\circ}C$ )**

| Parameter Description  | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      | Units |
|--|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
|  | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. |       |
| <b>TTL Output Module Timing<sup>1</sup></b>                  |            |      |            |      |            |      |             |      |            |      |       |
| $t_{DLH}$ Data-to-Pad HIGH                                   |            | 2.4  |            | 2.7  |            | 3.1  |             | 3.6  |            | 5.1  | ns    |
| $t_{DHL}$ Data-to-Pad LOW                                    |            | 2.8  |            | 3.2  |            | 3.6  |             | 4.2  |            | 5.9  | ns    |
| $t_{ENZH}$ Enable Pad Z to HIGH                              |            | 2.5  |            | 2.8  |            | 3.2  |             | 3.8  |            | 5.3  | ns    |
| $t_{ENZL}$ Enable Pad Z to LOW                               |            | 2.8  |            | 3.1  |            | 3.5  |             | 4.2  |            | 5.9  | ns    |
| $t_{ENHZ}$ Enable Pad HIGH to Z                              |            | 5.2  |            | 5.7  |            | 6.5  |             | 7.6  |            | 10.7 | ns    |
| $t_{ENLZ}$ Enable Pad LOW to Z                               |            | 4.8  |            | 5.3  |            | 6.0  |             | 7.1  |            | 9.9  | ns    |
| $t_{GLH}$ G-to-Pad HIGH                                      |            | 2.9  |            | 3.2  |            | 3.6  |             | 4.3  |            | 6.0  | ns    |
| $t_{GHL}$ G-to-Pad LOW                                       |            | 2.9  |            | 3.2  |            | 3.6  |             | 4.3  |            | 6.0  | ns    |
| $t_{LSU}$ I/O Latch Output Set-Up                            | 0.5        |      | 0.5        |      | 0.6        |      | 0.7         |      | 1.0        |      | ns    |
| $t_{LH}$ I/O Latch Output Hold                               | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| $t_{LCO}$ I/O Latch Clock-to-Out (Pad-to-Pad)<br>32 I/O      |            | 5.6  |            | 6.1  |            | 6.9  |             | 8.1  |            | 11.4 | ns    |
| $t_{ACO}$ Array Latch Clock-to-Out<br>(Pad-to-Pad)<br>32 I/O |            | 10.6 |            | 11.8 |            | 13.4 |             | 15.7 |            | 22.0 | ns    |
| $d_{TLH}$ Capacitive Loading, LOW to HIGH                    |            | 0.04 |            | 0.04 |            | 0.04 |             | 0.05 |            | 0.07 | ns/pF |
| $d_{THL}$ Capacitive Loading, HIGH to LOW                    |            | 0.03 |            | 0.03 |            | 0.03 |             | 0.04 |            | 0.06 | ns/pF |
| <b>CMOS Output Module Timing<sup>1</sup></b>                 |            |      |            |      |            |      |             |      |            |      |       |
| $t_{DLH}$ Data-to-Pad HIGH                                   |            | 3.1  |            | 3.5  |            | 3.9  |             | 4.6  |            | 6.4  | ns    |
| $t_{DHL}$ Data-to-Pad LOW                                    |            | 2.4  |            | 2.6  |            | 3.0  |             | 3.5  |            | 4.9  | ns    |
| $t_{ENZH}$ Enable Pad Z to HIGH                              |            | 2.5  |            | 2.8  |            | 3.2  |             | 3.8  |            | 5.3  | ns    |
| $t_{ENZL}$ Enable Pad Z to LOW                               |            | 2.8  |            | 3.1  |            | 3.5  |             | 4.2  |            | 5.8  | ns    |
| $t_{ENHZ}$ Enable Pad HIGH to Z                              |            | 5.2  |            | 5.7  |            | 6.5  |             | 7.6  |            | 10.7 | ns    |
| $t_{ENLZ}$ Enable Pad LOW to Z                               |            | 4.8  |            | 5.3  |            | 6.0  |             | 7.1  |            | 9.9  | ns    |
| $t_{GLH}$ G-to-Pad HIGH                                      |            | 4.9  |            | 5.4  |            | 6.2  |             | 7.2  |            | 10.1 | ns    |
| $t_{GHL}$ G-to-Pad LOW                                       |            | 4.9  |            | 5.4  |            | 6.2  |             | 7.2  |            | 10.1 | ns    |
| $t_{LSU}$ I/O Latch Set-Up                                   | 0.5        |      | 0.5        |      | 0.6        |      | 0.7         |      | 1.0        |      | ns    |
| $t_{LH}$ I/O Latch Hold                                      | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| $t_{LCO}$ I/O Latch Clock-to-Out (Pad-to-Pad)<br>32 I/O      |            | 5.5  |            | 6.1  |            | 6.9  |             | 8.1  |            | 11.3 | ns    |
| $t_{ACO}$ Array Latch Clock-to-Out<br>(Pad-to-Pad)<br>32 I/O |            | 10.6 |            | 11.8 |            | 13.4 |             | 15.7 |            | 22.0 | ns    |
| $d_{TLH}$ Capacitive Loading, LOW to HIGH                    |            | 0.04 |            | 0.04 |            | 0.04 |             | 0.05 |            | 0.07 | ns/pF |
| $d_{THL}$ Capacitive Loading, HIGH to LOW                    |            | 0.03 |            | 0.03 |            | 0.03 |             | 0.04 |            | 0.06 | ns/pF |

**Note:**

1. Delays based on 35 pF loading.

**A42MX24 Timing Characteristics (Nominal 3.3V Operation)****(Worst-Case Commercial Conditions,  $V_{CC} = 3.0V$ ,  $T_J = 70^{\circ}C$ )**

|  |  | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      |       |
|--|--|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
| Parameter  | Description                                | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. | Units |
| <b>Logic Module Combinatorial Functions<sup>1</sup></b>  |  |            |      |            |      |            |      |             |      |            |      |       |
| $t_{PD}$   | Internal Array Module Delay                |            | 2.0  |            | 1.8  |            | 2.1  |             | 2.5  |            | 3.4  | ns    |
| $t_{PDD}$  | Internal Decode Module Delay               |            | 1.1  |            | 2.2  |            | 2.5  |             | 3.0  |            | 4.2  | ns    |
| <b>Logic Module Predicted Routing Delays<sup>2</sup></b> |  |            |      |            |      |            |      |             |      |            |      |       |
| $t_{RD1}$  | FO=1 Routing Delay                         |            | 1.7  |            | 1.3  |            | 1.4  |             | 1.7  |            | 2.3  | ns    |
| $t_{RD2}$  | FO=2 Routing Delay                         |            | 2.0  |            | 1.6  |            | 1.8  |             | 2.1  |            | 3.0  | ns    |
| $t_{RD3}$  | FO=3 Routing Delay                         |            | 1.1  |            | 2.0  |            | 2.2  |             | 2.6  |            | 3.7  | ns    |
| $t_{RD4}$  | FO=4 Routing Delay                         |            | 1.5  |            | 2.3  |            | 2.6  |             | 3.1  |            | 4.3  | ns    |
| $t_{RD5}$  | FO=8 Routing Delay                         |            | 1.8  |            | 3.7  |            | 4.2  |             | 5.0  |            | 7.0  | ns    |
| <b>Logic Module Sequential Timing<sup>3, 4</sup></b>     |  |            |      |            |      |            |      |             |      |            |      |       |
| $t_{CO}$   | Flip-Flop Clock-to-Output                  |            | 2.1  |            | 2.0  |            | 2.3  |             | 2.7  |            | 3.7  | ns    |
| $t_{GO}$   | Latch Gate-to-Output                       |            | 3.4  |            | 1.9  |            | 2.1  |             | 2.5  |            | 3.4  | ns    |
| $t_{SU}$   | Flip-Flop (Latch) Set-Up Time              | 0.4        |      | 0.5        |      | 0.6        |      | 0.7         |      | 0.9        |      | ns    |
| $t_H$  | Flip-Flop (Latch) Hold Time                | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| $t_{RO}$   | Flip-Flop (Latch) Reset-to-Output          |            | 2.0  |            | 2.2  |            | 2.5  |             | 2.9  |            | 4.1  | ns    |
| $t_{SUENA}$  | Flip-Flop (Latch) Enable Set-Up            | 0.6        |      | 0.6        |      | 0.7        |      | 0.8         |      | 1.2        |      | ns    |
| $t_{HENA}$   | Flip-Flop (Latch) Enable Hold              | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| $t_{WCLKA}$  | Flip-Flop (Latch) Clock Active Pulse Width | 4.6        |      | 5.2        |      | 5.8        |      | 6.9         |      | 9.6        |      | ns    |
| $t_{WASYN}$  | Flip-Flop (Latch) Asynchronous Pulse Width | 6.1        |      | 6.8        |      | 7.7        |      | 9.0         |      | 12.6       |      | ns    |

**Notes:**

1. For dual-module macros, use  $t_{PD1} + t_{RD1} + t_{PDn}$ ,  $t_{CO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
3. Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
4. Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

**A42MX24 Timing Characteristics (Nominal 3.3V Operation) (continued)**
**(Worst-Case Commercial Conditions, V<sub>CC</sub> = 3.0V, T<sub>J</sub> = 70°C)**

|  |                                      |        | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      |       |
|--|--------------------------------------|--------|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
| Parameter  | Description                          |        | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. | Units |
| <b>Input Module Propagation Delays</b>                   |                                      |        |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>INPY</sub>  | Input Data Pad-to-Y                  |        |            | 1.4  |            | 1.6  |            | 1.8  |             | 2.2  |            | 3.0  | ns    |
| t <sub>INGO</sub>  | Input Latch Gate-to-Output           |        |            | 1.8  |            | 1.9  |            | 2.2  |             | 2.6  |            | 3.6  | ns    |
| t <sub>INH</sub>   | Input Latch Hold                     |        | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>INSU</sub>  | Input Latch Set-Up                   |        | 0.7        |      | 0.7        |      | 0.8        |      | 1.0         |      | 1.4        |      | ns    |
| t <sub>ILA</sub>   | Latch Active Pulse Width             |        | 6.5        |      | 7.3        |      | 8.2        |      | 9.7         |      | 13.5       |      | ns    |
| <b>Input Module Predicted Routing Delays<sup>1</sup></b> |                                      |        |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>IRD1</sub>  | FO=1 Routing Delay                   |        |            | 2.6  |            | 2.9  |            | 3.2  |             | 3.8  |            | 5.3  | ns    |
| t <sub>IRD2</sub>  | FO=2 Routing Delay                   |        |            | 2.9  |            | 3.2  |            | 3.6  |             | 4.3  |            | 6.0  | ns    |
| t <sub>IRD3</sub>  | FO=3 Routing Delay                   |        |            | 3.2  |            | 3.6  |            | 4.0  |             | 4.8  |            | 6.6  | ns    |
| t <sub>IRD4</sub>  | FO=4 Routing Delay                   |        |            | 3.5  |            | 3.9  |            | 4.4  |             | 5.2  |            | 7.3  | ns    |
| t <sub>IRD8</sub>  | FO=8 Routing Delay                   |        |            | 4.8  |            | 5.3  |            | 6.1  |             | 7.1  |            | 10.0 | ns    |
| <b>Global Clock Network</b>                              |                                      |        |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>CKH</sub>   | Input LOW to HIGH                    | FO=32  |            | 4.4  |            | 4.8  |            | 5.5  |             | 6.5  |            | 9.1  | ns    |
|  |                                      | FO=486 |            | 4.8  |            | 5.3  |            | 6.0  |             | 7.1  |            | 10.0 | ns    |
| t <sub>CKL</sub>   | Input HIGH to LOW                    | FO=32  |            | 5.1  |            | 5.7  |            | 6.4  |             | 7.6  |            | 10.6 | ns    |
|  |                                      | FO=486 |            | 6.0  |            | 6.6  |            | 7.5  |             | 8.8  |            | 12.4 | ns    |
| t <sub>PWH</sub>   | Minimum Pulse Width HIGH             | FO=32  | 3.0        |      | 3.3        |      | 3.8        |      | 4.5         |      | 6.3        |      | ns    |
|  |                                      | FO=486 | 3.3        |      | 3.7        |      | 4.2        |      | 4.9         |      | 6.9        |      | ns    |
| t <sub>PWL</sub>   | Minimum Pulse Width LOW              | FO=32  | 3.0        |      | 3.4        |      | 3.8        |      | 4.5         |      | 6.3        |      | ns    |
|  |                                      | FO=486 | 3.3        |      | 3.7        |      | 4.2        |      | 4.9         |      | 6.9        |      | ns    |
| t <sub>CKSW</sub>  | Maximum Skew                         | FO=32  |            | 0.8  |            | 0.8  |            | 1.0  |             | 1.1  |            | 1.6  | ns    |
|  |                                      | FO=486 |            | 0.8  |            | 0.8  |            | 1.0  |             | 1.1  |            | 1.6  | ns    |
| t <sub>SUEXT</sub>                                       | Input Latch External Set-Up          | FO=32  | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
|  |                                      | FO=486 | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>HEXT</sub>  | Input Latch External Hold            | FO=32  | 3.9        |      | 4.3        |      | 4.9        |      | 5.7         |      | 8.1        |      | ns    |
|  |                                      | FO=486 | 4.6        |      | 5.2        |      | 5.8        |      | 6.9         |      | 9.6        |      | ns    |
| t <sub>P</sub>   | Minimum Period (1/f <sub>MAX</sub> ) | FO=32  | 7.8        |      | 8.7        |      | 9.47       |      | 10.8        |      | 18.2       |      | ns    |
|  |                                      | FO=486 | 8.6        |      | 9.5        |      | 10.4       |      | 11.9        |      | 19.9       |      | ns    |
| f <sub>MAX</sub>   | Maximum Datapath Frequency           | FO=32  |            | 126  |            | 115  |            | 106  |             | 92   |            | 55   | MHz   |
|  |                                      | FO=486 |            | 116  |            | 105  |            | 97   |             | 84   |            | 50   | MHz   |

**Note:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

**A42MX24 Timing Characteristics (Nominal 3.3V Operation) (continued)****(Worst-Case Commercial Conditions,  $V_{CC} = 3.0V$ ,  $T_J = 70^\circ C$ )**

|  |  | '-3 Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      |       |
|--|--|-----------|------|------------|------|------------|------|-------------|------|------------|------|-------|
| Parameter                                    | Description  | Min.      | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. | Units |
| <b>TTL Output Module Timing<sup>1</sup></b>  |  |           |      |            |      |            |      |             |      |            |      |       |
| t <sub>DLH</sub>                             | Data-to-Pad HIGH                                   |           | 3.4  |            | 3.8  |            | 4.3  |             | 5.0  |            | 7.1  | ns    |
| t <sub>DHL</sub>                             | Data-to-Pad LOW                                    |           | 4.0  |            | 4.4  |            | 5.0  |             | 5.9  |            | 8.3  | ns    |
| t <sub>ENZH</sub>                            | Enable Pad Z to HIGH                               |           | 3.6  |            | 4.0  |            | 4.5  |             | 5.3  |            | 7.4  | ns    |
| t <sub>ENZL</sub>                            | Enable Pad Z to LOW                                |           | 3.9  |            | 4.4  |            | 5.0  |             | 5.8  |            | 8.2  | ns    |
| t <sub>ENHZ</sub>                            | Enable Pad HIGH to Z                               |           | 7.2  |            | 8.0  |            | 9.07 |             | 10.7 |            | 14.9 | ns    |
| t <sub>ENLZ</sub>                            | Enable Pad LOW to Z                                |           | 6.7  |            | 7.5  |            | 8.5  |             | 9.9  |            | 13.9 | ns    |
| t <sub>GLH</sub>                             | G-to-Pad HIGH                                      |           | 4.8  |            | 5.3  |            | 6.0  |             | 7.2  |            | 10.0 | ns    |
| t <sub>GHL</sub>                             | G-to-Pad LOW                                       |           | 4.8  |            | 5.3  |            | 6.0  |             | 7.2  |            | 10.0 | ns    |
| t <sub>LSU</sub>                             | I/O Latch Output Set-Up                            | 0.7       |      | 0.7        |      | 0.8        |      | 1.0         |      | 1.4        |      | ns    |
| t <sub>LH</sub>                              | I/O Latch Output Hold                              | 0.0       |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>LCO</sub>                             | I/O Latch Clock-to-Out (Pad-to-Pad)<br>32 I/O      |           | 7.67 |            | 8.5  |            | 9.6  |             | 11.3 |            | 15.9 | ns    |
| t <sub>ACO</sub>                             | Array Latch Clock-to-Out<br>(Pad-to-Pad)<br>32 I/O |           | 14.8 |            | 16.5 |            | 18.7 |             | 22.0 |            | 30.8 | ns    |
| d <sub>TLH</sub>                             | Capacitive Loading, LOW to HIGH                    |           | 0.05 |            | 0.05 |            | 0.06 |             | 0.07 |            | 0.10 | ns/pF |
| d <sub>THL</sub>                             | Capacitive Loading, HIGH to LOW                    |           | 0.04 |            | 0.04 |            | 0.05 |             | 0.06 |            | 0.08 | ns/pF |
| <b>CMOS Output Module Timing<sup>1</sup></b> |  |           |      |            |      |            |      |             |      |            |      |       |
| t <sub>DLH</sub>                             | Data-to-Pad HIGH                                   |           | 4.8  |            | 5.3  |            | 5.5  |             | 6.4  |            | 9.0  | ns    |
| t <sub>DHL</sub>                             | Data-to-Pad LOW                                    |           | 3.5  |            | 3.9  |            | 4.1  |             | 4.9  |            | 6.8  | ns    |
| t <sub>ENZH</sub>                            | Enable Pad Z to HIGH                               |           | 3.6  |            | 4.0  |            | 4.5  |             | 5.3  |            | 7.4  | ns    |
| t <sub>ENZL</sub>                            | Enable Pad Z to LOW                                |           | 3.4  |            | 4.0  |            | 5.0  |             | 5.8  |            | 8.2  | ns    |
| t <sub>ENHZ</sub>                            | Enable Pad HIGH to Z                               |           | 7.2  |            | 8.0  |            | 9.01 |             | 10.7 |            | 14.9 | ns    |
| t <sub>ENLZ</sub>                            | Enable Pad LOW to Z                                |           | 6.7  |            | 7.5  |            | 8.5  |             | 9.9  |            | 13.9 | ns    |
| t <sub>GLH</sub>                             | G-to-Pad HIGH                                      |           | 6.8  |            | 7.6  |            | 8.6  |             | 10.1 |            | 14.2 | ns    |
| t <sub>GHL</sub>                             | G-to-Pad LOW                                       |           | 6.8  |            | 7.6  |            | 8.6  |             | 10.1 |            | 14.2 | ns    |
| t <sub>LSU</sub>                             | I/O Latch Set-Up                                   | 0.7       |      | 0.7        |      | 0.8        |      | 1.0         |      | 1.4        |      | ns    |
| t <sub>LH</sub>                              | I/O Latch Hold                                     | 0.0       |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>LCO</sub>                             | I/O Latch Clock-to-Out (Pad-to-Pad)<br>32 I/O      |           | 7.7  |            | 8.5  |            | 9.6  |             | 11.3 |            | 15.9 | ns    |
| t <sub>ACO</sub>                             | Array Latch Clock-to-Out<br>(Pad-to-Pad)<br>32 I/O |           | 14.8 |            | 16.5 |            | 18.7 |             | 22.0 |            | 30.8 | ns    |
| d <sub>TLH</sub>                             | Capacitive Loading, LOW to HIGH                    |           | 0.05 |            | 0.05 |            | 0.06 |             | 0.07 |            | 0.10 | ns/pF |
| d <sub>THL</sub>                             | Capacitive Loading, HIGH to LOW                    |           | 0.04 |            | 0.04 |            | 0.05 |             | 0.06 |            | 0.08 | ns/pF |

**Note:**

1. Delays based on 35 pF loading.

**A42MX36 Timing Characteristics (Nominal 5.0V Operation)**
**(Worst-Case Commercial Conditions, V<sub>CC</sub> = 4.75V, T<sub>J</sub> = 70°C)**

| Parameter Description   | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      | Units |
|---|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
|   | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. |       |
| <b>Logic Module Combinatorial Functions<sup>1</sup></b>       |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>PD</sub> Internal Array Module Delay                   |            | 1.3  |            | 1.5  |            | 1.7  |             | 2.0  |            | 2.7  | ns    |
| t <sub>PDD</sub> Internal Decode Module Delay                 |            | 1.6  |            | 1.8  |            | 2.0  |             | 2.4  |            | 3.3  | ns    |
| <b>Logic Module Predicted Routing Delays<sup>2</sup></b>      |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>RD1</sub> FO=1 Routing Delay                           |            | 0.9  |            | 1.0  |            | 1.2  |             | 1.4  |            | 2.0  | ns    |
| t <sub>RD2</sub> FO=2 Routing Delay                           |            | 1.3  |            | 1.4  |            | 1.6  |             | 1.9  |            | 2.7  | ns    |
| t <sub>RD3</sub> FO=3 Routing Delay                           |            | 1.6  |            | 1.8  |            | 2.0  |             | 2.4  |            | 3.4  | ns    |
| t <sub>RD4</sub> FO=4 Routing Delay                           |            | 2.0  |            | 2.2  |            | 2.5  |             | 2.9  |            | 4.1  | ns    |
| t <sub>RD5</sub> FO=8 Routing Delay                           |            | 3.3  |            | 3.7  |            | 4.2  |             | 4.9  |            | 6.9  | ns    |
| t <sub>RDD</sub> Decode-to-Output Routing Delay               |            | 0.3  |            | 0.4  |            | 0.4  |             | 0.5  |            | 0.7  | ns    |
| <b>Logic Module Sequential Timing<sup>3, 4</sup></b>          |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>CO</sub> Flip-Flop Clock-to-Output                     |            | 1.3  |            | 1.4  |            | 1.6  |             | 1.9  |            | 2.7  | ns    |
| t <sub>GO</sub> Latch Gate-to-Output                          |            | 1.3  |            | 1.4  |            | 1.6  |             | 1.9  |            | 2.7  | ns    |
| t <sub>SU</sub> Flip-Flop (Latch) Set-Up Time                 | 0.3        |      | 0.34       |      | 0.4        |      | 0.5         |      | 0.7        |      | ns    |
| t <sub>H</sub> Flip-Flop (Latch) Hold Time                    | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>RO</sub> Flip-Flop (Latch) Reset-to-Output             |            | 1.6  |            | 1.7  |            | 2.0  |             | 2.3  |            | 3.2  | ns    |
| t <sub>SUENA</sub> Flip-Flop (Latch) Enable Set-Up            | 0.7        |      | 0.8        |      | 0.9        |      | 1.0         |      | 1.4        |      | ns    |
| t <sub>HENA</sub> Flip-Flop (Latch) Enable Hold               | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>WCLKA</sub> Flip-Flop (Latch) Clock Active Pulse Width | 3.3        |      | 3.7        |      | 4.2        |      | 4.9         |      | 6.9        |      | ns    |
| t <sub>WASYN</sub> Flip-Flop (Latch) Asynchronous Pulse Width | 4.4        |      | 4.8        |      | 5.5        |      | 6.4         |      | 9.0        |      | ns    |

**Notes:**

- For dual-module macros, use  $t_{PD1} + t_{RD1} + t_{PDn}$ ,  $t_{CO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
- Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
- Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.



**A42MX36 Timing Characteristics (Nominal 5.0V Operation) (continued)****(Worst-Case Commercial Conditions,  $V_{CC} = 4.75V$ ,  $T_J = 70^\circ C$ )**

| Logic Module Timing                 |                                     | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      |       |
|-------------------------------------|-------------------------------------|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
| Parameter                           | Description                         | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. | Units |
| <b>Synchronous SRAM Operations</b>  |                                     |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>RC</sub>                     | Read Cycle Time                     | 6.8        |      | 7.5        |      | 8.5        |      | 10.0        |      | 14.0       |      | ns    |
| t <sub>WC</sub>                     | Write Cycle Time                    | 6.8        |      | 7.5        |      | 8.5        |      | 10.0        |      | 14.0       |      | ns    |
| t <sub>RCKHL</sub>                  | Clock HIGH/LOW Time                 | 3.4        |      | 3.8        |      | 4.3        |      | 5.0         |      | 7.0        |      | ns    |
| t <sub>RCO</sub>                    | Data Valid After Clock HIGH/LOW     |            | 3.4  |            | 3.78 |            | 4.3  |             | 5.0  |            | 7.0  | ns    |
| t <sub>ADSU</sub>                   | Address/Data Set-Up Time            | 1.6        |      | 1.8        |      | 2.0        |      | 2.4         |      | 3.4        |      | ns    |
| t <sub>ADH</sub>                    | Address/Data Hold Time              | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>RENSU</sub>                  | Read Enable Set-Up                  | 0.6        |      | 0.7        |      | 0.8        |      | 0.9         |      | 1.3        |      | ns    |
| t <sub>RENH</sub>                   | Read Enable Hold                    | 3.4        |      | 3.8        |      | 4.3        |      | 5.0         |      | 7.0        |      | ns    |
| t <sub>WENSU</sub>                  | Write Enable Set-Up                 | 2.7        |      | 3.0        |      | 3.4        |      | 4.0         |      | 5.6        |      | ns    |
| t <sub>WENH</sub>                   | Write Enable Hold                   | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>BENS</sub>                   | Block Enable Set-Up                 | 2.8        |      | 3.1        |      | 3.5        |      | 4.1         |      | 5.7        |      | ns    |
| t <sub>BENH</sub>                   | Block Enable Hold                   | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| <b>Asynchronous SRAM Operations</b> |                                     |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>RPD</sub>                    | Asynchronous Access Time            |            | 8.1  |            | 9.0  |            | 10.2 |             | 12.0 |            | 16.8 | ns    |
| t <sub>RDADV</sub>                  | Read Address Valid                  | 8.8        |      | 9.8        |      | 11.1       |      | 13.0        |      | 18.2       |      | ns    |
| t <sub>ADSU</sub>                   | Address/Data Set-Up Time            | 1.6        |      | 1.8        |      | 2.0        |      | 2.4         |      | 3.4        |      | ns    |
| t <sub>ADH</sub>                    | Address/Data Hold Time              | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>RENSUA</sub>                 | Read Enable Set-Up to Address Valid | 0.6        |      | 0.7        |      | 0.8        |      | 0.9         |      | 1.3        |      | ns    |
| t <sub>RENHA</sub>                  | Read Enable Hold                    | 3.4        |      | 3.8        |      | 4.3        |      | 5.0         |      | 7.0        |      | ns    |
| t <sub>WENSU</sub>                  | Write Enable Set-Up                 | 2.7        |      | 3.0        |      | 3.4        |      | 4.0         |      | 5.6        |      | ns    |
| t <sub>WENH</sub>                   | Write Enable Hold                   | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>DOH</sub>                    | Data Out Hold Time                  |            | 1.2  |            | 1.34 |            | 1.5  |             | 1.8  |            | 2.5  | ns    |

**A42MX36 Timing Characteristics (Nominal 5.0V Operation) (continued)**
**(Worst-Case Commercial Conditions,  $V_{CC} = 4.75V$ ,  $T_J = 70^\circ C$ )**

|  |                                |        | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      |       |
|--|--------------------------------|--------|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
| Parameter  | Description                    |        | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. | Units |
| <b>Input Module Propagation Delays</b>                   |                                |        |            |      |            |      |            |      |             |      |            |      |       |
| $t_{INPY}$   | Input Data Pad-to-Y            |        |            | 1.0  |            | 1.1  |            | 1.3  |             | 1.5  |            | 2.1  | ns    |
| $t_{INGO}$   | Input Latch Gate-to-Output     |        |            | 1.4  |            | 1.6  |            | 1.8  |             | 2.1  |            | 2.9  | ns    |
| $t_{INH}$  | Input Latch Hold               |        | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| $t_{INSU}$   | Input Latch Set-Up             |        | 0.5        |      | 0.5        |      | 0.6        |      | 0.7         |      | 1.0        |      | ns    |
| $t_{ILA}$  | Latch Active Pulse Width       |        | 4.7        |      | 5.2        |      | 5.9        |      | 6.9         |      | 9.7        |      | ns    |
| <b>Input Module Predicted Routing Delays<sup>1</sup></b> |                                |        |            |      |            |      |            |      |             |      |            |      |       |
| $t_{IRD1}$   | FO=1 Routing Delay             |        |            | 2.0  |            | 2.2  |            | 2.5  |             | 2.9  |            | 4.1  | ns    |
| $t_{IRD2}$   | FO=2 Routing Delay             |        |            | 2.3  |            | 2.6  |            | 2.9  |             | 3.4  |            | 4.8  | ns    |
| $t_{IRD3}$   | FO=3 Routing Delay             |        |            | 2.6  |            | 2.9  |            | 3.3  |             | 3.9  |            | 5.5  | ns    |
| $t_{IRD4}$   | FO=4 Routing Delay             |        |            | 3.0  |            | 3.3  |            | 3.8  |             | 4.4  |            | 6.2  | ns    |
| $t_{IRD8}$   | FO=8 Routing Delay             |        |            | 4.3  |            | 4.8  |            | 5.5  |             | 6.4  |            | 9.0  | ns    |
| <b>Global Clock Network</b>                              |                                |        |            |      |            |      |            |      |             |      |            |      |       |
| $t_{CKH}$  | Input LOW to HIGH              | FO=32  |            | 2.7  |            | 3.0  |            | 3.4  |             | 4.0  |            | 5.6  | ns    |
|  |                                | FO=635 |            | 3.0  |            | 3.3  |            | 3.8  |             | 4.4  |            | 6.2  | ns    |
| $t_{CKL}$  | Input HIGH to LOW              | FO=32  |            | 3.8  |            | 4.2  |            | 4.8  |             | 5.6  |            | 7.8  | ns    |
|  |                                | FO=635 |            | 4.9  |            | 5.4  |            | 6.1  |             | 7.2  |            | 10.1 | ns    |
| $t_{PWH}$  | Minimum Pulse Width HIGH       | FO=32  | 1.8        |      | 2.0        |      | 2.2        |      | 2.6         |      | 3.6        |      | ns    |
|  |                                | FO=635 | 2.0        |      | 2.2        |      | 2.5        |      | 2.9         |      | 4.1        |      | ns    |
| $t_{PWL}$  | Minimum Pulse Width LOW        | FO=32  | 1.8        |      | 2.0        |      | 2.2        |      | 2.6         |      | 3.6        |      | ns    |
|  |                                | FO=635 | 2.0        |      | 2.2        |      | 2.5        |      | 2.9         |      | 4.1        |      | ns    |
| $t_{CKSW}$   | Maximum Skew                   | FO=32  |            | 0.8  |            | 0.8  |            | 0.9  |             | 1.0  |            | 1.4  | ns    |
|  |                                | FO=635 |            | 0.8  |            | 0.8  |            | 0.9  |             | 1.0  |            | 1.4  | ns    |
| $t_{SUEXT}$  | Input Latch External Set-Up    | FO=32  | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
|  |                                | FO=635 | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| $t_{HEXT}$   | Input Latch External Hold      | FO=32  | 2.8        |      | 3.2        |      | 3.6        |      | 4.2         |      | 5.9        |      | ns    |
|  |                                | FO=635 | 3.3        |      | 3.7        |      | 4.2        |      | 4.9         |      | 6.9        |      | ns    |
| $t_P$  | Minimum Period ( $1/f_{MAX}$ ) | FO=32  | 5.5        |      | 6.1        |      | 6.6        |      | 7.6         |      | 12.7       |      | ns    |
|  |                                | FO=635 | 6.0        |      | 6.6        |      | 7.2        |      | 8.3         |      | 13.8       |      | ns    |
| $f_{HMAX}$   | Maximum Datapath Frequency     | FO=32  |            | 180  |            | 164  |            | 151  |             | 131  |            | 79   | MHz   |
|  |                                | FO=635 |            | 166  |            | 151  |            | 139  |             | 121  |            | 73   | MHz   |

**Note:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

**A42MX36 Timing Characteristics (Nominal 5.0V Operation) (continued)****(Worst-Case Commercial Conditions,  $V_{CC} = 4.75V$ ,  $T_J = 70^\circ C$ )**

|  |  | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      |       |
|--|--|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
| Parameter                                    | Description  | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. | Units |
| <b>TTL Output Module Timing<sup>1</sup></b>  |  |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>DLH</sub>                             | Data-to-Pad HIGH                                   |            | 2.6  |            | 2.8  |            | 3.2  |             | 3.8  |            | 5.3  | ns    |
| t <sub>DHL</sub>                             | Data-to-Pad LOW                                    |            | 3.0  |            | 3.3  |            | 3.7  |             | 4.4  |            | 6.2  | ns    |
| t <sub>ENZH</sub>                            | Enable Pad Z to HIGH                               |            | 2.7  |            | 3.0  |            | 3.3  |             | 3.9  |            | 5.5  | ns    |
| t <sub>ENZL</sub>                            | Enable Pad Z to LOW                                |            | 3.0  |            | 3.3  |            | 3.7  |             | 4.3  |            | 6.1  | ns    |
| t <sub>ENHZ</sub>                            | Enable Pad HIGH to Z                               |            | 5.3  |            | 5.8  |            | 6.6  |             | 7.8  |            | 10.9 | ns    |
| t <sub>ENLZ</sub>                            | Enable Pad LOW to Z                                |            | 4.9  |            | 5.5  |            | 6.2  |             | 7.3  |            | 10.2 | ns    |
| t <sub>GLH</sub>                             | G-to-Pad HIGH                                      |            | 2.9  |            | 3.3  |            | 3.7  |             | 4.4  |            | 6.1  | ns    |
| t <sub>GHL</sub>                             | G-to-Pad LOW                                       |            | 2.9  |            | 3.3  |            | 3.7  |             | 4.4  |            | 6.1  | ns    |
| t <sub>LSU</sub>                             | I/O Latch Output Set-Up                            | 0.5        |      | 0.5        |      | 0.6        |      | 0.7         |      | 1.0        |      | ns    |
| t <sub>LH</sub>                              | I/O Latch Output Hold                              | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>LCO</sub>                             | I/O Latch Clock-to-Out (Pad-to-Pad)<br>32 I/O      |            | 5.7  |            | 6.3  |            | 7.1  |             | 8.4  |            | 11.8 | ns    |
| t <sub>ACO</sub>                             | Array Latch Clock-to-Out<br>(Pad-to-Pad)<br>32 I/O |            | 7.8  |            | 8.6  |            | 9.8  |             | 11.5 |            | 16.1 | ns    |
| d <sub>TLH</sub>                             | Capacitive Loading, LOW to HIGH                    | 0.07       |      | 0.08       |      | 0.09       |      | 0.10        |      | 0.14       |      | ns/pF |
| d <sub>THL</sub>                             | Capacitive Loading, HIGH to LOW                    | 0.07       |      | 0.08       |      | 0.09       |      | 0.10        |      | 0.14       |      | ns/pF |
| <b>CMOS Output Module Timing<sup>1</sup></b> |  |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>DLH</sub>                             | Data-to-Pad HIGH                                   |            | 3.5  |            | 3.9  |            | 4.5  |             | 5.2  |            | 7.3  | ns    |
| t <sub>DHL</sub>                             | Data-to-Pad LOW                                    |            | 2.5  |            | 2.7  |            | 3.1  |             | 3.6  |            | 5.1  | ns    |
| t <sub>ENZH</sub>                            | Enable Pad Z to HIGH                               |            | 2.7  |            | 3.0  |            | 3.3  |             | 3.9  |            | 5.5  | ns    |
| t <sub>ENZL</sub>                            | Enable Pad Z to LOW                                |            | 2.9  |            | 3.3  |            | 3.7  |             | 4.3  |            | 6.1  | ns    |
| t <sub>ENHZ</sub>                            | Enable Pad HIGH to Z                               |            | 5.3  |            | 5.8  |            | 6.6  |             | 7.8  |            | 10.9 | ns    |
| t <sub>ENLZ</sub>                            | Enable Pad LOW to Z                                |            | 4.9  |            | 5.5  |            | 6.2  |             | 7.3  |            | 10.2 | ns    |
| t <sub>GLH</sub>                             | G-to-Pad HIGH                                      |            | 5.0  |            | 5.6  |            | 6.3  |             | 7.5  |            | 10.4 | ns    |
| t <sub>GHL</sub>                             | G-to-Pad LOW                                       |            | 5.0  |            | 5.6  |            | 6.3  |             | 7.5  |            | 10.4 | ns    |
| t <sub>LSU</sub>                             | I/O Latch Set-Up                                   | 0.5        |      | 0.5        |      | 0.6        |      | 0.7         |      | 1.0        |      | ns    |
| t <sub>LH</sub>                              | I/O Latch Hold                                     | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>LCO</sub>                             | I/O Latch Clock-to-Out (Pad-to-Pad)<br>32 I/O      |            | 5.7  |            | 6.3  |            | 7.1  |             | 8.4  |            | 11.8 | ns    |
| t <sub>ACO</sub>                             | Array Latch Clock-to-Out<br>(Pad-to-Pad)<br>32 I/O |            | 7.78 |            | 8.6  |            | 9.8  |             | 11.5 |            | 16.1 | ns    |
| d <sub>TLH</sub>                             | Capacitive Loading, LOW to HIGH                    | 0.07       |      | 0.08       |      | 0.09       |      | 0.10        |      | 0.14       |      | ns/pF |
| d <sub>THL</sub>                             | Capacitive Loading, HIGH to LOW                    | 0.07       |      | 0.08       |      | 0.09       |      | 0.10        |      | 0.14       |      | ns/pF |

**Note:**

1. Delays based on 35 pF loading.

**A42MX36 Timing Characteristics (Nominal 3.3V Operation)**
**(Worst-Case Commercial Conditions,  $V_{CC} = 3.0V$ ,  $T_J = 70^{\circ}C$ )**

| Parameter Description                                    | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      | Units |
|--|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
|  | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. |       |
| <b>Logic Module Combinatorial Functions<sup>1</sup></b>  |            |      |            |      |            |      |             |      |            |      |       |
| $t_{PD}$ Internal Array Module Delay                     |            | 1.9  |            | 2.1  |            | 2.3  |             | 2.7  |            | 3.8  | ns    |
| $t_{PDD}$ Internal Decode Module Delay                   |            | 2.2  |            | 2.5  |            | 2.8  |             | 3.3  |            | 4.7  | ns    |
| <b>Logic Module Predicted Routing Delays<sup>2</sup></b> |            |      |            |      |            |      |             |      |            |      |       |
| $t_{RD1}$ FO=1 Routing Delay                             |            | 1.3  |            | 1.5  |            | 1.7  |             | 2.0  |            | 2.7  | ns    |
| $t_{RD2}$ FO=2 Routing Delay                             |            | 1.8  |            | 2.0  |            | 2.3  |             | 2.7  |            | 3.7  | ns    |
| $t_{RD3}$ FO=3 Routing Delay                             |            | 2.3  |            | 2.5  |            | 2.8  |             | 3.4  |            | 4.7  | ns    |
| $t_{RD4}$ FO=4 Routing Delay                             |            | 2.8  |            | 3.1  |            | 3.5  |             | 4.1  |            | 5.7  | ns    |
| $t_{RD5}$ FO=8 Routing Delay                             |            | 4.6  |            | 5.2  |            | 5.8  |             | 6.9  |            | 9.6  | ns    |
| $t_{RDD}$ Decode-to-Output Routing Delay                 |            | 0.5  |            | 0.5  |            | 0.6  |             | 0.7  |            | 1.0  | ns    |
| <b>Logic Module Sequential Timing<sup>3, 4</sup></b>     |            |      |            |      |            |      |             |      |            |      |       |
| $t_{CO}$ Flip-Flop Clock-to-Output                       |            | 1.8  |            | 2.0  |            | 2.3  |             | 2.7  |            | 3.7  | ns    |
| $t_{GO}$ Latch Gate-to-Output                            |            | 1.8  |            | 2.0  |            | 2.3  |             | 2.7  |            | 3.7  | ns    |
| $t_{SU}$ Flip-Flop (Latch) Set-Up Time                   | 0.4        |      | 0.5        |      | 0.6        |      | 0.7         |      | 0.9        |      | ns    |
| $t_H$ Flip-Flop (Latch) Hold Time                        | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| $t_{RO}$ Flip-Flop (Latch) Reset-to-Output               |            | 2.2  |            | 2.4  |            | 2.7  |             | 3.2  |            | 4.5  | ns    |
| $t_{SUENA}$ Flip-Flop (Latch) Enable Set-Up              | 1.0        |      | 1.1        |      | 1.2        |      | 1.4         |      | 2.0        |      | ns    |
| $t_{HENA}$ Flip-Flop (Latch) Enable Hold                 | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| $t_{WCLKA}$ Flip-Flop (Latch) Clock Active Pulse Width   | 4.6        |      | 5.2        |      | 5.8        |      | 6.9         |      | 9.6        |      | ns    |
| $t_{WASYN}$ Flip-Flop (Latch) Asynchronous Pulse Width   | 6.1        |      | 6.8        |      | 7.7        |      | 9.0         |      | 12.6       |      | ns    |

**Notes:**

- For dual-module macros, use  $t_{PD1} + t_{RD1} + t_{PDn}$ ,  $t_{CO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
- Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
- Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

**A42MX36 Timing Characteristics (Nominal 3.3V Operation) (continued)****(Worst-Case Commercial Conditions,  $V_{CC} = 3.0V$ ,  $T_J = 70^\circ C$ )**

| Logic Module Timing                 |                                     | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      |       |
|-------------------------------------|-------------------------------------|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
| Parameter                           | Description                         | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. | Units |
| <b>Synchronous SRAM Operations</b>  |                                     |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>RC</sub>                     | Read Cycle Time                     | 9.5        |      | 10.5       |      | 11.9       |      | 14.0        |      | 19.6       |      | ns    |
| t <sub>WC</sub>                     | Write Cycle Time                    | 9.5        |      | 10.5       |      | 11.9       |      | 14.0        |      | 19.6       |      | ns    |
| t <sub>RCKHL</sub>                  | Clock HIGH/LOW Time                 | 4.8        |      | 5.3        |      | 6.0        |      | 7.0         |      | 9.8        |      | ns    |
| t <sub>RCO</sub>                    | Data Valid After Clock HIGH/LOW     |            | 4.8  |            | 5.3  |            | 6.0  |             | 7.0  |            | 9.8  | ns    |
| t <sub>ADSU</sub>                   | Address/Data Set-Up Time            | 2.3        |      | 2.5        |      | 2.8        |      | 3.4         |      | 4.8        |      | ns    |
| t <sub>ADH</sub>                    | Address/Data Hold Time              | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>RENSU</sub>                  | Read Enable Set-Up                  | 0.9        |      | 1.0        |      | 1.1        |      | 1.3         |      | 1.8        |      | ns    |
| t <sub>RENH</sub>                   | Read Enable Hold                    | 4.8        |      | 5.3        |      | 6.0        |      | 7.0         |      | 9.8        |      | ns    |
| t <sub>WENSU</sub>                  | Write Enable Set-Up                 | 3.8        |      | 4.2        |      | 4.8        |      | 5.6         |      | 7.8        |      | ns    |
| t <sub>WENH</sub>                   | Write Enable Hold                   | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>BENS</sub>                   | Block Enable Set-Up                 | 3.9        |      | 4.3        |      | 4.9        |      | 5.7         |      | 8.0        |      | ns    |
| t <sub>BENH</sub>                   | Block Enable Hold                   | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| <b>Asynchronous SRAM Operations</b> |                                     |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>RPD</sub>                    | Asynchronous Access Time            |            | 11.3 |            | 12.6 |            | 14.3 |             | 16.8 |            | 23.5 | ns    |
| t <sub>RDADV</sub>                  | Read Address Valid                  | 12.3       |      | 13.7       |      | 15.5       |      | 18.2        |      | 25.5       |      | ns    |
| t <sub>ADSU</sub>                   | Address/Data Set-Up Time            | 2.3        |      | 2.5        |      | 2.8        |      | 3.4         |      | 4.8        |      | ns    |
| t <sub>ADH</sub>                    | Address/Data Hold Time              | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>RENSUA</sub>                 | Read Enable Set-Up to Address Valid | 0.9        |      | 1.0        |      | 1.1        |      | 1.3         |      | 1.8        |      | ns    |
| t <sub>RENHA</sub>                  | Read Enable Hold                    | 4.8        |      | 5.3        |      | 6.0        |      | 7.0         |      | 9.8        |      | ns    |
| t <sub>WENSU</sub>                  | Write Enable Set-Up                 | 3.8        |      | 4.2        |      | 4.8        |      | 5.6         |      | 7.8        |      | ns    |
| t <sub>WENH</sub>                   | Write Enable Hold                   | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>DOH</sub>                    | Data Out Hold Time                  |            | 1.8  |            | 2.0  |            | 2.1  |             | 2.5  |            | 3.5  | ns    |

**A42MX36 Timing Characteristics (Nominal 3.3V Operation) (continued)**
**(Worst-Case Commercial Conditions, V<sub>CC</sub> = 3.0V, T<sub>J</sub> = 70°C)**

|  |                                      |        | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      |       |
|--|--------------------------------------|--------|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
| Parameter  | Description                          |        | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. | Units |
| <b>Input Module Propagation Delays</b>                   |                                      |        |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>INPY</sub>  | Input Data Pad-to-Y                  |        |            | 1.4  |            | 1.6  |            | 1.8  |             | 2.1  |            | 3.0  | ns    |
| t <sub>INGO</sub>  | Input Latch Gate-to-Output           |        |            | 2.0  |            | 2.2  |            | 2.5  |             | 2.9  |            | 4.1  | ns    |
| t <sub>INH</sub>   | Input Latch Hold                     |        | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>INSU</sub>  | Input Latch Set-Up                   |        | 0.7        |      | 0.7        |      | 0.8        |      | 1.0         |      | 1.4        |      | ns    |
| t <sub>ILA</sub>   | Latch Active Pulse Width             |        | 6.5        |      | 7.3        |      | 8.2        |      | 9.7         |      | 13.5       |      | ns    |
| <b>Input Module Predicted Routing Delays<sup>1</sup></b> |                                      |        |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>IRD1</sub>  | FO=1 Routing Delay                   |        |            | 2.8  |            | 3.1  |            | 3.5  |             | 4.07 |            | 5.7  | ns    |
| t <sub>IRD2</sub>  | FO=2 Routing Delay                   |        |            | 3.2  |            | 3.5  |            | 4.1  |             | 4.8  |            | 6.7  | ns    |
| t <sub>IRD3</sub>  | FO=3 Routing Delay                   |        |            | 3.7  |            | 4.1  |            | 4.7  |             | 5.5  |            | 7.7  | ns    |
| t <sub>IRD4</sub>  | FO=4 Routing Delay                   |        |            | 4.2  |            | 4.6  |            | 5.3  |             | 6.2  |            | 8.7  | ns    |
| t <sub>IRD8</sub>  | FO=8 Routing Delay                   |        |            | 6.1  |            | 6.8  |            | 7.7  |             | 9.0  |            | 12.6 | ns    |
| <b>Global Clock Network</b>                              |                                      |        |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>CKH</sub>   | Input LOW to HIGH                    | FO=32  |            | 4.6  |            | 5.1  |            | 5.7  |             | 6.7  |            | 9.3  | ns    |
|  |                                      | FO=635 |            | 5.0  |            | 5.6  |            | 6.3  |             | 7.4  |            | 10.3 | ns    |
| t <sub>CKL</sub>   | Input HIGH to LOW                    | FO=32  |            | 5.3  |            | 5.9  |            | 6.7  |             | 7.8  |            | 11.0 | ns    |
|  |                                      | FO=635 |            | 6.8  |            | 7.6  |            | 8.6  |             | 10.1 |            | 14.1 | ns    |
| t <sub>PWH</sub>   | Minimum Pulse Width HIGH             | FO=32  | 2.5        |      | 2.7        |      | 3.1        |      | 3.6         |      | 5.1        |      | ns    |
|  |                                      | FO=635 | 2.8        |      | 3.1        |      | 3.5        |      | 4.1         |      | 5.7        |      | ns    |
| t <sub>PWL</sub>   | Minimum Pulse Width LOW              | FO=32  | 2.5        |      | 2.7        |      | 3.1        |      | 3.6         |      | 5.1        |      | ns    |
|  |                                      | FO=635 | 2.8        |      | 3.1        |      | 3.5        |      | 4.1         |      | 5.7        |      | ns    |
| t <sub>CKSW</sub>  | Maximum Skew                         | FO=32  |            | 1.0  |            | 1.2  |            | 1.3  |             | 1.5  |            | 2.2  | ns    |
|  |                                      | FO=635 |            | 1.0  |            | 1.2  |            | 1.3  |             | 1.5  |            | 2.2  | ns    |
| t <sub>SUEXT</sub>                                       | Input Latch External Set-Up          | FO=32  | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
|  |                                      | FO=635 | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>HEXT</sub>  | Input Latch External Hold            | FO=32  | 4.0        |      | 4.4        |      | 5.0        |      | 5.9         |      | 8.2        |      | ns    |
|  |                                      | FO=635 | 4.6        |      | 5.2        |      | 5.9        |      | 6.9         |      | 9.6        |      | ns    |
| t <sub>P</sub>   | Minimum Period (1/f <sub>MAX</sub> ) | FO=32  | 9.2        |      | 10.2       |      | 11.1       |      | 12.7        |      | 21.2       |      | ns    |
|  |                                      | FO=635 | 9.9        |      | 11.0       |      | 12.0       |      | 13.8        |      | 23.0       |      | ns    |
| f <sub>HMAX</sub>  | Maximum Datapath Frequency           | FO=32  |            | 108  |            | 98   |            | 90   |             | 79   |            | 47   | MHz   |
|  |                                      | FO=635 |            | 100  |            | 91   |            | 83   |             | 73   |            | 44   | MHz   |

**Note:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

**A42MX36 Timing Characteristics (Nominal 3.3V Operation) (continued)****(Worst-Case Commercial Conditions,  $V_{CC} = 3.0V$ ,  $T_J = 70^\circ C$ )**

|  |  | '-3' Speed |      | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      |       |
|--|--|------------|------|------------|------|------------|------|-------------|------|------------|------|-------|
| Parameter                                    | Description  | Min.       | Max. | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. | Units |
| <b>TTL Output Module Timing<sup>1</sup></b>  |  |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>DLH</sub>                             | Data-to-Pad HIGH                                   |            | 3.6  |            | 4.0  |            | 4.5  |             | 5.3  |            | 7.4  | ns    |
| t <sub>DHL</sub>                             | Data-to-Pad LOW                                    |            | 4.2  |            | 4.6  |            | 5.2  |             | 6.2  |            | 8.6  | ns    |
| t <sub>ENZH</sub>                            | Enable Pad Z to HIGH                               |            | 3.7  |            | 4.2  |            | 4.7  |             | 5.5  |            | 7.7  | ns    |
| t <sub>ENZL</sub>                            | Enable Pad Z to LOW                                |            | 4.1  |            | 4.6  |            | 5.2  |             | 6.1  |            | 8.5  | ns    |
| t <sub>ENHZ</sub>                            | Enable Pad HIGH to Z                               |            | 7.34 |            | 8.2  |            | 9.3  |             | 10.9 |            | 15.3 | ns    |
| t <sub>ENLZ</sub>                            | Enable Pad LOW to Z                                |            | 6.9  |            | 7.6  |            | 8.7  |             | 10.2 |            | 14.3 | ns    |
| t <sub>GLH</sub>                             | G-to-Pad HIGH                                      |            | 4.9  |            | 5.5  |            | 6.2  |             | 7.3  |            | 10.2 | ns    |
| t <sub>GHL</sub>                             | G-to-Pad LOW                                       |            | 4.9  |            | 5.5  |            | 6.2  |             | 7.3  |            | 10.2 | ns    |
| t <sub>LSU</sub>                             | I/O Latch Output Set-Up                            | 0.7        |      | 0.7        |      | 0.8        |      | 1.0         |      | 1.4        |      | ns    |
| t <sub>LH</sub>                              | I/O Latch Output Hold                              | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>LCO</sub>                             | I/O Latch Clock-to-Out (Pad-to-Pad)<br>32 I/O      |            | 7.9  |            | 8.8  |            | 10.0 |             | 11.8 |            | 16.5 | ns    |
| t <sub>ACO</sub>                             | Array Latch Clock-to-Out<br>(Pad-to-Pad)<br>32 I/O |            | 10.9 |            | 12.1 |            | 13.7 |             | 16.1 |            | 22.5 | ns    |
| d <sub>TLH</sub>                             | Capacitive Loading, LOW to HIGH                    |            | 0.10 |            | 0.11 |            | 0.12 |             | 0.14 |            | 0.20 | ns/pF |
| d <sub>THL</sub>                             | Capacitive Loading, HIGH to LOW                    |            | 0.10 |            | 0.11 |            | 0.12 |             | 0.14 |            | 0.20 | ns/pF |
| <b>CMOS Output Module Timing<sup>1</sup></b> |  |            |      |            |      |            |      |             |      |            |      |       |
| t <sub>DLH</sub>                             | Data-to-Pad HIGH                                   |            | 4.9  |            | 5.5  |            | 6.2  |             | 7.3  |            | 10.3 | ns    |
| t <sub>DHL</sub>                             | Data-to-Pad LOW                                    |            | 3.4  |            | 3.8  |            | 4.3  |             | 5.1  |            | 7.1  | ns    |
| t <sub>ENZH</sub>                            | Enable Pad Z to HIGH                               |            | 3.7  |            | 4.1  |            | 4.7  |             | 5.5  |            | 7.7  | ns    |
| t <sub>ENZL</sub>                            | Enable Pad Z to LOW                                |            | 4.1  |            | 4.6  |            | 5.2  |             | 6.1  |            | 8.5  | ns    |
| t <sub>ENHZ</sub>                            | Enable Pad HIGH to Z                               |            | 7.4  |            | 8.2  |            | 9.3  |             | 10.9 |            | 15.3 | ns    |
| t <sub>ENLZ</sub>                            | Enable Pad LOW to Z                                |            | 6.9  |            | 7.6  |            | 8.7  |             | 10.2 |            | 14.3 | ns    |
| t <sub>GLH</sub>                             | G-to-Pad HIGH                                      |            | 7.0  |            | 7.8  |            | 8.9  |             | 10.4 |            | 14.6 | ns    |
| t <sub>GHL</sub>                             | G-to-Pad LOW                                       |            | 7.0  |            | 7.8  |            | 8.9  |             | 10.4 |            | 14.6 | ns    |
| t <sub>LSU</sub>                             | I/O Latch Set-Up                                   | 0.7        |      | 0.7        |      | 0.8        |      | 1.0         |      | 1.4        |      | ns    |
| t <sub>LH</sub>                              | I/O Latch Hold                                     | 0.0        |      | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>LCO</sub>                             | I/O Latch Clock-to-Out (Pad-to-Pad)<br>32 I/O      |            | 7.9  |            | 8.8  |            | 10.0 |             | 11.8 |            | 16.5 | ns    |
| t <sub>ACO</sub>                             | Array Latch Clock-to-Out<br>(Pad-to-Pad)<br>32 I/O |            | 10.9 |            | 12.1 |            | 13.7 |             | 16.1 |            | 22.5 | ns    |
| d <sub>TLH</sub>                             | Capacitive Loading, LOW to HIGH                    |            | 0.10 |            | 0.11 |            | 0.12 |             | 0.14 |            | 0.20 | ns/pF |
| d <sub>THL</sub>                             | Capacitive Loading, HIGH to LOW                    |            | 0.10 |            | 0.11 |            | 0.12 |             | 0.14 |            | 0.20 | ns/pF |

**Note:**

1. Delays based on 35 pF loading.

**A42MX36 Timing Characteristics (Nominal 5.0V Operation)**
**(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^\circ C$ )**

| Parameter  | Description                                | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      | Units |
|--|--|------------|------|------------|------|-------------|------|------------|------|-------|
|  |  | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. |       |
| <b>Logic Module Combinatorial Functions<sup>1</sup></b>  |  |            |      |            |      |             |      |            |      |       |
| $t_{PD}$   | Internal Array Module Delay                |            | 1.5  |            | 1.7  |             | 2.0  |            | 2.7  | ns    |
| $t_{PDD}$  | Internal Decode Module Delay               |            | 1.8  |            | 2.0  |             | 2.4  |            | 3.3  | ns    |
| <b>Logic Module Predicted Routing Delays<sup>2</sup></b> |  |            |      |            |      |             |      |            |      |       |
| $t_{RD1}$  | FO=1 Routing Delay                         |            | 1.0  |            | 1.2  |             | 1.4  |            | 2.0  | ns    |
| $t_{RD2}$  | FO=2 Routing Delay                         |            | 1.4  |            | 1.6  |             | 1.9  |            | 2.7  | ns    |
| $t_{RD3}$  | FO=3 Routing Delay                         |            | 1.8  |            | 2.0  |             | 2.4  |            | 3.4  | ns    |
| $t_{RD4}$  | FO=4 Routing Delay                         |            | 2.2  |            | 2.5  |             | 2.9  |            | 4.1  | ns    |
| $t_{RD5}$  | FO=8 Routing Delay                         |            | 3.7  |            | 4.2  |             | 4.9  |            | 6.9  | ns    |
| $t_{RDD}$  | Decode-to-Output Routing Delay             |            | 0.4  |            | 0.4  |             | 0.5  |            | 0.7  | ns    |
| <b>Logic Module Sequential Timing<sup>3, 4</sup></b>     |  |            |      |            |      |             |      |            |      |       |
| $t_{CO}$   | Flip-Flop Clock-to-Output                  |            | 1.4  |            | 1.6  |             | 1.9  |            | 2.7  | ns    |
| $t_{GO}$   | Latch Gate-to-Output                       |            | 1.4  |            | 1.6  |             | 1.9  |            | 2.7  | ns    |
| $t_{SU}$   | Flip-Flop (Latch) Set-Up Time              | 0.4        |      | 0.4        |      | 0.5         |      | 0.7        |      | ns    |
| $t_H$  | Flip-Flop (Latch) Hold Time                | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| $t_{RO}$   | Flip-Flop (Latch) Reset-to-Output          |            | 1.7  |            | 2.0  |             | 2.3  |            | 3.2  | ns    |
| $t_{SUENA}$  | Flip-Flop (Latch) Enable Set-Up            | 0.8        |      | 0.9        |      | 1.0         |      | 1.4        |      | ns    |
| $t_{HENA}$   | Flip-Flop (Latch) Enable Hold              | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| $t_{WCLKA}$  | Flip-Flop (Latch) Clock Active Pulse Width | 3.7        |      | 4.2        |      | 4.9         |      | 6.9        |      | ns    |
| $t_{WASYN}$  | Flip-Flop (Latch) Asynchronous Pulse Width | 4.8        |      | 5.5        |      | 6.4         |      | 9.0        |      | ns    |

**Notes:**

- For dual-module macros, use  $t_{PD1} + t_{RD1} + t_{PDn}$ ,  $t_{CO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate..
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
- Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
- Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.



**A42MX36 Timing Characteristics (Nominal 5.0V Operation) (continued)****(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^\circ C$ )**

| Logic Module Timing                 |                                     | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      |       |
|-------------------------------------|-------------------------------------|------------|------|------------|------|-------------|------|------------|------|-------|
| Parameter                           | Description                         | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. | Units |
| <b>Synchronous SRAM Operations</b>  |                                     |            |      |            |      |             |      |            |      |       |
| t <sub>RC</sub>                     | Read Cycle Time                     | 7.5        |      | 8.5        |      | 10.0        |      | 14.0       |      | ns    |
| t <sub>WC</sub>                     | Write Cycle Time                    | 7.5        |      | 8.5        |      | 10.0        |      | 14.0       |      | ns    |
| t <sub>RCKHL</sub>                  | Clock HIGH/LOW Time                 | 3.8        |      | 4.3        |      | 5.0         |      | 7.0        |      | ns    |
| t <sub>RCO</sub>                    | Data Valid After Clock HIGH/LOW     |            | 3.8  |            | 4.3  |             | 5.0  |            | 7.0  | ns    |
| t <sub>ADSU</sub>                   | Address/Data Set-Up Time            | 1.8        |      | 2.0        |      | 2.4         |      | 3.4        |      | ns    |
| t <sub>ADH</sub>                    | Address/Data Hold Time              | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>RENSU</sub>                  | Read Enable Set-Up                  | 0.7        |      | 0.8        |      | 0.9         |      | 1.3        |      | ns    |
| t <sub>RENH</sub>                   | Read Enable Hold                    | 3.8        |      | 4.3        |      | 5.0         |      | 7.0        |      | ns    |
| t <sub>WENSU</sub>                  | Write Enable Set-Up                 | 3.0        |      | 3.4        |      | 4.0         |      | 5.6        |      | ns    |
| t <sub>WENH</sub>                   | Write Enable Hold                   | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>BENS</sub>                   | Block Enable Set-Up                 | 3.1        |      | 3.5        |      | 4.1         |      | 5.7        |      | ns    |
| t <sub>BENH</sub>                   | Block Enable Hold                   | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| <b>Asynchronous SRAM Operations</b> |                                     |            |      |            |      |             |      |            |      |       |
| t <sub>RPD</sub>                    | Asynchronous Access Time            |            | 9.0  |            | 10.2 |             | 12.0 |            | 16.8 | ns    |
| t <sub>RDADV</sub>                  | Read Address Valid                  | 9.8        |      | 11.1       |      | 13.0        |      | 18.2       |      | ns    |
| t <sub>ADSU</sub>                   | Address/Data Set-Up Time            | 1.8        |      | 2.1        |      | 2.4         |      | 3.4        |      | ns    |
| t <sub>ADH</sub>                    | Address/Data Hold Time              | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>RENSUA</sub>                 | Read Enable Set-Up to Address Valid | 0.7        |      | 0.8        |      | 0.9         |      | 1.3        |      | ns    |
| t <sub>RENHA</sub>                  | Read Enable Hold                    | 3.8        |      | 4.3        |      | 5.0         |      | 7.0        |      | ns    |
| t <sub>WENSU</sub>                  | Write Enable Set-Up                 | 3.0        |      | 3.4        |      | 4.0         |      | 5.6        |      | ns    |
| t <sub>WENH</sub>                   | Write Enable Hold                   | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>DOH</sub>                    | Data Out Hold Time                  |            | 1.4  |            | 1.5  |             | 1.8  |            | 2.5  | ns    |

**A42MX36 Timing Characteristics (Nominal 5.0V Operation) (continued)**
**(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^{\circ}C$ )**

| Parameter  | Description                          |        | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      | Units |
|--|--------------------------------------|--------|------------|------|------------|------|-------------|------|------------|------|-------|
|  |                                      |        | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. |       |
| <b>Input Module Propagation Delays</b>                   |                                      |        |            |      |            |      |             |      |            |      |       |
| t <sub>INPY</sub>  | Input Data Pad-to-Y                  |        |            | 1.1  |            | 1.3  |             | 1.5  |            | 2.1  | ns    |
| t <sub>INGO</sub>  | Input Latch Gate-to-Output           |        |            | 1.6  |            | 1.8  |             | 2.1  |            | 2.9  | ns    |
| t <sub>INH</sub>   | Input Latch Hold                     |        | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>INSU</sub>  | Input Latch Set-Up                   |        | 0.5        |      | 0.6        |      | 0.7         |      | 1.0        |      | ns    |
| t <sub>ILA</sub>   | Latch Active Pulse Width             |        | 5.2        |      | 5.9        |      | 6.9         |      | 9.7        |      | ns    |
| <b>Input Module Predicted Routing Delays<sup>1</sup></b> |                                      |        |            |      |            |      |             |      |            |      |       |
| t <sub>IRD1</sub>  | FO=1 Routing Delay                   |        |            | 2.2  |            | 2.5  |             | 2.9  |            | 4.1  | ns    |
| t <sub>IRD2</sub>  | FO=2 Routing Delay                   |        |            | 2.6  |            | 2.9  |             | 3.4  |            | 4.8  | ns    |
| t <sub>IRD3</sub>  | FO=3 Routing Delay                   |        |            | 2.9  |            | 3.3  |             | 3.9  |            | 5.5  | ns    |
| t <sub>IRD4</sub>  | FO=4 Routing Delay                   |        |            | 3.3  |            | 3.8  |             | 4.4  |            | 6.2  | ns    |
| t <sub>IRD8</sub>  | FO=8 Routing Delay                   |        |            | 4.8  |            | 5.5  |             | 6.4  |            | 9.0  | ns    |
| <b>Global Clock Network</b>                              |                                      |        |            |      |            |      |             |      |            |      |       |
| t <sub>CKH</sub>   | Input LOW to HIGH                    | FO=32  |            | 3.0  |            | 3.4  |             | 4.0  |            | 5.6  | ns    |
|  |                                      | FO=635 |            | 3.3  |            | 3.8  |             | 4.4  |            | 6.2  | ns    |
| t <sub>CKL</sub>   | Input HIGH to LOW                    | FO=32  |            | 4.2  |            | 4.8  |             | 5.6  |            | 7.8  | ns    |
|  |                                      | FO=635 |            | 5.4  |            | 6.1  |             | 7.2  |            | 10.1 | ns    |
| t <sub>PWH</sub>   | Minimum Pulse Width HIGH             | FO=32  | 2.0        |      | 2.2        |      | 2.6         |      | 3.7        |      | ns    |
|  |                                      | FO=635 | 2.2        |      | 2.5        |      | 2.9         |      | 4.1        |      | ns    |
| t <sub>PWL</sub>   | Minimum Pulse Width LOW              | FO=32  | 2.0        |      | 2.2        |      | 2.6         |      | 3.7        |      | ns    |
|  |                                      | FO=635 | 2.2        |      | 2.5        |      | 2.9         |      | 4.1        |      | ns    |
| t <sub>CKSW</sub>  | Maximum Skew                         | FO=32  |            | 0.8  |            | 0.9  |             | 1.0  |            | 1.4  | ns    |
|  |                                      | FO=635 |            | 0.8  |            | 0.9  |             | 1.0  |            | 1.4  | ns    |
| t <sub>SUEXT</sub>                                       | Input Latch External Set-Up          | FO=32  | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
|  |                                      | FO=635 | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>HEXT</sub>  | Input Latch External Hold            | FO=32  | 3.2        |      | 3.6        |      | 4.2         |      | 5.9        |      | ns    |
|  |                                      | FO=635 | 3.7        |      | 4.2        |      | 4.9         |      | 6.9        |      | ns    |
| t <sub>P</sub>   | Minimum Period (1/f <sub>MAX</sub> ) | FO=32  | 6.1        |      | 6.6        |      | 7.6         |      | 12.7       |      | ns    |
|  |                                      | FO=635 | 6.6        |      | 7.2        |      | 8.3         |      | 13.8       |      | ns    |
| f <sub>HMAX</sub>  | Maximum Datapath Frequency           | FO=32  |            | 164  |            | 151  |             | 131  |            | 79   | MHz   |
|  |                                      | FO=635 |            | 151  |            | 139  |             | 121  |            | 73   | MHz   |

**Note:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

**A42MX36 Timing Characteristics (Nominal 5.0V Operation) (continued)****(Worst-Case Military Conditions,  $V_{CC} = 4.5V$ ,  $T_J = 125^\circ C$ )**

| Parameter                                    | Description                                     | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      | '-F' Speed |      | Units |
|--|---|------------|------|------------|------|-------------|------|------------|------|-------|
|  |   | Min.       | Max. | Min.       | Max. | Min.        | Max. | Min.       | Max. |       |
| <b>TTL Output Module Timing<sup>1</sup></b>  |   |            |      |            |      |             |      |            |      |       |
| t <sub>DLH</sub>                             | Data-to-Pad HIGH                                |            | 2.8  |            | 3.2  |             | 3.8  |            | 5.3  | ns    |
| t <sub>DHL</sub>                             | Data-to-Pad LOW                                 |            | 3.3  |            | 3.7  |             | 4.4  |            | 6.2  | ns    |
| t <sub>ENZH</sub>                            | Enable Pad Z to HIGH                            |            | 3.0  |            | 3.3  |             | 3.9  |            | 5.5  | ns    |
| t <sub>ENZL</sub>                            | Enable Pad Z to LOW                             |            | 3.3  |            | 3.7  |             | 4.3  |            | 6.1  | ns    |
| t <sub>ENHZ</sub>                            | Enable Pad HIGH to Z                            |            | 5.8  |            | 6.6  |             | 7.8  |            | 11.0 | ns    |
| t <sub>ENLZ</sub>                            | Enable Pad LOW to Z                             |            | 5.5  |            | 6.2  |             | 7.3  |            | 10.2 | ns    |
| t <sub>GLH</sub>                             | G-to-Pad HIGH                                   |            | 3.3  |            | 3.7  |             | 4.4  |            | 6.1  | ns    |
| t <sub>GHL</sub>                             | G-to-Pad LOW                                    |            | 3.3  |            | 3.7  |             | 4.4  |            | 6.1  | ns    |
| t <sub>LSU</sub>                             | I/O Latch Output Set-Up                         | 0.5        |      | 0.6        |      | 0.7         |      | 1.0        |      | ns    |
| t <sub>LH</sub>                              | I/O Latch Output Hold                           | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>LCO</sub>                             | I/O Latch Clock-to-Out (Pad-to-Pad)<br>32 I/O   |            | 6.3  |            | 7.1  |             | 8.4  |            | 11.8 | ns    |
| t <sub>ACO</sub>                             | Array Latch Clock-to-Out (Pad-to-Pad)<br>32 I/O |            | 8.6  |            | 9.8  |             | 11.5 |            | 16.1 | ns    |
| d <sub>TLH</sub>                             | Capacitive Loading, LOW to HIGH                 |            | 0.08 |            | 0.09 |             | 0.10 |            | 0.14 | ns/pF |
| d <sub>THL</sub>                             | Capacitive Loading, HIGH to LOW                 |            | 0.08 |            | 0.09 |             | 0.10 |            | 0.14 | ns/pF |
| <b>CMOS Output Module Timing<sup>1</sup></b> |   |            |      |            |      |             |      |            |      |       |
| t <sub>DLH</sub>                             | Data-to-Pad HIGH                                |            | 3.9  |            | 4.5  |             | 5.2  |            | 7.3  | ns    |
| t <sub>DHL</sub>                             | Data-to-Pad LOW                                 |            | 2.7  |            | 3.1  |             | 3.7  |            | 5.1  | ns    |
| t <sub>ENZH</sub>                            | Enable Pad Z to HIGH                            |            | 3.0  |            | 3.3  |             | 3.9  |            | 5.5  | ns    |
| t <sub>ENZL</sub>                            | Enable Pad Z to LOW                             |            | 3.3  |            | 3.7  |             | 4.3  |            | 6.1  | ns    |
| t <sub>ENHZ</sub>                            | Enable Pad HIGH to Z                            |            | 5.8  |            | 6.6  |             | 7.8  |            | 10.9 | ns    |
| t <sub>ENLZ</sub>                            | Enable Pad LOW to Z                             |            | 5.5  |            | 6.2  |             | 7.3  |            | 10.2 | ns    |
| t <sub>GLH</sub>                             | G-to-Pad HIGH                                   |            | 5.6  |            | 6.3  |             | 7.5  |            | 10.4 | ns    |
| t <sub>GHL</sub>                             | G-to-Pad LOW                                    |            | 5.6  |            | 6.3  |             | 7.5  |            | 10.4 | ns    |
| t <sub>LSU</sub>                             | I/O Latch Set-Up                                | 0.5        |      | 0.6        |      | 0.7         |      | 1.0        |      | ns    |
| t <sub>LH</sub>                              | I/O Latch Hold                                  | 0.0        |      | 0.0        |      | 0.0         |      | 0.0        |      | ns    |
| t <sub>LCO</sub>                             | I/O Latch Clock-to-Out (Pad-to-Pad)<br>32 I/O   |            | 6.3  |            | 7.1  |             | 8.4  |            | 11.8 | ns    |
| t <sub>ACO</sub>                             | Array Latch Clock-to-Out (Pad-to-Pad)<br>32 I/O |            | 8.6  |            | 9.78 |             | 11.5 |            | 16.1 | ns    |
| d <sub>TLH</sub>                             | Capacitive Loading, LOW to HIGH                 |            | 0.08 |            | 0.09 |             | 0.10 |            | 0.14 | ns/pF |
| d <sub>THL</sub>                             | Capacitive Loading, HIGH to LOW                 |            | 0.08 |            | 0.09 |             | 0.10 |            | 0.14 | ns/pF |

**Note:**

1. Delays based on 35 pF loading.

**A42MX36 Timing Characteristics (Nominal 3.3V Operation)**
**(Worst-Case Military Conditions,  $V_{CC} = 3.0V$ ,  $T_J = 125^{\circ}C$ )**

|  |  | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      |       |
|--|--|------------|------|------------|------|-------------|------|-------|
| Parameter  | Description                                | Min.       | Max. | Min.       | Max. | Min.        | Max. | Units |
| <b>Logic Module Combinatorial Functions<sup>1</sup></b>  |  |            |      |            |      |             |      |       |
| $t_{PD}$   | Internal Array Module Delay                |            | 2.4  |            | 2.7  |             | 3.2  | ns    |
| $t_{PDD}$  | Internal Decode Module Delay               |            | 2.9  |            | 3.3  |             | 3.9  | ns    |
| <b>Logic Module Predicted Routing Delays<sup>2</sup></b> |  |            |      |            |      |             |      |       |
| $t_{RD1}$  | FO=1 Routing Delay                         |            | 1.7  |            | 2.0  |             | 2.3  | ns    |
| $t_{RD2}$  | FO=2 Routing Delay                         |            | 2.3  |            | 2.6  |             | 3.1  | ns    |
| $t_{RD3}$  | FO=3 Routing Delay                         |            | 2.9  |            | 3.3  |             | 3.9  | ns    |
| $t_{RD4}$  | FO=4 Routing Delay                         |            | 3.6  |            | 4.0  |             | 4.7  | ns    |
| $t_{RD5}$  | FO=8 Routing Delay                         |            | 6.0  |            | 6.8  |             | 8.0  | ns    |
| $t_{RDD}$  | Decode-to-Output Routing Delay             |            | 6.7  |            | 0.8  |             | 0.9  | ns    |
| <b>Logic Module Sequential Timing<sup>3, 4</sup></b>     |  |            |      |            |      |             |      |       |
| $t_{CO}$   | Flip-Flop Clock-to-Output                  |            | 2.4  |            | 2.7  |             | 3.1  | ns    |
| $t_{GO}$   | Latch Gate-to-Output                       |            | 2.4  |            | 2.7  |             | 3.1  | ns    |
| $t_{SU}$   | Flip-Flop (Latch) Set-Up Time              | 0.6        |      | 0.7        |      | 0.8         |      | ns    |
| $t_H$  | Flip-Flop (Latch) Hold Time                | 0.0        |      | 0.0        |      | 0.0         |      | ns    |
| $t_{RO}$   | Flip-Flop (Latch) Reset-to-Output          |            | 2.9  |            | 3.2  |             | 3.8  | ns    |
| $t_{SUENA}$  | Flip-Flop (Latch) Enable Set-Up            | 1.3        |      | 1.4        |      | 1.7         |      | ns    |
| $t_{HENA}$   | Flip-Flop (Latch) Enable Hold              | 0.0        |      | 0.0        |      | 0.0         |      | ns    |
| $t_{WCLKA}$  | Flip-Flop (Latch) Clock Active Pulse Width | 6.0        |      | 6.8        |      | 8.0         |      | ns    |
| $t_{WASYN}$  | Flip-Flop (Latch) Asynchronous Pulse Width | 7.9        |      | 8.9        |      | 10.5        |      | ns    |

**Notes:**

- For dual-module macros, use  $t_{PD1} + t_{RD1} + t_{PDn}$ ,  $t_{CO} + t_{RD1} + t_{PDn}$ , or  $t_{PD1} + t_{RD1} + t_{SUD}$ , whichever is appropriate.
- Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.
- Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the Timer utility.
- Set-up and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.

**A42MX36 Timing Characteristics (Nominal 3.3V Operation) (continued)****(Worst-Case Military Conditions,  $V_{CC} = 3.0V$ ,  $T_J = 125^{\circ}C$ )**

| Logic Module Timing                 |                                     | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      |       |
|-------------------------------------|-------------------------------------|------------|------|------------|------|-------------|------|-------|
| Parameter                           | Description                         | Min.       | Max. | Min.       | Max. | Min.        | Max. | Units |
| <b>Synchronous SRAM Operations</b>  |                                     |            |      |            |      |             |      |       |
| $t_{RC}$                            | Read Cycle Time                     | 12.1       |      | 13.8       |      | 16.2        |      | ns    |
| $t_{WC}$                            | Write Cycle Time                    | 12.1       |      | 13.8       |      | 16.2        |      | ns    |
| $t_{RCKHL}$                         | Clock HIGH/LOW Time                 | 6.1        |      | 6.9        |      | 8.1         |      | ns    |
| $t_{RCO}$                           | Data Valid After Clock HIGH/LOW     |            | 6.2  |            | 7.0  |             | 8.2  | ns    |
| $t_{ADSU}$                          | Address/Data Set-Up Time            | 2.9        |      | 3.2        |      | 3.9         |      | ns    |
| $t_{ADH}$                           | Address/Data Hold Time              | 0.0        |      | 0.0        |      | 0.0         |      | ns    |
| $t_{RENSU}$                         | Read Enable Set-Up                  |            |      | 1.2        |      | 1.5         |      | ns    |
| $t_{RENH}$                          | Read Enable Hold                    | 6.1        |      | 6.9        |      | 8.1         |      | ns    |
| $t_{WENSU}$                         | Write Enable Set-Up                 | 4.8        |      | 5.5        |      | 6.4         |      | ns    |
| $t_{WENH}$                          | Write Enable Hold                   | 0.0        |      | 0.0        |      | 0.0         |      | ns    |
| $t_{BENS}$                          | Block Enable Set-Up                 | 4.9        |      | 5.6        |      | 6.6         |      | ns    |
| $t_{BENH}$                          | Block Enable Hold                   | 0.0        |      | 0.0        |      | 0.0         |      | ns    |
| <b>Asynchronous SRAM Operations</b> |                                     |            |      |            |      |             |      |       |
| $t_{RPD}$                           | Asynchronous Access Time            |            | 14.7 |            | 16.6 |             | 19.5 | ns    |
| $t_{RDADV}$                         | Read Address Valid                  | 15.9       |      | 18.0       |      | 21.1        |      | ns    |
| $t_{ADSU}$                          | Address/Data Set-Up Time            | 2.9        |      | 3.2        |      | 3.9         |      | ns    |
| $t_{ADH}$                           | Address/Data Hold Time              | 0.0        |      | 0.0        |      | 0.0         |      | ns    |
| $t_{RENSUA}$                        | Read Enable Set-Up to Address Valid | 1.1        |      | 1.2        |      | 1.5         |      | ns    |
| $t_{RENHA}$                         | Read Enable Hold                    | 6.1        |      | 6.9        |      | 8.1         |      | ns    |
| $t_{WENSU}$                         | Write Enable Set-Up                 | 4.8        |      | 5.5        |      | 6.4         |      | ns    |
| $t_{WENH}$                          | Write Enable Hold                   | 0.0        |      | 0.0        |      | 0.0         |      | ns    |
| $t_{DOH}$                           | Data Out Hold Time                  |            | 2.4  |            | 2.5  |             | 2.9  | ns    |

**A42MX36 Timing Characteristics (Nominal 3.3V Operation) (continued)**
**(Worst-Case Military Conditions,  $V_{CC} = 3.0V$ ,  $T_J = 125^{\circ}C$ )**

|  |                                |        | '-2' Speed |      | '-1' Speed |      | 'Std' Speed |      |       |
|--|--------------------------------|--------|------------|------|------------|------|-------------|------|-------|
| Parameter  | Description                    |        | Min.       | Max. | Min.       | Max. | Min.        | Max. | Units |
| <b>Input Module Propagation Delays</b>                   |                                |        |            |      |            |      |             |      |       |
| $t_{INPY}$   | Input Data Pad-to-Y            |        |            | 1.9  |            | 2.1  |             | 2.5  | ns    |
| $t_{INGO}$   | Input Latch Gate-to-Output     |        |            | 2.6  |            | 2.9  |             | 3.4  | ns    |
| $t_{INH}$  | Input Latch Hold               |        | 0.0        |      | 0.0        |      | 0.0         |      | ns    |
| $t_{INSU}$   | Input Latch Set-Up             |        | 0.8        |      | 0.9        |      | 1.1         |      | ns    |
| $t_{ILA}$  | Latch Active Pulse Width       |        | 8.4        |      | 9.5        |      | 11.2        |      | ns    |
| <b>Input Module Predicted Routing Delays<sup>1</sup></b> |                                |        |            |      |            |      |             |      |       |
| $t_{IRD1}$   | FO=1 Routing Delay             |        |            | 3.6  |            | 4.0  |             | 4.8  | ns    |
| $t_{IRD2}$   | FO=2 Routing Delay             |        |            | 4.2  |            | 4.7  |             | 5.6  | ns    |
| $t_{IRD3}$   | FO=3 Routing Delay             |        |            | 4.8  |            | 5.4  |             | 6.4  | ns    |
| $t_{IRD4}$   | FO=4 Routing Delay             |        |            | 5.4  |            | 6.1  |             | 7.2  | ns    |
| $t_{IRD8}$   | FO=8 Routing Delay             |        |            | 7.9  |            | 8.9  |             | 10.5 | ns    |
| <b>Global Clock Network</b>                              |                                |        |            |      |            |      |             |      |       |
| $t_{CKH}$  | Input LOW to HIGH              | FO=32  |            | 5.9  |            | 6.7  |             | 7.8  | ns    |
|  |                                | FO=635 |            | 6.5  |            | 7.3  |             | 8.6  | ns    |
| $t_{CKL}$  | Input HIGH to LOW              | FO=32  |            | 6.9  |            | 7.8  |             | 9.1  | ns    |
|  |                                | FO=635 |            | 8.8  |            | 10.0 |             | 11.7 | ns    |
| $t_{PWH}$  | Minimum Pulse Width HIGH       | FO=32  | 3.1        |      | 3.5        |      | 4.2         |      | ns    |
|  |                                | FO=635 | 3.5        |      | 4.0        |      | 4.7         |      | ns    |
| $t_{PWL}$  | Minimum Pulse Width LOW        | FO=32  | 3.1        |      | 3.5        |      | 4.2         |      | ns    |
|  |                                | FO=635 | 3.5        |      | 4.0        |      | 4.7         |      | ns    |
| $t_{CKSW}$   | Maximum Skew                   | FO=32  |            | 1.4  |            | 1.6  |             | 1.8  | ns    |
|  |                                | FO=635 |            | 1.4  |            | 1.6  |             | 1.8  | ns    |
| $t_{SUEXT}$  | Input Latch External Set-Up    | FO=32  | 0.0        |      | 0.0        |      | 0.0         |      | ns    |
|  |                                | FO=635 | 0.0        |      | 0.0        |      | 0.0         |      | ns    |
| $t_{HEXT}$   | Input Latch External Hold      | FO=32  | 5.1        |      | 5.8        |      | 6.8         |      | ns    |
|  |                                | FO=635 | 5.9        |      | 6.7        |      | 7.9         |      | ns    |
| $t_P$  | Minimum Period ( $1/f_{MAX}$ ) | FO=32  | 11.8       |      | 12.8       |      | 14.7        |      | ns    |
|  |                                | FO=635 | 12.7       |      | 13.8       |      | 15.9        |      | ns    |
| $f_{HMAX}$   | Maximum Datapath Frequency     | FO=32  |            | 85   |            | 78   |             | 67   | MHz   |
|  |                                | FO=635 |            | 78   |            | 71   |             | 62   | MHz   |

**Note:**

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

**A42MX36 Timing Characteristics (Nominal 3.3V Operation) (continued)****(Worst-Case Military Conditions,  $V_{CC} = 3.0V$ ,  $T_J = 125^\circ C$ )**

| Parameter                                    | Description                                     | ‘-2’ Speed |      | ‘-1’ Speed |      | ‘Std’ Speed |      | Units |
|--|---|------------|------|------------|------|-------------|------|-------|
|  |   | Min.       | Max. | Min.       | Max. | Min.        | Max. |       |
| <b>TTL Output Module Timing<sup>1</sup></b>  |   |            |      |            |      |             |      |       |
| t <sub>DLH</sub>                             | Data-to-Pad HIGH                                |            | 4.6  |            | 5.2  |             | 6.2  | ns    |
| t <sub>DHL</sub>                             | Data-to-Pad LOW                                 |            | 5.3  |            | 6.1  |             | 7.2  | ns    |
| t <sub>ENZH</sub>                            | Enable Pad Z to HIGH                            |            | 4.8  |            | 5.4  |             | 6.4  | ns    |
| t <sub>ENZL</sub>                            | Enable Pad Z to LOW                             |            | 5.3  |            | 6.0  |             | 7.1  | ns    |
| t <sub>ENHZ</sub>                            | Enable Pad HIGH to Z                            |            | 9.5  |            | 10.8 |             | 12.7 | ns    |
| t <sub>ENLZ</sub>                            | Enable Pad LOW to Z                             |            | 8.9  |            | 10.0 |             | 11.8 | ns    |
| t <sub>GLH</sub>                             | G-to-Pad HIGH                                   |            | 6.3  |            | 7.2  |             | 8.4  | ns    |
| t <sub>GHL</sub>                             | G-to-Pad LOW                                    |            | 6.3  |            | 7.2  |             | 8.4  | ns    |
| t <sub>LSU</sub>                             | I/O Latch Output Set-Up                         | 0.8        |      | 0.9        |      | 1.1         |      | ns    |
| t <sub>LH</sub>                              | I/O Latch Output Hold                           | 0.0        |      | 0.0        |      | 0.0         |      | ns    |
| t <sub>LCO</sub>                             | I/O Latch Clock-to-Out (Pad-to-Pad)<br>32 I/O   |            | 10.2 |            | 11.6 |             | 13.7 | ns    |
| t <sub>ACO</sub>                             | Array Latch Clock-to-Out (Pad-to-Pad)<br>32 I/O |            | 14.0 |            | 15.9 |             | 18.7 | ns    |
| d <sub>TLH</sub>                             | Capacitive Loading, LOW to HIGH                 |            | 0.13 |            | 0.14 |             | 0.16 | ns/pF |
| d <sub>THL</sub>                             | Capacitive Loading, HIGH to LOW                 |            | 0.13 |            | 0.14 |             | 0.16 | ns/pF |
| <b>CMOS Output Module Timing<sup>1</sup></b> |   |            |      |            |      |             |      |       |
| t <sub>DLH</sub>                             | Data-to-Pad HIGH                                |            | 6.4  |            | 7.3  |             | 8.5  | ns    |
| t <sub>DHL</sub>                             | Data-to-Pad LOW                                 |            | 4.5  |            | 5.1  |             | 5.9  | ns    |
| t <sub>ENZH</sub>                            | Enable Pad Z to HIGH                            |            | 4.8  |            | 5.5  |             | 6.4  | ns    |
| t <sub>ENZL</sub>                            | Enable Pad Z to LOW                             |            | 5.3  |            | 6.0  |             | 7.1  | ns    |
| t <sub>ENHZ</sub>                            | Enable Pad HIGH to Z                            |            | 9.5  |            | 10.8 |             | 12.7 | ns    |
| t <sub>ENLZ</sub>                            | Enable Pad LOW to Z                             |            | 8.9  |            | 10.0 |             | 11.8 | ns    |
| t <sub>GLH</sub>                             | G-to-Pad HIGH                                   |            | 9.1  |            | 10.3 |             | 12.1 | ns    |
| t <sub>GHL</sub>                             | G-to-Pad LOW                                    |            | 9.1  |            | 10.3 |             | 12.1 | ns    |
| t <sub>LSU</sub>                             | I/O Latch Set-Up                                | 0.8        |      | 0.9        |      | 1.1         |      | ns    |
| t <sub>LH</sub>                              | I/O Latch Hold                                  | 0.0        |      | 0.0        |      | 0.0         |      | ns    |
| t <sub>LCO</sub>                             | I/O Latch Clock-to-Out (Pad-to-Pad)<br>32 I/O   |            | 10.2 |            | 13.7 |             | 13.7 | ns    |
| t <sub>ACO</sub>                             | Array Latch Clock-to-Out (Pad-to-Pad)<br>32 I/O |            | 14.0 |            | 18.7 |             | 18.7 | ns    |
| d <sub>TLH</sub>                             | Capacitive Loading, LOW to HIGH                 |            | 0.13 |            | 0.16 |             | 0.16 | ns/pF |
| d <sub>THL</sub>                             | Capacitive Loading, HIGH to LOW                 |            | 0.13 |            | 0.16 |             | 0.16 | ns/pF |

**Note:**

1. Delays based on 35 pF loading.

## Pin Descriptions

### **CLK, CLKA,**

#### **CLKB      Global Clock (Input)**

TTL clock inputs for clock distribution networks. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

#### **DCLK      Diagnostic Clock (Input)**

TTL clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

#### **GND      Ground (Input)**

Input LOW supply voltage.

#### **I/O      Input/Output (Input, Output)**

Input, output, tri-state, or bi-directional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven LOW by the Designer Series software.

#### **LP      Low Power Mode**

Controls the low power mode of all 42MX devices. This pin must be set HIGH to switch the device to low power mode. To exit the LOW power mode, the LP pin must be set LOW.

#### **MODE      Mode (Input)**

Controls the use of multifunction pins (DCLK, PRA, PRB, SDI, TDO). To provide verification capability, the MODE pin should be held HIGH. To facilitate this, the MODE pin should be terminated to GND through a 10K $\frac{3}{4}$  resistor so that the MODE pin can be pulled HIGH when required.

#### **NC      No Connection**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

#### **PRA, I/O      Probe A (Output)**

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

#### **PRB, I/O      Probe B (Output)**

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is

accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

#### **QCLKA,B,C,D Quadrant Clock (Input/Output)**

Quadrant clock inputs. When not used as a register control signal, these pins can function as general-purpose I/Os.

#### **SDI      Serial Data Input (Input)**

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

#### **SDO, TDO,**

#### **I/O      Serial Data (Output)**

Serial data output for diagnostic probe and device programming. SDO is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW. SDO is not available for 40MX devices.

#### **TCK      Test Clock**

Clock signal to shift the Boundary Scan Test (BST) data into the device. This pin functions as an I/O when the test fuse is not programmed. BST pins are only available in the A42MX24, A42MX24A, and A42MX36 devices.

#### **TDI      Test Data In**

Serial data input for BST instructions and data. Data is shifted in on the rising edge of TCK. This pin functions as an I/O when the test fuse is not programmed. BST pins are only available in the A42MX24 and A42MX36 devices.

#### **TDO      Test Data Out**

Serial data output for BST instructions and test data. This pin functions as an I/O when the test fuse is not programmed. BST pins are only available in the A42MX24 and A42MX36 devices.

#### **TMS      Test Mode Select**

Serial data input for boundary scan test mode. Data is shifted in on the rising edge of TCK. This pin functions as an I/O when the test fuse is not programmed. BST pins are only available in the A42MX24 and A42MX36 devices.

#### **V<sub>CC</sub>      Supply Voltage (Input)**

Input HIGH supply voltage.

#### **V<sub>CCA</sub>      Supply Voltage (Input)**

Input HIGH supply voltage, supplies array core only.

#### **V<sub>CCI</sub>      Supply Voltage (Input)**

Input HIGH supply voltage, supplies I/O cells only.

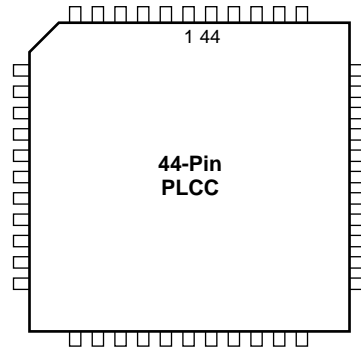
#### **WD      Wide Decode Output**

When a wide decode module is used in a 42MX device, this pin can be used as a dedicated output from the wide decode module. This direct connection eliminates additional interconnect delays associated with regular logic modules. To implement the direct I/O connection, connect an output buffer of any type to the output of the wide decode macro and place this output on one of the reserved WD pins.



Package Pin Assignments

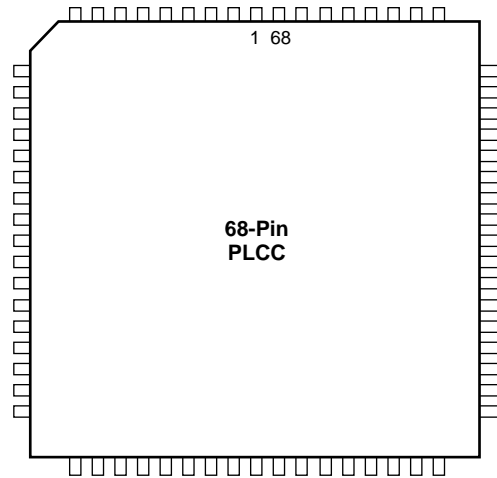
44-Pin PLCC



44-pin PLCC

| Pin Number | A40MX02 Function | A40MX04 Function |
|------------|------------------|------------------|
| 1          | I/O              | I/O              |
| 2          | I/O              | I/O              |
| 3          | V <sub>CC</sub>  | V <sub>CC</sub>  |
| 4          | I/O              | I/O              |
| 5          | I/O              | I/O              |
| 6          | I/O              | I/O              |
| 7          | I/O              | I/O              |
| 8          | I/O              | I/O              |
| 9          | I/O              | I/O              |
| 10         | GND              | GND              |
| 11         | I/O              | I/O              |
| 12         | I/O              | I/O              |
| 13         | I/O              | I/O              |
| 14         | V <sub>CC</sub>  | V <sub>CC</sub>  |
| 15         | I/O              | I/O              |
| 16         | V <sub>CC</sub>  | V <sub>CC</sub>  |
| 17         | I/O              | I/O              |
| 18         | I/O              | I/O              |
| 19         | I/O              | I/O              |
| 20         | I/O              | I/O              |
| 21         | GND              | GND              |
| 22         | I/O              | I/O              |

| Pin Number | A40MX02 Function | A40MX04 Function |
|------------|------------------|------------------|
| 23         | I/O              | I/O              |
| 24         | I/O              | I/O              |
| 25         | V <sub>CC</sub>  | V <sub>CC</sub>  |
| 26         | I/O              | I/O              |
| 27         | I/O              | I/O              |
| 28         | I/O              | I/O              |
| 29         | I/O              | I/O              |
| 30         | I/O              | I/O              |
| 31         | I/O              | I/O              |
| 32         | GND              | GND              |
| 33         | CLK, I/O         | CLK, I/O         |
| 34         | MODE             | MODE             |
| 35         | V <sub>CC</sub>  | V <sub>CC</sub>  |
| 36         | SDI, I/O         | SDI, I/O         |
| 37         | DCLK, I/O        | DCLK, I/O        |
| 38         | PRA, I/O         | PRA, I/O         |
| 39         | PRB, I/O         | PRB, I/O         |
| 40         | I/O              | I/O              |
| 41         | I/O              | I/O              |
| 42         | I/O              | I/O              |
| 43         | GND              | GND              |
| 44         | I/O              | I/O              |

**Package Pin Assignments**
**68-Pin PLCC**

**68-Pin PLCC**

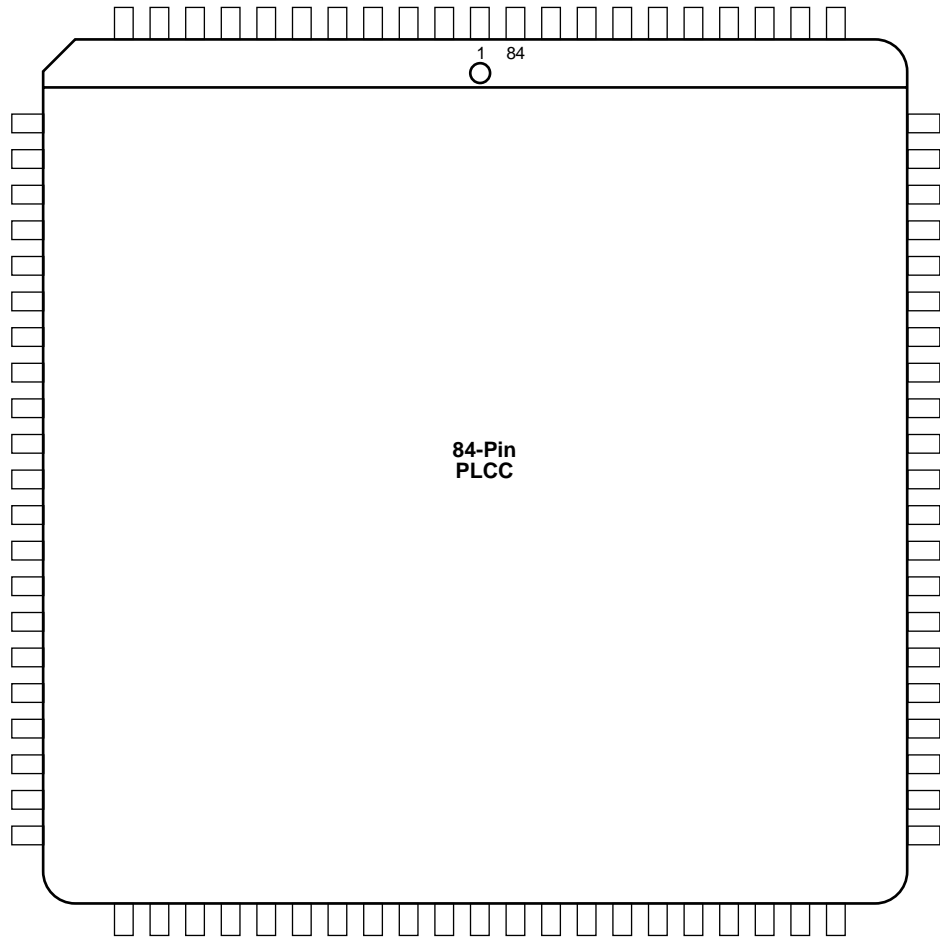
| Pin Number | A40MX02 Function | A40MX04 Function |
|------------|------------------|------------------|
| 1          | I/O              | I/O              |
| 2          | I/O              | I/O              |
| 3          | I/O              | I/O              |
| 4          | V <sub>CC</sub>  | V <sub>CC</sub>  |
| 5          | I/O              | I/O              |
| 6          | I/O              | I/O              |
| 7          | I/O              | I/O              |
| 8          | I/O              | I/O              |
| 9          | I/O              | I/O              |
| 10         | I/O              | I/O              |
| 11         | I/O              | I/O              |
| 12         | I/O              | I/O              |
| 13         | I/O              | I/O              |
| 14         | GND              | GND              |
| 15         | GND              | GND              |
| 16         | I/O              | I/O              |
| 17         | I/O              | I/O              |
| 18         | I/O              | I/O              |
| 19         | I/O              | I/O              |
| 20         | I/O              | I/O              |
| 21         | V <sub>CC</sub>  | V <sub>CC</sub>  |
| 22         | I/O              | I/O              |
| 23         | I/O              | I/O              |

| Pin Number | A40MX02 Function | A40MX04 Function |
|------------|------------------|------------------|
| 24         | I/O              | I/O              |
| 25         | V <sub>CC</sub>  | V <sub>CC</sub>  |
| 26         | I/O              | I/O              |
| 27         | I/O              | I/O              |
| 28         | I/O              | I/O              |
| 29         | I/O              | I/O              |
| 30         | I/O              | I/O              |
| 31         | I/O              | I/O              |
| 32         | GND              | GND              |
| 33         | I/O              | I/O              |
| 34         | I/O              | I/O              |
| 35         | I/O              | I/O              |
| 36         | I/O              | I/O              |
| 37         | I/O              | I/O              |
| 38         | V <sub>CC</sub>  | V <sub>CC</sub>  |
| 39         | I/O              | I/O              |
| 40         | I/O              | I/O              |
| 41         | I/O              | I/O              |
| 42         | I/O              | I/O              |
| 43         | I/O              | I/O              |
| 44         | I/O              | I/O              |
| 45         | I/O              | I/O              |
| 46         | I/O              | I/O              |

| Pin Number | A40MX02 Function | A40MX04 Function |
|------------|------------------|------------------|
| 47         | I/O              | I/O              |
| 48         | I/O              | I/O              |
| 49         | GND              | GND              |
| 50         | I/O              | I/O              |
| 51         | I/O              | I/O              |
| 52         | CLK, I/O         | CLK, I/O         |
| 53         | I/O              | I/O              |
| 54         | MODE             | MODE             |
| 55         | V <sub>CC</sub>  | V <sub>CC</sub>  |
| 56         | SDI, I/O         | SDI, I/O         |
| 57         | DCLK, I/O        | DCLK, I/O        |
| 58         | PRA, I/O         | PRA, I/O         |
| 59         | PRB, I/O         | PRB, I/O         |
| 60         | I/O              | I/O              |
| 61         | I/O              | I/O              |
| 62         | I/O              | I/O              |
| 63         | I/O              | I/O              |
| 64         | I/O              | I/O              |
| 65         | I/O              | I/O              |
| 66         | GND              | GND              |
| 67         | I/O              | I/O              |
| 68         | I/O              | I/O              |

**Package Pin Assignments (continued)**

**84-Pin PLCC**

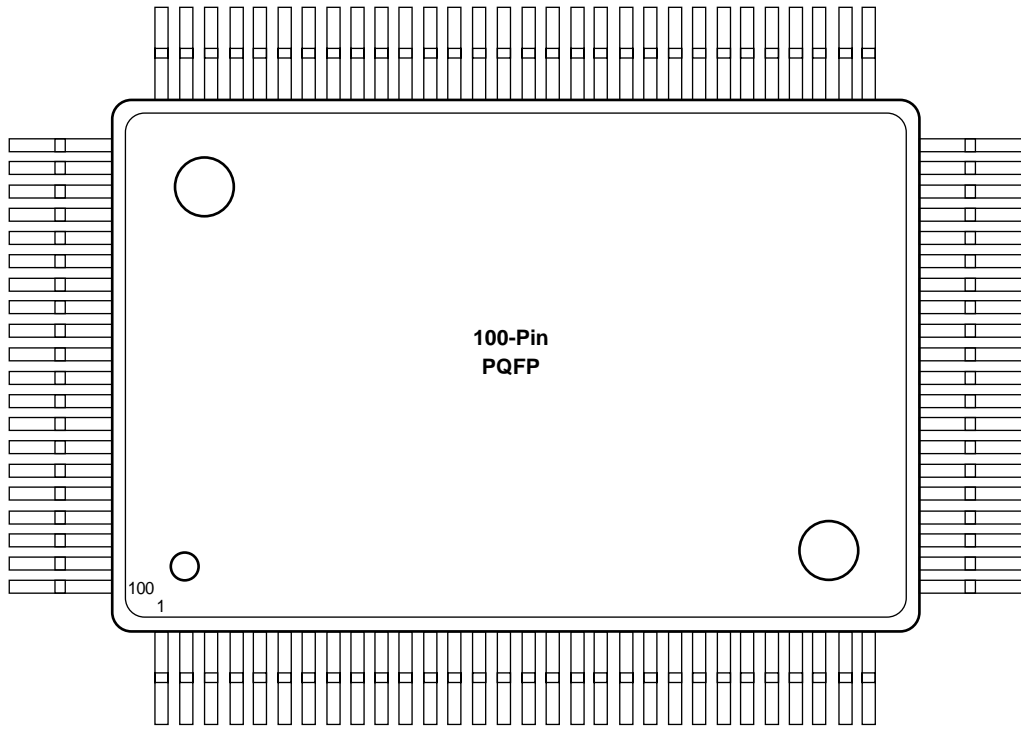


**84-Pin PLCC**

| Pin Number | A40MX04 Function | A42MX09 Function | A42MX16 Function | A42MX24 Function | Pin Number | A40MX04 Function | A42MX09 Function | A42MX16 Function | A42MX24 Function |
|------------|------------------|------------------|------------------|------------------|------------|------------------|------------------|------------------|------------------|
| 1          | I/O              | I/O              | I/O              | I/O              | 43         | I/O              | V <sub>CCA</sub> | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 2          | I/O              | CLKB, I/O        | CLKB, I/O        | CLKB, I/O        | 44         | I/O              | I/O              | I/O              | I/O (WD)         |
| 3          | I/O              | I/O              | I/O              | I/O              | 45         | I/O              | I/O              | I/O              | I/O (WD)         |
| 4          | V <sub>CC</sub>  | PRB, I/O         | PRB, I/O         | PRB, I/O         | 46         | V <sub>CC</sub>  | I/O              | I/O              | I/O (WD)         |
| 5          | I/O              | I/O              | I/O              | I/O (WD)         | 47         | I/O              | I/O              | I/O              | I/O (WD)         |
| 6          | I/O              | GND              | GND              | GND              | 48         | I/O              | I/O              | I/O              | I/O              |
| 7          | I/O              | I/O              | I/O              | I/O              | 49         | I/O              | GND              | GND              | GND              |
| 8          | I/O              | I/O              | I/O              | I/O (WD)         | 50         | I/O              | I/O              | I/O              | I/O (WD)         |
| 9          | I/O              | I/O              | I/O              | I/O (WD)         | 51         | I/O              | I/O              | I/O              | I/O (WD)         |
| 10         | I/O              | DCLK, I/O        | DCLK, I/O        | DCLK, I/O        | 52         | I/O              | SDO, I/O         | SDO, I/O         | SDO, TDO (WD)    |
| 11         | I/O              | I/O              | I/O              | I/O              | 53         | I/O              | I/O              | I/O              | I/O              |
| 12         | NC               | MODE             | MODE             | MODE             | 54         | I/O              | I/O              | I/O              | I/O              |
| 13         | I/O              | I/O              | I/O              | I/O              | 55         | I/O              | I/O              | I/O              | I/O              |
| 14         | I/O              | I/O              | I/O              | I/O              | 56         | I/O              | I/O              | I/O              | I/O              |
| 15         | I/O              | I/O              | I/O              | I/O              | 57         | I/O              | I/O              | I/O              | I/O              |
| 16         | I/O              | I/O              | I/O              | I/O              | 58         | I/O              | I/O              | I/O              | I/O              |
| 17         | I/O              | I/O              | I/O              | I/O              | 59         | I/O              | I/O              | I/O              | I/O              |
| 18         | GND              | I/O              | I/O              | I/O              | 60         | GND              | I/O              | I/O              | I/O              |
| 19         | GND              | I/O              | I/O              | I/O              | 61         | GND              | I/O              | I/O              | I/O              |
| 20         | I/O              | I/O              | I/O              | I/O              | 62         | I/O              | I/O              | I/O              | TCK, I/O         |
| 21         | I/O              | I/O              | I/O              | I/O              | 63         | I/O              | GND (LP)         | GND (LP)         | GND (LP)         |
| 22         | I/O              | V <sub>CCA</sub> | V <sub>CCI</sub> | V <sub>CCI</sub> | 64         | CLK, I/O         | V <sub>CCA</sub> | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 23         | I/O              | V <sub>CCI</sub> | V <sub>CCA</sub> | V <sub>CCA</sub> | 65         | I/O              | V <sub>CCI</sub> | V <sub>CCI</sub> | V <sub>CCI</sub> |
| 24         | I/O              | I/O              | I/O              | I/O              | 66         | MODE             | I/O              | I/O              | I/O              |
| 25         | V <sub>CC</sub>  | I/O              | I/O              | I/O              | 67         | V <sub>CC</sub>  | I/O              | I/O              | I/O              |
| 26         | V <sub>CC</sub>  | I/O              | I/O              | I/O              | 68         | V <sub>CC</sub>  | I/O              | I/O              | I/O              |
| 27         | I/O              | I/O              | I/O              | I/O              | 69         | I/O              | I/O              | I/O              | I/O              |
| 28         | I/O              | GND              | GND              | GND              | 70         | I/O              | GND              | GND              | GND              |
| 29         | I/O              | I/O              | I/O              | I/O              | 71         | I/O              | I/O              | I/O              | I/O              |
| 30         | I/O              | I/O              | I/O              | I/O              | 72         | SDI, I/O         | I/O              | I/O              | I/O              |
| 31         | I/O              | I/O              | I/O              | I/O              | 73         | DCLK, I/O        | I/O              | I/O              | I/O              |
| 32         | I/O              | I/O              | I/O              | I/O              | 74         | PRA, I/O         | I/O              | I/O              | I/O              |
| 33         | V <sub>CC</sub>  | I/O              | I/O              | I/O              | 75         | PRB, I/O         | I/O              | I/O              | I/O              |
| 34         | I/O              | I/O              | I/O              | TMS, I/O         | 76         | I/O              | SDI, I/O         | SDI, I/O         | SDI, I/O         |
| 35         | I/O              | I/O              | I/O              | TDI, I/O         | 77         | I/O              | I/O              | I/O              | I/O              |
| 36         | I/O              | I/O              | I/O              | I/O (WD)         | 78         | I/O              | I/O              | I/O              | I/O (WD)         |
| 37         | I/O              | I/O              | I/O              | I/O              | 79         | I/O              | I/O              | I/O              | I/O (WD)         |
| 38         | I/O              | I/O              | I/O              | I/O (WD)         | 80         | I/O              | I/O              | I/O              | I/O (WD)         |
| 39         | I/O              | I/O              | I/O              | I/O (WD)         | 81         | I/O              | PRA, I/O         | PRA, I/O         | PRA, I/O         |
| 40         | GND              | I/O              | I/O              | I/O              | 82         | GND              | I/O              | I/O              | I/O              |
| 41         | I/O              | I/O              | I/O              | I/O              | 83         | I/O              | CLKA, I/O        | CLKA, I/O        | CLKA, I/O        |
| 42         | I/O              | I/O              | I/O              | I/O              | 84         | I/O              | V <sub>CCA</sub> | V <sub>CCA</sub> | V <sub>CCA</sub> |

**Package Pin Assignments (continued)**

**100-Pin PQFP Package (Top View)**



**100-Pin PQFP**

| Pin Number | A40MX02 Function | A40MX04 Function | A42MX09 Function | A42MX16 Function |
|------------|------------------|------------------|------------------|------------------|
| 1          | NC               | NC               | I/O              | I/O              |
| 2          | NC               | NC               | DCLK, I/O        | DCLK, I/O        |
| 3          | NC               | NC               | I/O              | I/O              |
| 4          | NC               | NC               | MODE             | MODE             |
| 5          | NC               | NC               | I/O              | I/O              |
| 6          | PRB, I/O         | PRB, I/O         | I/O              | I/O              |
| 7          | I/O              | I/O              | I/O              | I/O              |
| 8          | I/O              | I/O              | I/O              | I/O              |
| 9          | I/O              | I/O              | GND              | GND              |
| 10         | I/O              | I/O              | I/O              | I/O              |
| 11         | I/O              | I/O              | I/O              | I/O              |
| 12         | I/O              | I/O              | I/O              | I/O              |
| 13         | GND              | GND              | I/O              | I/O              |
| 14         | I/O              | I/O              | I/O              | I/O              |
| 15         | I/O              | I/O              | I/O              | I/O              |
| 16         | I/O              | I/O              | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 17         | I/O              | I/O              | V <sub>CCI</sub> | V <sub>CCA</sub> |
| 18         | I/O              | I/O              | I/O              | I/O              |
| 19         | V <sub>CC</sub>  | V <sub>CC</sub>  | I/O              | I/O              |
| 20         | I/O              | I/O              | I/O              | I/O              |
| 21         | I/O              | I/O              | I/O              | I/O              |
| 22         | I/O              | I/O              | GND              | GND              |
| 23         | I/O              | I/O              | I/O              | I/O              |
| 24         | I/O              | I/O              | I/O              | I/O              |
| 25         | I/O              | I/O              | I/O              | I/O              |
| 26         | I/O              | I/O              | I/O              | I/O              |
| 27         | NC               | NC               | I/O              | I/O              |
| 28         | NC               | NC               | I/O              | I/O              |
| 29         | NC               | NC               | I/O              | I/O              |
| 30         | NC               | NC               | I/O              | I/O              |
| 31         | NC               | I/O              | I/O              | I/O              |
| 32         | NC               | I/O              | I/O              | I/O              |
| 33         | NC               | I/O              | I/O              | I/O              |
| 34         | I/O              | I/O              | GND              | GND              |
| 35         | I/O              | I/O              | I/O              | I/O              |
| 36         | GND              | GND              | I/O              | I/O              |
| 37         | GND              | GND              | I/O              | I/O              |
| 38         | I/O              | I/O              | I/O              | I/O              |
| 39         | I/O              | I/O              | I/O              | I/O              |

| Pin Number | A40MX02 Function | A40MX04 Function | A42MX09 Function | A42MX16 Function |
|------------|------------------|------------------|------------------|------------------|
| 40         | I/O              | I/O              | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 41         | I/O              | I/O              | I/O              | I/O              |
| 42         | I/O              | I/O              | I/O              | I/O              |
| 43         | V <sub>CC</sub>  | V <sub>CC</sub>  | I/O              | I/O              |
| 44         | V <sub>CC</sub>  | V <sub>CC</sub>  | I/O              | I/O              |
| 45         | I/O              | I/O              | I/O              | I/O              |
| 46         | I/O              | I/O              | GND              | GND              |
| 47         | I/O              | I/O              | I/O              | I/O              |
| 48         | NC               | I/O              | I/O              | I/O              |
| 49         | NC               | I/O              | I/O              | I/O              |
| 50         | NC               | I/O              | I/O              | I/O              |
| 51         | NC               | NC               | I/O              | I/O              |
| 52         | NC               | NC               | SDO, I/O         | SDO, I/O         |
| 53         | NC               | NC               | I/O              | I/O              |
| 54         | NC               | NC               | I/O              | I/O              |
| 55         | NC               | NC               | I/O              | I/O              |
| 56         | V <sub>CC</sub>  | V <sub>CC</sub>  | I/O              | I/O              |
| 57         | I/O              | I/O              | GND              | GND              |
| 58         | I/O              | I/O              | I/O              | I/O              |
| 59         | I/O              | I/O              | I/O              | I/O              |
| 60         | I/O              | I/O              | I/O              | I/O              |
| 61         | I/O              | I/O              | I/O              | I/O              |
| 62         | I/O              | I/O              | I/O              | I/O              |
| 63         | GND              | GND              | I/O              | I/O              |
| 64         | I/O              | I/O              | GND (LP)         | GND (LP)         |
| 65         | I/O              | I/O              | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 66         | I/O              | I/O              | V <sub>CCI</sub> | V <sub>CCI</sub> |
| 67         | I/O              | I/O              | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 68         | I/O              | I/O              | I/O              | I/O              |
| 69         | V <sub>CC</sub>  | V <sub>CC</sub>  | I/O              | I/O              |
| 70         | I/O              | I/O              | I/O              | I/O              |
| 71         | I/O              | I/O              | I/O              | I/O              |
| 72         | I/O              | I/O              | GND              | GND              |
| 73         | I/O              | I/O              | I/O              | I/O              |
| 74         | I/O              | I/O              | I/O              | I/O              |
| 75         | I/O              | I/O              | I/O              | I/O              |
| 76         | I/O              | I/O              | I/O              | I/O              |
| 77         | NC               | NC               | I/O              | I/O              |
| 78         | NC               | NC               | I/O              | I/O              |

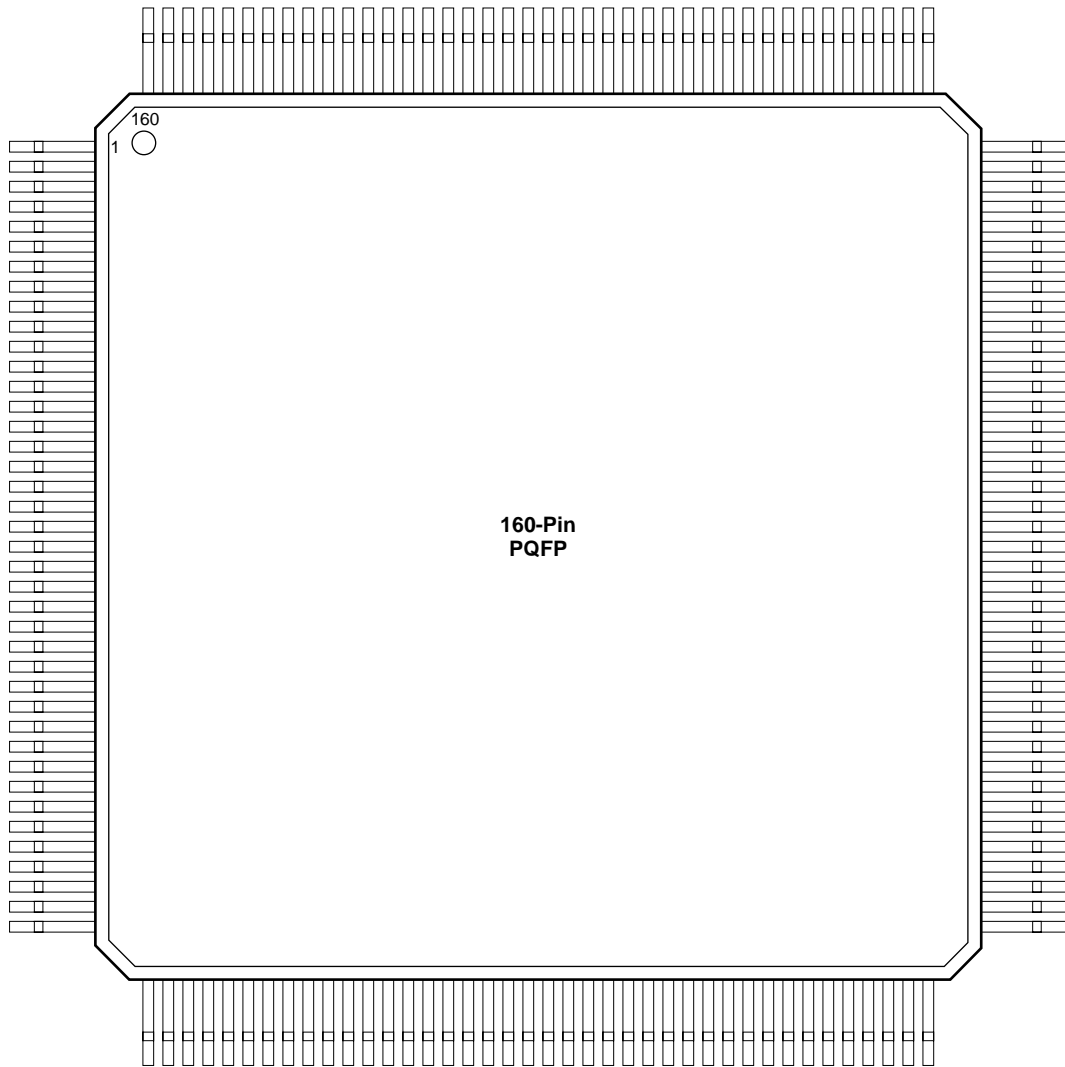
100-Pin PQFP (Continued)

| Pin Number | A40MX02 Function | A40MX04 Function | A42MX09 Function | A42MX16 Function |
|------------|------------------|------------------|------------------|------------------|
| 79         | NC               | NC               | SDI, I/O         | SDI, I/O         |
| 80         | NC               | I/O              | I/O              | I/O              |
| 81         | NC               | I/O              | I/O              | I/O              |
| 82         | NC               | I/O              | I/O              | I/O              |
| 83         | I/O              | I/O              | I/O              | I/O              |
| 84         | I/O              | I/O              | GND              | GND              |
| 85         | I/O              | I/O              | I/O              | I/O              |
| 86         | GND              | GND              | I/O              | I/O              |
| 87         | GND              | GND              | PRA, I/O         | PRA, I/O         |
| 88         | I/O              | I/O              | I/O              | I/O              |
| 89         | I/O              | I/O              | CLKA, I/O        | CLKA, I/O        |

| Pin Number | A40MX02 Function | A40MX04 Function | A42MX09 Function | A42MX16 Function |
|------------|------------------|------------------|------------------|------------------|
| 90         | CLK, I/O         | CLK, I/O         | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 91         | I/O              | I/O              | I/O              | I/O              |
| 92         | MODE             | MODE             | CLKB, I/O        | CLKB, I/O        |
| 93         | V <sub>CC</sub>  | V <sub>CC</sub>  | I/O              | I/O              |
| 94         | V <sub>CC</sub>  | V <sub>CC</sub>  | PRB, I/O         | PRB, I/O         |
| 95         | NC               | I/O              | I/O              | I/O              |
| 96         | NC               | I/O              | GND              | GND              |
| 97         | NC               | I/O              | I/O              | I/O              |
| 98         | SDI, I/O         | SDI, I/O         | I/O              | I/O              |
| 99         | DCLK, I/O        | DCLK, I/O        | I/O              | I/O              |
| 100        | PRA, I/O         | PRA, I/O         | I/O              | I/O              |

**Package Pin Assignments (continued)**

**160-Pin PQFP Package (Top View)**





160-Pin PQFP

| Pin Number | A42MX09 Function | A42MX16 Function | A42MX24 Function |
|------------|------------------|------------------|------------------|
| 1          | I/O              | I/O              | I/O              |
| 2          | DCLK, I/O        | DCLK, I/O        | DCLK, I/O        |
| 3          | NC               | I/O              | I/O              |
| 4          | I/O              | I/O              | I/O (WD)         |
| 5          | I/O              | I/O              | I/O (WD)         |
| 6          | NC               | V <sub>CCI</sub> | V <sub>CCI</sub> |
| 7          | I/O              | I/O              | I/O              |
| 8          | I/O              | I/O              | I/O              |
| 9          | I/O              | I/O              | I/O              |
| 10         | NC               | I/O              | I/O              |
| 11         | GND              | GND              | GND              |
| 12         | NC               | I/O              | I/O              |
| 13         | I/O              | I/O              | I/O (WD)         |
| 14         | I/O              | I/O              | I/O (WD)         |
| 15         | I/O              | I/O              | I/O              |
| 16         | PRB, I/O         | PRB, I/O         | PRB, I/O         |
| 17         | I/O              | I/O              | I/O              |
| 18         | CLKB, I/O        | CLKB, I/O        | CLKB, I/O        |
| 19         | I/O              | I/O              | I/O              |
| 20         | V <sub>CCA</sub> | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 21         | CLKA, I/O        | CLKA, I/O        | CLKA, I/O        |
| 22         | I/O              | I/O              | I/O              |
| 23         | PRA, I/O         | PRA, I/O         | PRA, I/O         |
| 24         | NC               | I/O              | I/O (WD)         |
| 25         | I/O              | I/O              | I/O (WD)         |
| 26         | I/O              | I/O              | I/O              |
| 27         | I/O              | I/O              | I/O              |
| 28         | NC               | I/O              | I/O              |
| 29         | I/O              | I/O              | I/O (WD)         |
| 30         | GND              | GND              | GND              |
| 31         | NC               | I/O              | I/O (WD)         |
| 32         | I/O              | I/O              | I/O              |
| 33         | I/O              | I/O              | I/O              |
| 34         | I/O              | I/O              | I/O              |
| 35         | NC               | V <sub>CCI</sub> | V <sub>CCI</sub> |
| 36         | I/O              | I/O              | I/O (WD)         |
| 37         | I/O              | I/O              | I/O (WD)         |
| 38         | SDI, I/O         | SDI, I/O         | SDI, I/O         |
| 39         | I/O              | I/O              | I/O              |
| 40         | GND              | GND              | GND              |

| Pin Number | A42MX09 Function | A42MX16 Function | A42MX24 Function |
|------------|------------------|------------------|------------------|
| 41         | I/O              | I/O              | I/O              |
| 42         | I/O              | I/O              | I/O              |
| 43         | I/O              | I/O              | I/O              |
| 44         | GND              | GND              | GND              |
| 45         | I/O              | I/O              | I/O              |
| 46         | I/O              | I/O              | I/O              |
| 47         | I/O              | I/O              | I/O              |
| 48         | I/O              | I/O              | I/O              |
| 49         | GND              | GND              | GND              |
| 50         | I/O              | I/O              | I/O              |
| 51         | I/O              | I/O              | I/O              |
| 52         | NC               | I/O              | I/O              |
| 53         | I/O              | I/O              | I/O              |
| 54         | NC               | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 55         | I/O              | I/O              | I/O              |
| 56         | I/O              | I/O              | I/O              |
| 57         | V <sub>CCA</sub> | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 58         | V <sub>CCI</sub> | V <sub>CCI</sub> | V <sub>CCI</sub> |
| 59         | GND              | GND              | GND              |
| 60         | V <sub>CCA</sub> | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 61         | GND (LP)         | GND (LP)         | GND (LP)         |
| 62         | I/O              | I/O              | TCK, I/O         |
| 63         | I/O              | I/O              | I/O              |
| 64         | GND              | GND              | GND              |
| 65         | I/O              | I/O              | I/O              |
| 66         | I/O              | I/O              | I/O              |
| 67         | I/O              | I/O              | I/O              |
| 68         | I/O              | I/O              | I/O              |
| 69         | GND              | GND              | GND              |
| 70         | NC               | I/O              | I/O              |
| 71         | I/O              | I/O              | I/O              |
| 72         | I/O              | I/O              | I/O              |
| 73         | I/O              | I/O              | I/O              |
| 74         | I/O              | I/O              | I/O              |
| 75         | NC               | I/O              | I/O              |
| 76         | I/O              | I/O              | I/O              |
| 77         | NC               | I/O              | I/O              |
| 78         | I/O              | I/O              | I/O              |
| 79         | NC               | I/O              | I/O              |
| 80         | GND              | GND              | GND              |

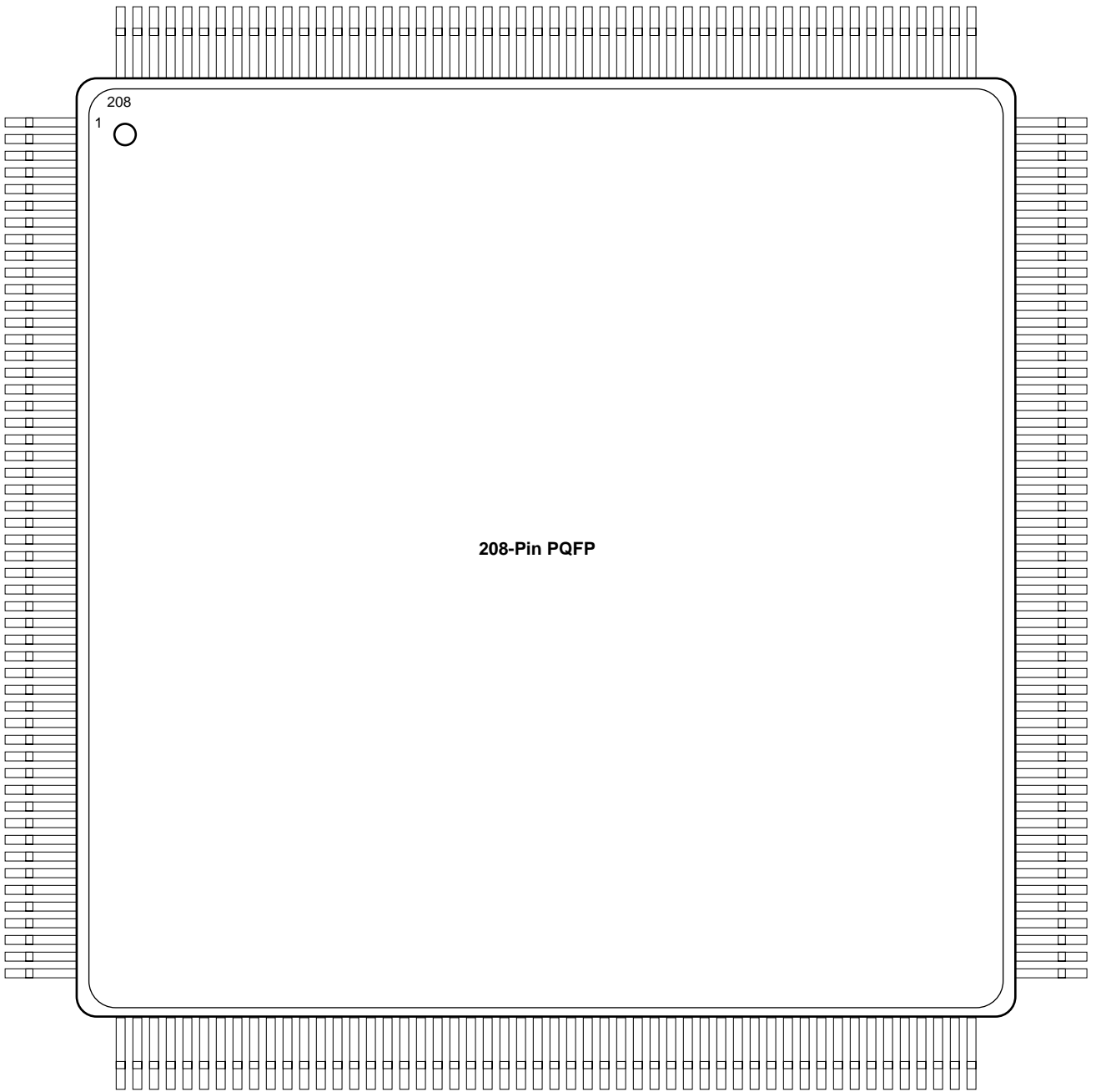
**160-Pin PQFP (Continued)**

| Pin Number | A42MX09 Function | A42MX16 Function | A42MX24 Function |
|------------|------------------|------------------|------------------|
| 81         | I/O              | I/O              | I/O              |
| 82         | SDO, I/O         | SDO, I/O         | SDO, TDO, I/O    |
| 83         | I/O              | I/O              | I/O (WD)         |
| 84         | I/O              | I/O              | I/O (WD)         |
| 85         | I/O              | I/O              | I/O              |
| 86         | NC               | V <sub>CCI</sub> | V <sub>CCI</sub> |
| 87         | I/O              | I/O              | I/O              |
| 88         | I/O              | I/O              | I/O (WD)         |
| 89         | GND              | GND              | GND              |
| 90         | NC               | I/O              | I/O              |
| 91         | I/O              | I/O              | I/O              |
| 92         | I/O              | I/O              | I/O              |
| 93         | I/O              | I/O              | I/O              |
| 94         | I/O              | I/O              | I/O              |
| 95         | I/O              | I/O              | I/O              |
| 96         | I/O              | I/O              | I/O (WD)         |
| 97         | I/O              | I/O              | I/O              |
| 98         | V <sub>CCA</sub> | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 99         | GND              | GND              | GND              |
| 100        | NC               | I/O              | I/O              |
| 101        | I/O              | I/O              | I/O              |
| 102        | I/O              | I/O              | I/O              |
| 103        | NC               | I/O              | I/O              |
| 104        | I/O              | I/O              | I/O              |
| 105        | I/O              | I/O              | I/O              |
| 106        | I/O              | I/O              | I/O (WD)         |
| 107        | I/O              | I/O              | I/O (WD)         |
| 108        | I/O              | I/O              | I/O              |
| 109        | GND              | GND              | GND              |
| 110        | NC               | I/O              | I/O              |
| 111        | I/O              | I/O              | I/O (WD)         |
| 112        | I/O              | I/O              | I/O (WD)         |
| 113        | I/O              | I/O              | I/O              |
| 114        | NC               | V <sub>CCI</sub> | V <sub>CCI</sub> |
| 115        | I/O              | I/O              | I/O (WD)         |
| 116        | NC               | I/O              | I/O (WD)         |
| 117        | I/O              | I/O              | I/O              |
| 118        | I/O              | I/O              | TDI, I/O         |
| 119        | I/O              | I/O              | TMS, I/O         |
| 120        | GND              | GND              | GND              |

| Pin Number | A42MX09 Function | A42MX16 Function | A42MX24 Function |
|------------|------------------|------------------|------------------|
| 121        | I/O              | I/O              | I/O              |
| 122        | I/O              | I/O              | I/O              |
| 123        | I/O              | I/O              | I/O              |
| 124        | NC               | I/O              | I/O              |
| 125        | GND              | GND              | GND              |
| 126        | I/O              | I/O              | I/O              |
| 127        | I/O              | I/O              | I/O              |
| 128        | I/O              | I/O              | I/O              |
| 129        | NC               | I/O              | I/O              |
| 130        | GND              | GND              | GND              |
| 131        | I/O              | I/O              | I/O              |
| 132        | I/O              | I/O              | I/O              |
| 133        | I/O              | I/O              | I/O              |
| 134        | I/O              | I/O              | I/O              |
| 135        | NC               | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 136        | I/O              | I/O              | I/O              |
| 137        | I/O              | I/O              | I/O              |
| 138        | NC               | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 139        | V <sub>CCI</sub> | V <sub>CCI</sub> | V <sub>CCI</sub> |
| 140        | GND              | GND              | GND              |
| 141        | NC               | I/O              | I/O              |
| 142        | I/O              | I/O              | I/O              |
| 143        | I/O              | I/O              | I/O              |
| 144        | I/O              | I/O              | I/O              |
| 145        | GND              | GND              | GND              |
| 146        | NC               | I/O              | I/O              |
| 147        | I/O              | I/O              | I/O              |
| 148        | I/O              | I/O              | I/O              |
| 149        | I/O              | I/O              | I/O              |
| 150        | NC               | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 151        | NC               | I/O              | I/O              |
| 152        | NC               | I/O              | I/O              |
| 153        | NC               | I/O              | I/O              |
| 154        | NC               | I/O              | I/O              |
| 155        | GND              | GND              | GND              |
| 156        | I/O              | I/O              | I/O              |
| 157        | I/O              | I/O              | I/O              |
| 158        | I/O              | I/O              | I/O              |
| 159        | MODE             | MODE             | MODE             |
| 160        | GND              | GND              | GND              |

**Package Pin Assignments (continued)**

**208-Pin PQFP Package (Top View)**



**208-Pin PQFP**

| Pin Number | A42MX16 Function | A42MX24 Function | A42MX36 Function |
|------------|------------------|------------------|------------------|
| 1          | GND              | GND              | GND              |
| 2          | NC               | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 3          | MODE             | MODE             | MODE             |
| 4          | I/O              | I/O              | I/O              |
| 5          | I/O              | I/O              | I/O              |
| 6          | I/O              | I/O              | I/O              |
| 7          | I/O              | I/O              | I/O              |
| 8          | I/O              | I/O              | I/O              |
| 9          | NC               | I/O              | I/O              |
| 10         | NC               | I/O              | I/O              |
| 11         | NC               | I/O              | I/O              |
| 12         | I/O              | I/O              | I/O              |
| 13         | I/O              | I/O              | I/O              |
| 14         | I/O              | I/O              | I/O              |
| 15         | I/O              | I/O              | I/O              |
| 16         | NC               | I/O              | I/O              |
| 17         | V <sub>CCA</sub> | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 18         | I/O              | I/O              | I/O              |
| 19         | I/O              | I/O              | I/O              |
| 20         | I/O              | I/O              | I/O              |
| 21         | I/O              | I/O              | I/O              |
| 22         | GND              | GND              | GND              |
| 23         | I/O              | I/O              | I/O              |
| 24         | I/O              | I/O              | I/O              |
| 25         | I/O              | I/O              | I/O              |
| 26         | I/O              | I/O              | I/O              |
| 27         | GND              | GND              | GND              |
| 28         | V <sub>CCI</sub> | V <sub>CCI</sub> | V <sub>CCI</sub> |
| 29         | V <sub>CCA</sub> | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 30         | I/O              | I/O              | I/O              |
| 31         | I/O              | I/O              | I/O              |
| 32         | V <sub>CCA</sub> | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 33         | I/O              | I/O              | I/O              |
| 34         | I/O              | I/O              | I/O              |
| 35         | I/O              | I/O              | I/O              |
| 36         | I/O              | I/O              | I/O              |
| 37         | I/O              | I/O              | I/O              |
| 38         | I/O              | I/O              | I/O              |
| 39         | I/O              | I/O              | I/O              |
| 40         | I/O              | I/O              | I/O              |
| 41         | NC               | I/O              | I/O              |
| 42         | NC               | I/O              | I/O              |

| Pin Number | A42MX16 Function | A42MX24 Function | A42MX36 Function |
|------------|------------------|------------------|------------------|
| 43         | NC               | I/O              | I/O              |
| 44         | I/O              | I/O              | I/O              |
| 45         | I/O              | I/O              | I/O              |
| 46         | I/O              | I/O              | I/O              |
| 47         | I/O              | I/O              | I/O              |
| 48         | I/O              | I/O              | I/O              |
| 49         | I/O              | I/O              | I/O              |
| 50         | NC               | I/O              | I/O              |
| 51         | NC               | I/O              | I/O              |
| 52         | GND              | GND              | GND              |
| 53         | GND              | GND              | GND              |
| 54         | I/O              | TMS, I/O         | TMS, I/O         |
| 55         | I/O              | TDI, I/O         | TDI, I/O         |
| 56         | I/O              | I/O              | I/O              |
| 57         | I/O              | I/O (WD)         | I/O (WD)         |
| 58         | I/O              | I/O (WD)         | I/O (WD)         |
| 59         | I/O              | I/O              | I/O              |
| 60         | V <sub>CCI</sub> | V <sub>CCI</sub> | V <sub>CCI</sub> |
| 61         | NC               | I/O              | I/O              |
| 62         | NC               | I/O              | I/O              |
| 63         | I/O              | I/O              | I/O              |
| 64         | I/O              | I/O              | I/O              |
| 65         | I/O              | I/O              | QCLKA, I/O       |
| 66         | I/O              | I/O (WD)         | I/O (WD)         |
| 67         | NC               | I/O (WD)         | I/O (WD)         |
| 68         | NC               | I/O              | I/O              |
| 69         | I/O              | I/O              | I/O              |
| 70         | I/O              | I/O (WD)         | I/O (WD)         |
| 71         | I/O              | I/O (WD)         | I/O (WD)         |
| 72         | I/O              | I/O              | I/O              |
| 73         | I/O              | I/O              | I/O              |
| 74         | I/O              | I/O              | I/O              |
| 75         | I/O              | I/O              | I/O              |
| 76         | I/O              | I/O              | I/O              |
| 77         | I/O              | I/O              | I/O              |
| 78         | GND              | GND              | GND              |
| 79         | V <sub>CCA</sub> | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 80         | NC               | V <sub>CCI</sub> | V <sub>CCI</sub> |
| 81         | I/O              | I/O              | I/O              |
| 82         | I/O              | I/O              | I/O              |
| 83         | I/O              | I/O              | I/O              |
| 84         | I/O              | I/O              | I/O              |

208-Pin PQFP (Continued)

| Pin Number | A42MX16 Function | A42MX24 Function | A42MX36 Function |
|------------|------------------|------------------|------------------|
| 85         | I/O              | I/O (WD)         | I/O (WD)         |
| 86         | I/O              | I/O (WD)         | I/O (WD)         |
| 87         | I/O              | I/O              | I/O              |
| 88         | I/O              | I/O              | I/O              |
| 89         | NC               | I/O              | I/O              |
| 90         | NC               | I/O              | I/O              |
| 91         | I/O              | I/O              | QCLKB, I/O       |
| 92         | I/O              | I/O              | I/O              |
| 93         | I/O              | I/O (WD)         | I/O (WD)         |
| 94         | I/O              | I/O (WD)         | I/O (WD)         |
| 95         | NC               | I/O              | I/O              |
| 96         | NC               | I/O              | I/O              |
| 97         | NC               | I/O              | I/O              |
| 98         | V <sub>CCI</sub> | V <sub>CCI</sub> | V <sub>CCI</sub> |
| 99         | I/O              | I/O              | I/O              |
| 100        | I/O              | I/O (WD)         | I/O (WD)         |
| 101        | I/O              | I/O (WD)         | I/O (WD)         |
| 102        | I/O              | I/O              | I/O              |
| 103        | SDO, I/O         | SDO, TDO, I/O    | SDO, TDO, I/O    |
| 104        | I/O              | I/O              | I/O              |
| 105        | GND              | GND              | GND              |
| 106        | NC               | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 107        | I/O              | I/O              | I/O              |
| 108        | I/O              | I/O              | I/O              |
| 109        | I/O              | I/O              | I/O              |
| 110        | I/O              | I/O              | I/O              |
| 111        | I/O              | I/O              | I/O              |
| 112        | NC               | I/O              | I/O              |
| 113        | NC               | I/O              | I/O              |
| 114        | NC               | I/O              | I/O              |
| 115        | NC               | I/O              | I/O              |
| 116        | I/O              | I/O              | I/O              |
| 117        | I/O              | I/O              | I/O              |
| 118        | I/O              | I/O              | I/O              |
| 119        | I/O              | I/O              | I/O              |
| 120        | I/O              | I/O              | I/O              |
| 121        | I/O              | I/O              | I/O              |
| 122        | I/O              | I/O              | I/O              |
| 123        | I/O              | I/O              | I/O              |
| 124        | I/O              | I/O              | I/O              |
| 125        | I/O              | I/O              | I/O              |
| 126        | GND              | GND              | GND              |

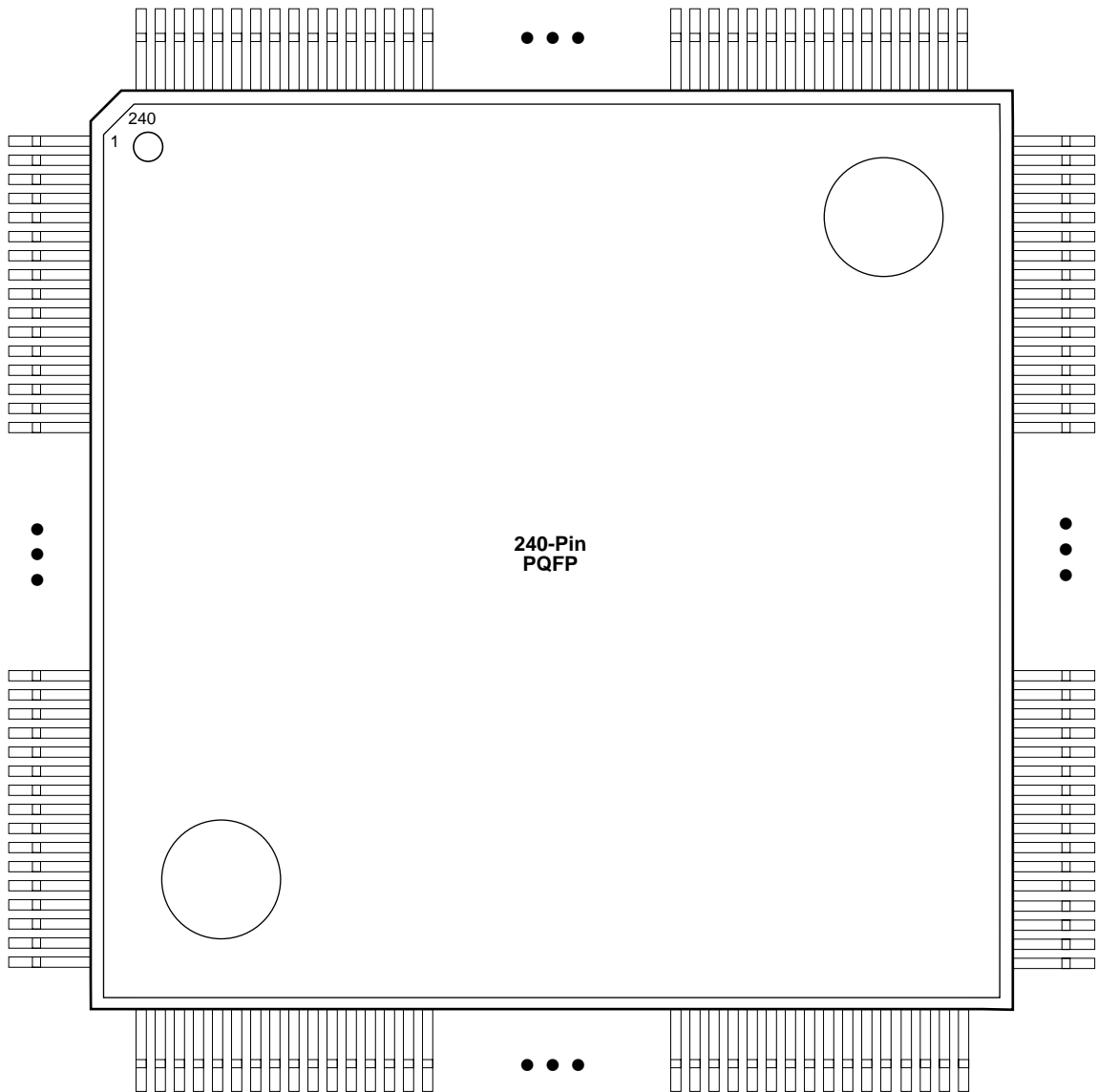
| Pin Number | A42MX16 Function | A42MX24 Function | A42MX36 Function |
|------------|------------------|------------------|------------------|
| 127        | I/O              | I/O              | I/O              |
| 128        | I/O              | TCK, I/O         | TCK, I/O         |
| 129        | GND (LP)         | GND (LP)         | GND (LP)         |
| 130        | V <sub>CCA</sub> | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 131        | GND              | GND              | GND              |
| 132        | V <sub>CCI</sub> | V <sub>CCI</sub> | V <sub>CCI</sub> |
| 133        | V <sub>CCA</sub> | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 134        | I/O              | I/O              | I/O              |
| 135        | I/O              | I/O              | I/O              |
| 136        | V <sub>CCA</sub> | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 137        | I/O              | I/O              | I/O              |
| 138        | I/O              | I/O              | I/O              |
| 139        | I/O              | I/O              | I/O              |
| 140        | I/O              | I/O              | I/O              |
| 141        | NC               | I/O              | I/O              |
| 142        | I/O              | I/O              | I/O              |
| 143        | I/O              | I/O              | I/O              |
| 144        | I/O              | I/O              | I/O              |
| 145        | I/O              | I/O              | I/O              |
| 146        | NC               | I/O              | I/O              |
| 147        | NC               | I/O              | I/O              |
| 148        | NC               | I/O              | I/O              |
| 149        | NC               | I/O              | I/O              |
| 150        | GND              | GND              | GND              |
| 151        | I/O              | I/O              | I/O              |
| 152        | I/O              | I/O              | I/O              |
| 153        | I/O              | I/O              | I/O              |
| 154        | I/O              | I/O              | I/O              |
| 155        | I/O              | I/O              | I/O              |
| 156        | I/O              | I/O              | I/O              |
| 157        | GND              | GND              | GND              |
| 158        | I/O              | I/O              | I/O              |
| 159        | SDI, I/O         | SDI, I/O         | SDI, I/O         |
| 160        | I/O              | I/O              | I/O              |
| 161        | I/O              | I/O (WD)         | I/O (WD)         |
| 162        | I/O              | I/O (WD)         | I/O (WD)         |
| 163        | I/O              | I/O              | I/O              |
| 164        | V <sub>CCI</sub> | V <sub>CCI</sub> | V <sub>CCI</sub> |
| 165        | NC               | I/O              | I/O              |
| 166        | NC               | I/O              | I/O              |
| 167        | I/O              | I/O              | I/O              |
| 168        | I/O              | I/O (WD)         | I/O (WD)         |

**208-Pin PQFP (Continued)**

| Pin Number | A42MX16 Function | A42MX24 Function | A42MX36 Function |
|------------|------------------|------------------|------------------|
| 169        | I/O              | I/O (WD)         | I/O (WD)         |
| 170        | I/O              | I/O              | I/O              |
| 171        | NC               | I/O              | QCLKD, I/O       |
| 172        | I/O              | I/O              | I/O              |
| 173        | I/O              | I/O              | I/O              |
| 174        | I/O              | I/O              | I/O              |
| 175        | I/O              | I/O              | I/O              |
| 176        | I/O              | I/O (WD)         | I/O (WD)         |
| 177        | I/O              | I/O (WD)         | I/O (WD)         |
| 178        | PRA, I/O         | PRA, I/O         | PRA, I/O         |
| 179        | I/O              | I/O              | I/O              |
| 180        | CLKA, I/O        | CLKA, I/O        | CLKA, I/O        |
| 181        | NC               | I/O              | I/O              |
| 182        | NC               | V <sub>CCI</sub> | V <sub>CCI</sub> |
| 183        | V <sub>CCA</sub> | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 184        | GND              | GND              | GND              |
| 185        | I/O              | I/O              | I/O              |
| 186        | CLKB, I/O        | CLKB, I/O        | CLKB, I/O        |
| 187        | I/O              | I/O              | I/O              |
| 188        | PRB, I/O         | PRB, I/O         | PRB, I/O         |

| Pin Number | A42MX16 Function | A42MX24 Function | A42MX36 Function |
|------------|------------------|------------------|------------------|
| 189        | I/O              | I/O              | I/O              |
| 190        | I/O              | I/O (WD)         | I/O (WD)         |
| 191        | I/O              | I/O (WD)         | I/O (WD)         |
| 192        | I/O              | I/O              | I/O              |
| 193        | NC               | I/O              | I/O              |
| 194        | NC               | I/O (WD)         | I/O (WD)         |
| 195        | NC               | I/O (WD)         | I/O (WD)         |
| 196        | I/O              | I/O              | QCLKC, I/O       |
| 197        | NC               | I/O              | I/O              |
| 198        | NC               | I/O              | I/O              |
| 199        | I/O              | I/O              | I/O              |
| 200        | I/O              | I/O              | I/O              |
| 201        | NC               | I/O              | I/O              |
| 202        | V <sub>CCI</sub> | V <sub>CCI</sub> | V <sub>CCI</sub> |
| 203        | I/O              | I/O (WD)         | I/O (WD)         |
| 204        | I/O              | I/O (WD)         | I/O (WD)         |
| 205        | I/O              | I/O              | I/O              |
| 206        | I/O              | I/O              | I/O              |
| 207        | DCLK, I/O        | DCLK, I/O        | DCLK, I/O        |
| 208        | I/O              | I/O              | I/O              |

**Package Pin Assignments (continued)**  
**240-Pin PQFP Package (Top View)**



**240-Pin PQFP**

| Pin Number | A42MX36 Function | Pin Number | A42MX36 Function | Pin Number | A42MX36 Function | Pin Number | A42MX36 Function |
|------------|------------------|------------|------------------|------------|------------------|------------|------------------|
| 1          | I/O              | 41         | I/O              | 81         | I/O              | 121        | GND              |
| 2          | DCLK, I/O        | 42         | I/O              | 82         | I/O              | 122        | I/O              |
| 3          | I/O              | 43         | I/O              | 83         | I/O              | 123        | SDO, TDO, I/O    |
| 4          | I/O              | 44         | I/O              | 84         | I/O              | 124        | I/O              |
| 5          | I/O              | 45         | QCLKD, I/O       | 85         | V <sub>CCA</sub> | 125        | I/O (WD)         |
| 6          | I/O (WD)         | 46         | I/O              | 86         | I/O              | 126        | I/O (WD)         |
| 7          | I/O (WD)         | 47         | I/O (WD)         | 87         | I/O              | 127        | I/O              |
| 8          | V <sub>CCI</sub> | 48         | I/O (WD)         | 88         | V <sub>CCA</sub> | 128        | V <sub>CCI</sub> |
| 9          | I/O              | 49         | I/O              | 89         | V <sub>CCI</sub> | 129        | I/O              |
| 10         | I/O              | 50         | I/O              | 90         | V <sub>CCA</sub> | 130        | I/O              |
| 11         | I/O              | 51         | I/O              | 91         | GND (LP)         | 131        | I/O              |
| 12         | I/O              | 52         | V <sub>CCI</sub> | 92         | TCK, I/O         | 132        | I/O (WD)         |
| 13         | I/O              | 53         | I/O              | 93         | I/O              | 133        | I/O (WD)         |
| 14         | I/O              | 54         | I/O (WD)         | 94         | GND              | 134        | I/O              |
| 15         | QCLKC, I/O       | 55         | I/O (WD)         | 95         | I/O              | 135        | QCLKB, I/O       |
| 16         | I/O              | 56         | I/O              | 96         | I/O              | 136        | I/O              |
| 17         | I/O (WD)         | 57         | SDI, I/O         | 97         | I/O              | 137        | I/O              |
| 18         | I/O (WD)         | 58         | I/O              | 98         | I/O              | 138        | I/O              |
| 19         | I/O              | 59         | V <sub>CCA</sub> | 99         | I/O              | 139        | I/O              |
| 20         | I/O              | 60         | GND              | 100        | I/O              | 140        | I/O              |
| 21         | I/O (WD)         | 61         | GND              | 101        | I/O              | 141        | I/O              |
| 22         | I/O (WD)         | 62         | I/O              | 102        | I/O              | 142        | I/O (WD)         |
| 23         | I/O              | 63         | I/O              | 103        | I/O              | 143        | I/O (WD)         |
| 24         | PRB, I/O         | 64         | I/O              | 104        | I/O              | 144        | I/O              |
| 25         | I/O              | 65         | I/O              | 105        | I/O              | 145        | I/O              |
| 26         | CLKB, I/O        | 66         | I/O              | 106        | I/O              | 146        | I/O              |
| 27         | I/O              | 67         | I/O              | 107        | I/O              | 147        | I/O              |
| 28         | GND              | 68         | I/O              | 108        | V <sub>CCI</sub> | 148        | I/O              |
| 29         | V <sub>CCA</sub> | 69         | I/O              | 109        | I/O              | 149        | I/O              |
| 30         | V <sub>CCI</sub> | 70         | I/O              | 110        | I/O              | 150        | V <sub>CCI</sub> |
| 31         | I/O              | 71         | V <sub>CCI</sub> | 111        | I/O              | 151        | V <sub>CCA</sub> |
| 32         | CLKA, I/O        | 72         | I/O              | 112        | I/O              | 152        | GND              |
| 33         | I/O              | 73         | I/O              | 113        | I/O              | 153        | I/O              |
| 34         | PRA, I/O         | 74         | I/O              | 114        | I/O              | 154        | I/O              |
| 35         | I/O              | 75         | I/O              | 115        | I/O              | 155        | I/O              |
| 36         | I/O              | 76         | I/O              | 116        | I/O              | 156        | I/O              |
| 37         | I/O (WD)         | 77         | I/O              | 117        | I/O              | 157        | I/O              |
| 38         | I/O (WD)         | 78         | I/O              | 118        | V <sub>CCA</sub> | 158        | I/O              |
| 39         | I/O              | 79         | I/O              | 119        | GND              | 159        | I/O (WD)         |
| 40         | I/O              | 80         | I/O              | 120        | GND              | 160        | I/O (WD)         |

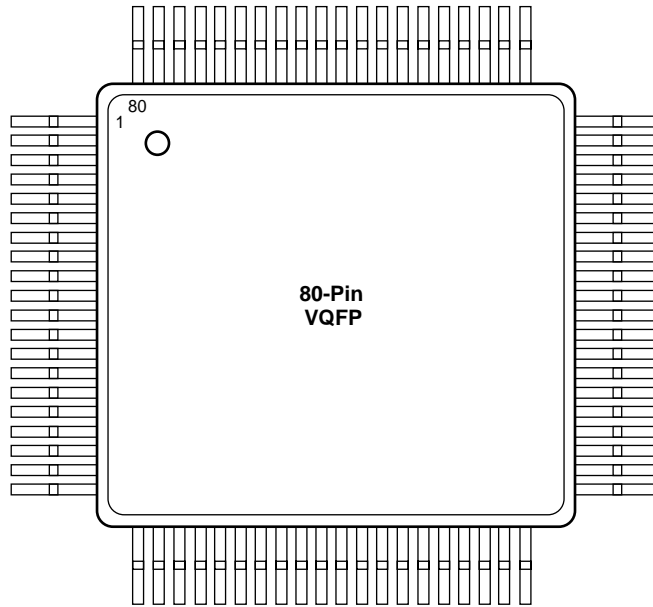


240-Pin PQFP (Continued)

| Pin Number | A42MX36 Function | Pin Number | A42MX36 Function | Pin Number | A42MX36 Function | Pin Number | A42MX36 Function |
|------------|------------------|------------|------------------|------------|------------------|------------|------------------|
| 161        | I/O              | 181        | V <sub>CCA</sub> | 201        | I/O              | 221        | I/O              |
| 162        | I/O              | 182        | GND              | 202        | I/O              | 222        | I/O              |
| 163        | I/O (WD)         | 183        | I/O              | 203        | I/O              | 223        | I/O              |
| 164        | I/O (WD)         | 184        | I/O              | 204        | I/O              | 224        | I/O              |
| 165        | I/O              | 185        | I/O              | 205        | I/O              | 225        | I/O              |
| 166        | QCLKA, I/O       | 186        | I/O              | 206        | V <sub>CCA</sub> | 226        | I/O              |
| 167        | I/O              | 187        | I/O              | 207        | I/O              | 227        | V <sub>CCI</sub> |
| 168        | I/O              | 188        | I/O              | 208        | I/O              | 228        | I/O              |
| 169        | I/O              | 189        | I/O              | 209        | V <sub>CCA</sub> | 229        | I/O              |
| 170        | I/O              | 190        | I/O              | 210        | V <sub>CCI</sub> | 230        | I/O              |
| 171        | I/O              | 191        | I/O              | 211        | I/O              | 231        | I/O              |
| 172        | V <sub>CCI</sub> | 192        | V <sub>CCI</sub> | 212        | I/O              | 232        | I/O              |
| 173        | I/O              | 193        | I/O              | 213        | I/O              | 233        | I/O              |
| 174        | I/O (WD)         | 194        | I/O              | 214        | I/O              | 234        | I/O              |
| 175        | I/O (WD)         | 195        | I/O              | 215        | I/O              | 235        | I/O              |
| 176        | I/O              | 196        | I/O              | 216        | I/O              | 236        | I/O              |
| 177        | I/O              | 197        | I/O              | 217        | I/O              | 237        | GND              |
| 178        | TDI, I/O         | 198        | I/O              | 218        | I/O              | 238        | MODE             |
| 179        | TMS, I/O         | 199        | I/O              | 219        | V <sub>CCA</sub> | 239        | V <sub>CCA</sub> |
| 180        | GND              | 200        | I/O              | 220        | I/O              | 240        | GND              |

**Package Pin Assignments (continued)**

**80-Pin VQFP**



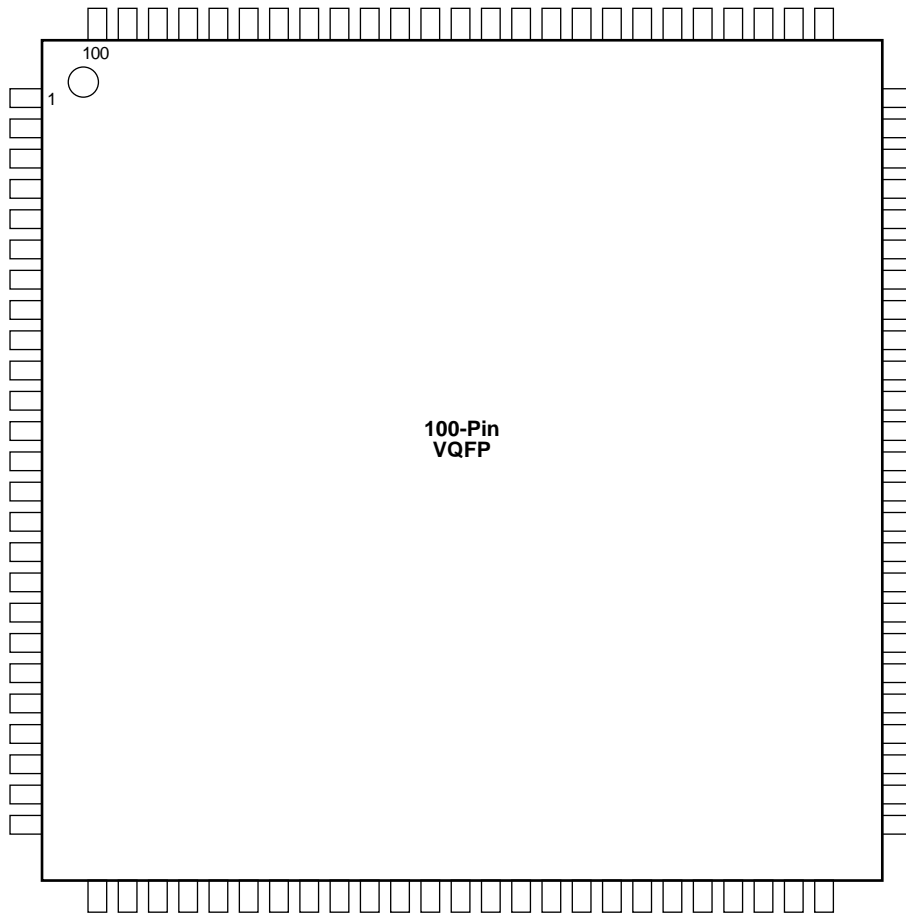
80-Pin VQFP

| Pin Number | A40MX02 Function | A40MX04 Function |
|------------|------------------|------------------|
| 1          | I/O              | I/O              |
| 2          | NC               | I/O              |
| 3          | NC               | I/O              |
| 4          | NC               | I/O              |
| 5          | I/O              | I/O              |
| 6          | I/O              | I/O              |
| 7          | GND              | GND              |
| 8          | I/O              | I/O              |
| 9          | I/O              | I/O              |
| 10         | I/O              | I/O              |
| 11         | I/O              | I/O              |
| 12         | I/O              | I/O              |
| 13         | V <sub>CC</sub>  | V <sub>CC</sub>  |
| 14         | I/O              | I/O              |
| 15         | I/O              | I/O              |
| 16         | I/O              | I/O              |
| 17         | NC               | I/O              |
| 18         | NC               | I/O              |
| 19         | NC               | I/O              |
| 20         | V <sub>CC</sub>  | V <sub>CC</sub>  |
| 21         | I/O              | I/O              |
| 22         | I/O              | I/O              |
| 23         | I/O              | I/O              |
| 24         | I/O              | I/O              |
| 25         | I/O              | I/O              |
| 26         | I/O              | I/O              |
| 27         | GND              | GND              |
| 28         | I/O              | I/O              |
| 29         | I/O              | I/O              |
| 30         | I/O              | I/O              |
| 31         | I/O              | I/O              |
| 32         | I/O              | I/O              |
| 33         | V <sub>CC</sub>  | V <sub>CC</sub>  |
| 34         | I/O              | I/O              |
| 35         | I/O              | I/O              |
| 36         | I/O              | I/O              |
| 37         | I/O              | I/O              |
| 38         | I/O              | I/O              |
| 39         | I/O              | I/O              |
| 40         | I/O              | I/O              |

| Pin Number | A40MX02 Function | A40MX04 Function |
|------------|------------------|------------------|
| 41         | NC               | I/O              |
| 42         | NC               | I/O              |
| 43         | NC               | I/O              |
| 44         | I/O              | I/O              |
| 45         | I/O              | I/O              |
| 46         | I/O              | I/O              |
| 47         | GND              | GND              |
| 48         | I/O              | I/O              |
| 49         | I/O              | I/O              |
| 50         | CLK, I/O         | CLK, I/O         |
| 51         | I/O              | I/O              |
| 52         | MODE             | MODE             |
| 53         | V <sub>CC</sub>  | V <sub>CC</sub>  |
| 54         | NC               | I/O              |
| 55         | NC               | I/O              |
| 56         | NC               | I/O              |
| 57         | SDI, I/O         | SDI, I/O         |
| 58         | DCLK, I/O        | DCLK, I/O        |
| 59         | PRA, I/O         | PRA, I/O         |
| 60         | NC               | NC               |
| 61         | PRB, I/O         | PRB, I/O         |
| 62         | I/O              | I/O              |
| 63         | I/O              | I/O              |
| 64         | I/O              | I/O              |
| 65         | I/O              | I/O              |
| 66         | I/O              | I/O              |
| 67         | I/O              | I/O              |
| 68         | GND              | GND              |
| 69         | I/O              | I/O              |
| 70         | I/O              | I/O              |
| 71         | I/O              | I/O              |
| 72         | I/O              | I/O              |
| 73         | I/O              | I/O              |
| 74         | V <sub>CC</sub>  | V <sub>CC</sub>  |
| 75         | I/O              | I/O              |
| 76         | I/O              | I/O              |
| 77         | I/O              | I/O              |
| 78         | I/O              | I/O              |
| 79         | I/O              | I/O              |
| 80         | I/O              | I/O              |

**Package Pin Assignments (continued)**

**100-Pin VQFP Package (Top View)**



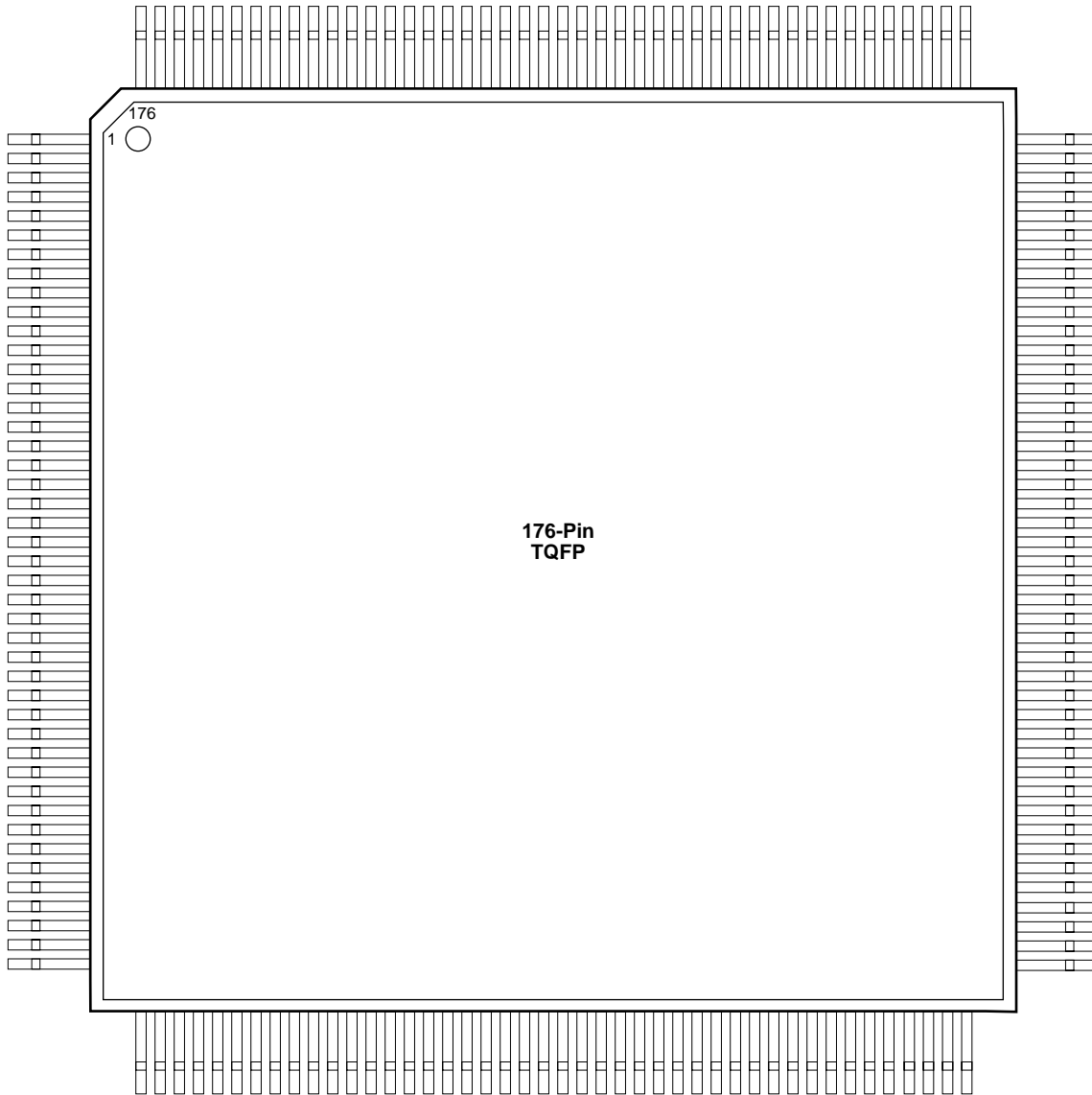
100-Pin VQFP Package

| Pin Number | A42MX09 Function | A42MX16 Function |
|------------|------------------|------------------|
| 1          | I/O              | I/O              |
| 2          | MODE             | MODE             |
| 3          | I/O              | I/O              |
| 4          | I/O              | I/O              |
| 5          | I/O              | I/O              |
| 6          | I/O              | I/O              |
| 7          | GND              | GND              |
| 8          | I/O              | I/O              |
| 9          | I/O              | I/O              |
| 10         | I/O              | I/O              |
| 11         | I/O              | I/O              |
| 12         | I/O              | I/O              |
| 13         | I/O              | I/O              |
| 14         | V <sub>CCA</sub> | NC               |
| 15         | V <sub>CCI</sub> | V <sub>CCI</sub> |
| 16         | I/O              | I/O              |
| 17         | I/O              | I/O              |
| 18         | I/O              | I/O              |
| 19         | I/O              | I/O              |
| 20         | GND              | GND              |
| 21         | I/O              | I/O              |
| 22         | I/O              | I/O              |
| 23         | I/O              | I/O              |
| 24         | I/O              | I/O              |
| 25         | I/O              | I/O              |
| 26         | I/O              | I/O              |
| 27         | I/O              | I/O              |
| 28         | I/O              | I/O              |
| 29         | I/O              | I/O              |
| 30         | I/O              | I/O              |
| 31         | I/O              | I/O              |
| 32         | GND              | GND              |
| 33         | I/O              | I/O              |
| 34         | I/O              | I/O              |
| 35         | I/O              | I/O              |
| 36         | I/O              | I/O              |
| 37         | I/O              | I/O              |
| 38         | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 39         | I/O              | I/O              |
| 40         | I/O              | I/O              |
| 41         | I/O              | I/O              |
| 42         | I/O              | I/O              |
| 43         | I/O              | I/O              |
| 44         | GND              | GND              |
| 45         | I/O              | I/O              |
| 46         | I/O              | I/O              |
| 47         | I/O              | I/O              |
| 48         | I/O              | I/O              |
| 49         | I/O              | I/O              |
| 50         | SDO, I/O         | SDO, I/O         |

| Pin Number | A42MX09 Function | A42MX16 Function |
|------------|------------------|------------------|
| 51         | I/O              | I/O              |
| 52         | I/O              | I/O              |
| 53         | I/O              | I/O              |
| 54         | I/O              | I/O              |
| 55         | GND              | GND              |
| 56         | I/O              | I/O              |
| 57         | I/O              | I/O              |
| 58         | I/O              | I/O              |
| 59         | I/O              | I/O              |
| 60         | I/O              | I/O              |
| 61         | I/O              | I/O              |
| 62         | GND (LP)         | GND (LP)         |
| 63         | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 64         | V <sub>CCI</sub> | V <sub>CCI</sub> |
| 65         | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 66         | I/O              | I/O              |
| 67         | I/O              | I/O              |
| 68         | I/O              | I/O              |
| 69         | I/O              | I/O              |
| 70         | GND              | GND              |
| 71         | I/O              | I/O              |
| 72         | I/O              | I/O              |
| 73         | I/O              | I/O              |
| 74         | I/O              | I/O              |
| 75         | I/O              | I/O              |
| 76         | I/O              | I/O              |
| 77         | SDI, I/O         | SDI, I/O         |
| 78         | I/O              | I/O              |
| 79         | I/O              | I/O              |
| 80         | I/O              | I/O              |
| 81         | I/O              | I/O              |
| 82         | GND              | GND              |
| 83         | I/O              | I/O              |
| 84         | I/O              | I/O              |
| 85         | PRA, I/O         | PRA, I/O         |
| 86         | I/O              | I/O              |
| 87         | CLKA, I/O        | CLKA, I/O        |
| 88         | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 89         | I/O              | I/O              |
| 90         | CLKB, I/O        | CLKB, I/O        |
| 91         | I/O              | I/O              |
| 92         | PRB, I/O         | PRB, I/O         |
| 93         | I/O              | I/O              |
| 94         | GND              | GND              |
| 95         | I/O              | I/O              |
| 96         | I/O              | I/O              |
| 97         | I/O              | I/O              |
| 98         | I/O              | I/O              |
| 99         | I/O              | I/O              |
| 100        | DCLK, I/O        | DCLK, I/O        |

**Package Pin Assignments (continued)**

**176-Pin TQFP Package (Top View)**



176-Pin TQFP

| Pin Number | A42MX09 Function | A42MX16 Function | A42MX24 Function |
|------------|------------------|------------------|------------------|
| 1          | GND              | GND              | GND              |
| 2          | MODE             | MODE             | MODE             |
| 3          | I/O              | I/O              | I/O              |
| 4          | I/O              | I/O              | I/O              |
| 5          | I/O              | I/O              | I/O              |
| 6          | I/O              | I/O              | I/O              |
| 7          | I/O              | I/O              | I/O              |
| 8          | NC               | NC               | I/O              |
| 9          | I/O              | I/O              | I/O              |
| 10         | NC               | I/O              | I/O              |
| 11         | NC               | I/O              | I/O              |
| 12         | I/O              | I/O              | I/O              |
| 13         | NC               | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 14         | I/O              | I/O              | I/O              |
| 15         | I/O              | I/O              | I/O              |
| 16         | I/O              | I/O              | I/O              |
| 17         | I/O              | I/O              | I/O              |
| 18         | GND              | GND              | GND              |
| 19         | NC               | I/O              | I/O              |
| 20         | NC               | I/O              | I/O              |
| 21         | I/O              | I/O              | I/O              |
| 22         | NC               | I/O              | I/O              |
| 23         | GND              | GND              | GND              |
| 24         | NC               | V <sub>CCI</sub> | V <sub>CCI</sub> |
| 25         | V <sub>CCA</sub> | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 26         | NC               | I/O              | I/O              |
| 27         | NC               | I/O              | I/O              |
| 28         | V <sub>CCI</sub> | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 29         | NC               | I/O              | I/O              |
| 30         | I/O              | I/O              | I/O              |
| 31         | I/O              | I/O              | I/O              |
| 32         | I/O              | I/O              | I/O              |
| 33         | NC               | NC               | I/O              |
| 34         | I/O              | I/O              | I/O              |
| 35         | I/O              | I/O              | I/O              |
| 36         | I/O              | I/O              | I/O              |
| 37         | NC               | I/O              | I/O              |
| 38         | NC               | NC               | I/O              |
| 39         | I/O              | I/O              | I/O              |
| 40         | I/O              | I/O              | I/O              |
| 41         | I/O              | I/O              | I/O              |
| 42         | I/O              | I/O              | I/O              |
| 43         | I/O              | I/O              | I/O              |
| 44         | I/O              | I/O              | I/O              |

| Pin Number | A42MX09 Function | A42MX16 Function | A42MX24 Function |
|------------|------------------|------------------|------------------|
| 45         | GND              | GND              | GND              |
| 46         | I/O              | I/O              | TMS, I/O         |
| 47         | I/O              | I/O              | TDI, I/O         |
| 48         | I/O              | I/O              | I/O              |
| 49         | I/O              | I/O              | I/O (WD)         |
| 50         | I/O              | I/O              | I/O (WD)         |
| 51         | I/O              | I/O              | I/O              |
| 52         | NC               | V <sub>CCI</sub> | V <sub>CCI</sub> |
| 53         | I/O              | I/O              | I/O              |
| 54         | NC               | I/O              | I/O              |
| 55         | NC               | I/O              | I/O (WD)         |
| 56         | I/O              | I/O              | I/O (WD)         |
| 57         | NC               | NC               | I/O              |
| 58         | I/O              | I/O              | I/O              |
| 59         | I/O              | I/O              | I/O (WD)         |
| 60         | I/O              | I/O              | I/O (WD)         |
| 61         | NC               | I/O              | I/O              |
| 62         | I/O              | I/O              | I/O              |
| 63         | I/O              | I/O              | I/O              |
| 64         | NC               | I/O              | I/O              |
| 65         | I/O              | I/O              | I/O              |
| 66         | NC               | I/O              | I/O              |
| 67         | GND              | GND              | GND              |
| 68         | V <sub>CCA</sub> | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 69         | I/O              | I/O              | I/O (WD)         |
| 70         | I/O              | I/O              | I/O (WD)         |
| 71         | I/O              | I/O              | I/O              |
| 72         | I/O              | I/O              | I/O              |
| 73         | I/O              | I/O              | I/O              |
| 74         | NC               | I/O              | I/O              |
| 75         | I/O              | I/O              | I/O              |
| 76         | I/O              | I/O              | I/O              |
| 77         | NC               | NC               | I/O (WD)         |
| 78         | NC               | I/O              | I/O (WD)         |
| 79         | I/O              | I/O              | I/O              |
| 80         | NC               | I/O              | I/O              |
| 81         | I/O              | I/O              | I/O              |
| 82         | NC               | V <sub>CCI</sub> | V <sub>CCI</sub> |
| 83         | I/O              | I/O              | I/O              |
| 84         | I/O              | I/O              | I/O (WD)         |
| 85         | I/O              | I/O              | I/O (WD)         |
| 86         | NC               | I/O              | I/O              |
| 87         | SDO, I/O         | SDO, I/O         | SDO, TDO, I/O    |
| 88         | I/O              | I/O              | I/O              |

**176-Pin TQFP (Continued)**

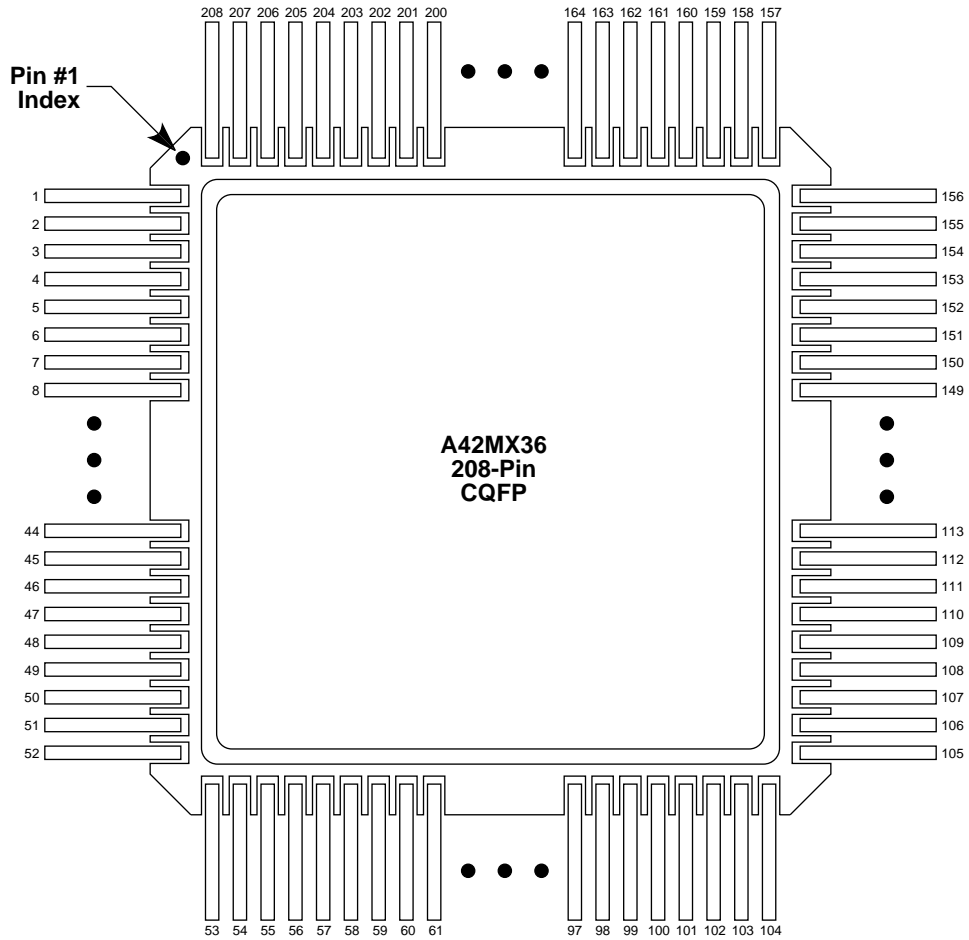
| Pin Number | A42MX09 Function | A42MX16 Function | A42MX24 Function |
|------------|------------------|------------------|------------------|
| 89         | GND              | GND              | GND              |
| 90         | I/O              | I/O              | I/O              |
| 91         | I/O              | I/O              | I/O              |
| 92         | I/O              | I/O              | I/O              |
| 93         | I/O              | I/O              | I/O              |
| 94         | I/O              | I/O              | I/O              |
| 95         | I/O              | I/O              | I/O              |
| 96         | NC               | I/O              | I/O              |
| 97         | NC               | I/O              | I/O              |
| 98         | I/O              | I/O              | I/O              |
| 99         | I/O              | I/O              | I/O              |
| 100        | I/O              | I/O              | I/O              |
| 101        | NC               | NC               | I/O              |
| 102        | I/O              | I/O              | I/O              |
| 103        | NC               | I/O              | I/O              |
| 104        | I/O              | I/O              | I/O              |
| 105        | I/O              | I/O              | I/O              |
| 106        | GND              | GND              | GND              |
| 107        | NC               | I/O              | I/O              |
| 108        | NC               | I/O              | TCK, I/O         |
| 109        | GND (LP)         | GND (LP)         | GND (LP)         |
| 110        | V <sub>CCA</sub> | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 111        | GND              | GND              | GND              |
| 112        | V <sub>CCI</sub> | V <sub>CCI</sub> | V <sub>CCI</sub> |
| 113        | V <sub>CCA</sub> | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 114        | NC               | I/O              | I/O              |
| 115        | NC               | I/O              | I/O              |
| 116        | NC               | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 117        | I/O              | I/O              | I/O              |
| 118        | I/O              | I/O              | I/O              |
| 119        | I/O              | I/O              | I/O              |
| 120        | I/O              | I/O              | I/O              |
| 121        | NC               | NC               | I/O              |
| 122        | I/O              | I/O              | I/O              |
| 123        | I/O              | I/O              | I/O              |
| 124        | NC               | I/O              | I/O              |
| 125        | NC               | I/O              | I/O              |
| 126        | NC               | NC               | I/O              |
| 127        | I/O              | I/O              | I/O              |
| 128        | I/O              | I/O              | I/O              |
| 129        | I/O              | I/O              | I/O              |
| 130        | I/O              | I/O              | I/O              |
| 131        | I/O              | I/O              | I/O              |
| 132        | I/O              | I/O              | I/O              |

| Pin Number | A42MX09 Function | A42MX16 Function | A42MX24 Function |
|------------|------------------|------------------|------------------|
| 133        | GND              | GND              | GND              |
| 134        | I/O              | I/O              | I/O              |
| 135        | SDI, I/O         | SDI, I/O         | SDI, I/O         |
| 136        | NC               | I/O              | I/O              |
| 137        | I/O              | I/O              | I/O (WD)         |
| 138        | I/O              | I/O              | I/O (WD)         |
| 139        | I/O              | I/O              | I/O              |
| 140        | NC               | V <sub>CCI</sub> | V <sub>CCI</sub> |
| 141        | I/O              | I/O              | I/O              |
| 142        | I/O              | I/O              | I/O              |
| 143        | NC               | I/O              | I/O              |
| 144        | NC               | I/O              | I/O (WD)         |
| 145        | NC               | NC               | I/O (WD)         |
| 146        | I/O              | I/O              | I/O              |
| 147        | NC               | I/O              | I/O              |
| 148        | I/O              | I/O              | I/O              |
| 149        | I/O              | I/O              | I/O              |
| 150        | I/O              | I/O              | I/O (WD)         |
| 151        | NC               | I/O              | I/O (WD)         |
| 152        | PRA, I/O         | PRA, I/O         | PRA, I/O         |
| 153        | I/O              | I/O              | I/O              |
| 154        | CLKA, I/O        | CLKA, I/O        | CLKA, I/O        |
| 155        | V <sub>CCA</sub> | V <sub>CCA</sub> | V <sub>CCA</sub> |
| 156        | GND              | GND              | GND              |
| 157        | I/O              | I/O              | I/O              |
| 158        | CLKB, I/O        | CLKB, I/O        | CLKB, I/O        |
| 159        | I/O              | I/O              | I/O              |
| 160        | PRB, I/O         | PRB, I/O         | PRB, I/O         |
| 161        | NC               | I/O              | I/O (WD)         |
| 162        | I/O              | I/O              | I/O (WD)         |
| 163        | I/O              | I/O              | I/O              |
| 164        | I/O              | I/O              | I/O              |
| 165        | NC               | NC               | I/O (WD)         |
| 166        | NC               | I/O              | I/O (WD)         |
| 167        | I/O              | I/O              | I/O              |
| 168        | NC               | I/O              | I/O              |
| 169        | I/O              | I/O              | I/O              |
| 170        | NC               | V <sub>CCI</sub> | V <sub>CCI</sub> |
| 171        | I/O              | I/O              | I/O (WD)         |
| 172        | I/O              | I/O              | I/O (WD)         |
| 173        | NC               | I/O              | I/O              |
| 174        | I/O              | I/O              | I/O              |
| 175        | DCLK, I/O        | DCLK, I/O        | DCLK, I/O        |
| 176        | I/O              | I/O              | I/O              |



## Package Pin Assignments

### 208-Pin CQFP (Top View)



**208-Pin CQFP**

| Pin Number | A42MX36 Function | Pin Number | A42MX36 Function | Pin Number | A42MX36 Function | Pin Number | A42MX36 Function |
|------------|------------------|------------|------------------|------------|------------------|------------|------------------|
| 1          | GND              | 40         | I/O              | 79         | V <sub>CCA</sub> | 118        | I/O              |
| 2          | V <sub>CCA</sub> | 41         | I/O              | 80         | V <sub>CCI</sub> | 119        | I/O              |
| 3          | MODE             | 42         | I/O              | 81         | I/O              | 120        | I/O              |
| 4          | I/O              | 43         | I/O              | 82         | I/O              | 121        | I/O              |
| 5          | I/O              | 44         | I/O              | 83         | I/O              | 122        | I/O              |
| 6          | I/O              | 45         | I/O              | 84         | I/O              | 123        | I/O              |
| 7          | I/O              | 46         | I/O              | 85         | I/O (WD)         | 124        | I/O              |
| 8          | I/O              | 47         | I/O              | 86         | I/O (WD)         | 125        | I/O              |
| 9          | I/O              | 48         | I/O              | 87         | I/O              | 126        | GND              |
| 10         | I/O              | 49         | I/O              | 88         | I/O              | 127        | I/O              |
| 11         | I/O              | 50         | I/O              | 89         | I/O              | 128        | TCK, I/O         |
| 12         | I/O              | 51         | I/O              | 90         | I/O              | 129        | GND (LP)         |
| 13         | I/O              | 52         | GND              | 91         | QCLKB, I/O       | 130        | V <sub>CCA</sub> |
| 14         | I/O              | 53         | GND              | 92         | I/O              | 131        | GND              |
| 15         | I/O              | 54         | TMS, I/O         | 93         | I/O (WD)         | 132        | V <sub>CCI</sub> |
| 16         | I/O              | 55         | TDI, I/O         | 94         | I/O (WD)         | 133        | V <sub>CCA</sub> |
| 17         | V <sub>CCA</sub> | 56         | I/O              | 95         | I/O              | 134        | I/O              |
| 18         | I/O              | 57         | I/O (WD)         | 96         | I/O              | 135        | I/O              |
| 19         | I/O              | 58         | I/O (WD)         | 97         | I/O              | 136        | V <sub>CCA</sub> |
| 20         | I/O              | 59         | I/O              | 98         | V <sub>CCI</sub> | 137        | I/O              |
| 21         | I/O              | 60         | V <sub>CCI</sub> | 99         | I/O              | 138        | I/O              |
| 22         | GND              | 61         | I/O              | 100        | I/O (WD)         | 139        | I/O              |
| 23         | I/O              | 62         | I/O              | 101        | I/O (WD)         | 140        | I/O              |
| 24         | I/O              | 63         | I/O              | 102        | I/O              | 141        | I/O              |
| 25         | I/O              | 64         | I/O              | 103        | TDO, I/O         | 142        | I/O              |
| 26         | I/O              | 65         | QCLKA, I/O       | 104        | I/O              | 143        | I/O              |
| 27         | GND              | 66         | I/O (WD)         | 105        | GND              | 144        | I/O              |
| 28         | V <sub>CCI</sub> | 67         | I/O (WD)         | 106        | V <sub>CCA</sub> | 145        | I/O              |
| 29         | V <sub>CCA</sub> | 68         | I/O              | 107        | I/O              | 146        | I/O              |
| 30         | I/O              | 69         | I/O              | 108        | I/O              | 147        | I/O              |
| 31         | I/O              | 70         | I/O (WD)         | 109        | I/O              | 148        | I/O              |
| 32         | V <sub>CCA</sub> | 71         | I/O (WD)         | 110        | I/O              | 149        | I/O              |
| 33         | I/O              | 72         | I/O              | 111        | I/O              | 150        | GND              |
| 34         | I/O              | 73         | I/O              | 112        | I/O              | 151        | I/O              |
| 35         | I/O              | 74         | I/O              | 113        | I/O              | 152        | I/O              |
| 36         | I/O              | 75         | I/O              | 114        | I/O              | 153        | I/O              |
| 37         | I/O              | 76         | I/O              | 115        | I/O              | 154        | I/O              |
| 38         | I/O              | 77         | I/O              | 116        | I/O              | 155        | I/O              |
| 39         | I/O              | 78         | GND              | 117        | I/O              | 156        | I/O              |

208-Pin CQFP (Continued)

| Pin Number | A42MX36 Function |
|------------|------------------|
| 157        | GND              |
| 158        | I/O              |
| 159        | SDI, I/O         |
| 160        | I/O              |
| 161        | I/O (WD)         |
| 162        | I/O (WD)         |
| 163        | I/O              |
| 164        | V <sub>CCI</sub> |
| 165        | I/O              |
| 166        | I/O              |
| 167        | I/O              |
| 168        | I/O (WD)         |
| 169        | I/O (WD)         |

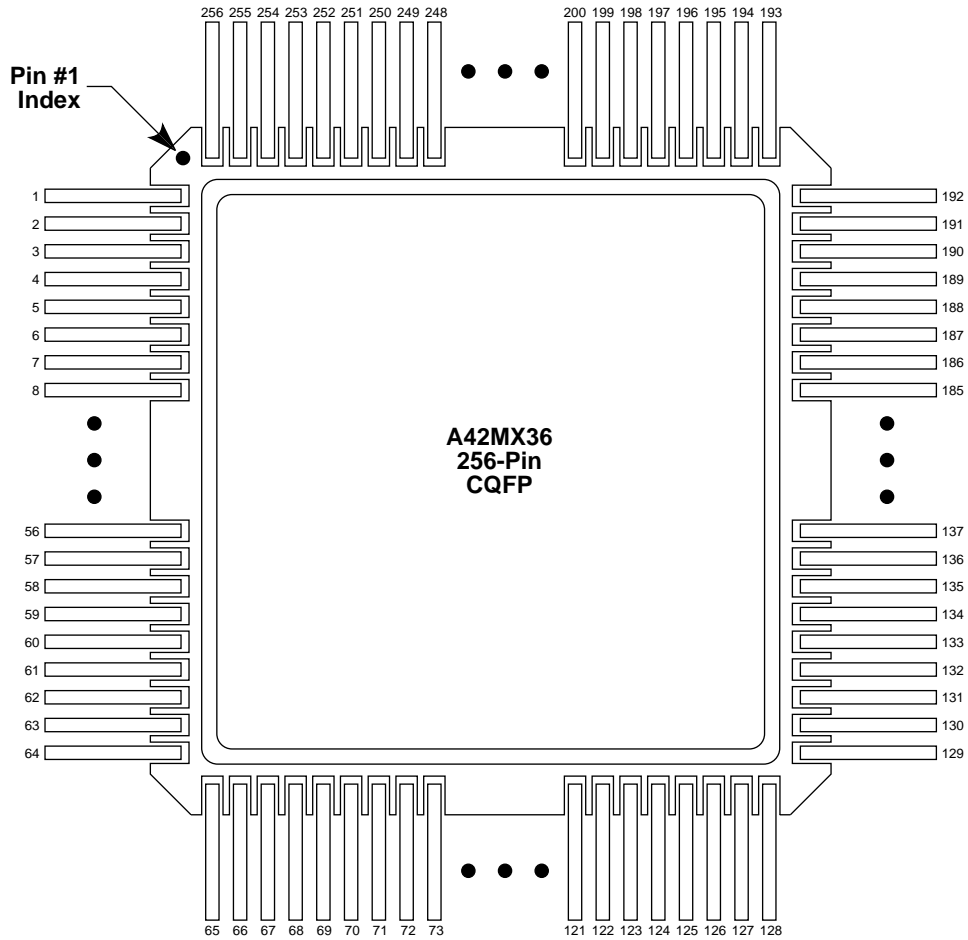
| Pin Number | A42MX36 Function |
|------------|------------------|
| 170        | I/O              |
| 171        | QCLKD, I/O       |
| 172        | I/O              |
| 173        | I/O              |
| 174        | I/O              |
| 175        | I/O              |
| 176        | I/O (WD)         |
| 177        | I/O (WD)         |
| 178        | PRA, I/O         |
| 179        | I/O              |
| 180        | CLKA, I/O        |
| 181        | I/O              |
| 182        | V <sub>CCI</sub> |

| Pin Number | A42MX36 Function |
|------------|------------------|
| 183        | V <sub>CCA</sub> |
| 184        | GND              |
| 185        | I/O              |
| 186        | CLKB, I/O        |
| 187        | I/O              |
| 188        | PRB, I/O         |
| 189        | I/O              |
| 190        | I/O (WD)         |
| 191        | I/O (WD)         |
| 192        | I/O              |
| 193        | I/O              |
| 194        | I/O (WD)         |
| 195        | I/O (WD)         |

| Pin Number | A42MX36 Function |
|------------|------------------|
| 196        | QCLKC, I/O       |
| 197        | I/O              |
| 198        | I/O              |
| 199        | I/O              |
| 200        | I/O              |
| 201        | I/O              |
| 202        | V <sub>CCI</sub> |
| 203        | I/O (WD)         |
| 204        | I/O (WD)         |
| 205        | I/O              |
| 206        | I/O              |
| 207        | DCLK, I/O        |
| 208        | I/O              |

### Package Pin Assignments (continued)

#### 256-Pin CQFP (Top View)



256-Pin CQFP

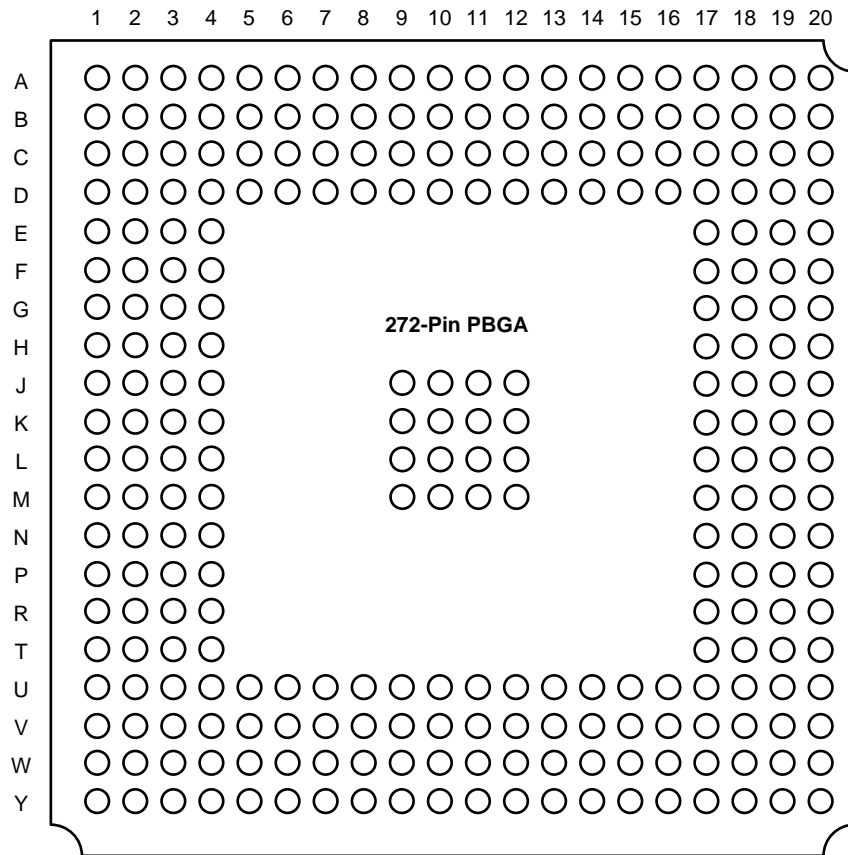
| Pin Number | A42MX36 Function | Pin Number | A42MX36 Function | Pin Number | A42MX36 Function | Pin Number | A42MX36 Function |
|------------|------------------|------------|------------------|------------|------------------|------------|------------------|
| 1          | NC               | 44         | I/O              | 87         | I/O, (WD)        | 130        | NC               |
| 2          | GND              | 45         | I/O              | 88         | I/O, (WD)        | 131        | GND              |
| 3          | I/O              | 46         | I/O              | 89         | I/O              | 132        | I/O              |
| 4          | I/O              | 47         | I/O              | 90         | I/O              | 133        | I/O              |
| 5          | I/O              | 48         | GND              | 91         | I/O              | 134        | I/O              |
| 6          | I/O              | 49         | I/O              | 92         | I/O              | 135        | I/O              |
| 7          | I/O              | 50         | I/O              | 93         | I/O              | 136        | I/O              |
| 8          | I/O              | 51         | I/O              | 94         | I/O              | 137        | I/O              |
| 9          | I/O              | 52         | I/O              | 95         | V <sub>CCI</sub> | 138        | I/O              |
| 10         | GND              | 53         | I/O              | 96         | V <sub>CCA</sub> | 139        | GND              |
| 11         | I/O              | 54         | I/O              | 97         | GND              | 140        | I/O              |
| 12         | I/O              | 55         | I/O              | 98         | GND              | 141        | I/O              |
| 13         | I/O              | 56         | I/O              | 99         | I/O              | 142        | I/O              |
| 14         | I/O              | 57         | I/O              | 100        | I/O              | 143        | I/O              |
| 15         | I/O              | 58         | I/O              | 101        | I/O              | 144        | I/O              |
| 16         | I/O              | 59         | I/O              | 102        | I/O              | 145        | I/O              |
| 17         | I/O              | 60         | V <sub>CCA</sub> | 103        | I/O              | 146        | I/O              |
| 18         | I/O              | 61         | GND              | 104        | I/O              | 147        | I/O              |
| 19         | I/O              | 62         | GND              | 105        | I/O, (WD)        | 148        | I/O              |
| 20         | I/O              | 63         | NC               | 106        | I/O, (WD)        | 149        | I/O              |
| 21         | I/O              | 64         | NC               | 107        | I/O              | 150        | I/O              |
| 22         | I/O              | 65         | NC               | 108        | I/O              | 151        | I/O              |
| 23         | I/O              | 66         | I/O              | 109        | I/O, (WD)        | 152        | I/O              |
| 24         | I/O              | 67         | SDO, TDO, I/O    | 110        | I/O, (WD)        | 153        | I/O              |
| 25         | I/O              | 68         | I/O              | 111        | I/O              | 154        | I/O              |
| 26         | V <sub>CCA</sub> | 69         | I/O (WD)         | 112        | QCLKA, I/O       | 155        | V <sub>CCA</sub> |
| 27         | I/O              | 70         | I/O (WD)         | 113        | I/O              | 156        | I/O              |
| 28         | I/O              | 71         | I/O              | 114        | GND              | 157        | I/O              |
| 29         | V <sub>CCA</sub> | 72         | V <sub>CCI</sub> | 115        | I/O              | 158        | V <sub>CCA</sub> |
| 30         | V <sub>CCI</sub> | 73         | I/O              | 116        | I/O              | 159        | V <sub>CCI</sub> |
| 31         | GND              | 74         | I/O              | 117        | I/O              | 160        | GND              |
| 32         | V <sub>CCA</sub> | 75         | I/O              | 118        | I/O              | 161        | I/O              |
| 33         | GND              | 76         | I/O (WD)         | 119        | V <sub>CCI</sub> | 162        | I/O              |
| 34         | TCK, I/O         | 77         | GND              | 120        | I/O              | 163        | I/O              |
| 35         | I/O              | 78         | I/O, (WD)        | 121        | I/O, (WD)        | 164        | I/O              |
| 36         | GND              | 79         | I/O              | 122        | I/O, (WD)        | 165        | GND              |
| 37         | I/O              | 80         | QCLKB, I/O       | 123        | I/O              | 166        | I/O              |
| 38         | I/O              | 81         | I/O              | 124        | I/O              | 167        | I/O              |
| 39         | I/O              | 82         | I/O              | 125        | I/O              | 168        | I/O              |
| 40         | I/O              | 83         | I/O              | 126        | I/O              | 169        | I/O              |
| 41         | I/O              | 84         | I/O              | 127        | GND              | 170        | V <sub>CCA</sub> |
| 42         | I/O              | 85         | I/O              | 128        | NC               | 171        | I/O              |
| 43         | I/O              | 86         | I/O              | 129        | NC               | 172        | I/O              |

**256-Pin CQFP (Continued)**

| Pin Number | A42MX36 Function | Pin Number | A42MX36 Function | Pin Number | A42MX36 Function | Pin Number | A42MX36 Function |
|------------|------------------|------------|------------------|------------|------------------|------------|------------------|
| 173        | I/O              | 194        | I/O              | 215        | I/O (WD)         | 236        | I/O              |
| 174        | I/O              | 195        | DCLK, I/O        | 216        | I/O (WD)         | 237        | I/O              |
| 175        | I/O              | 196        | I/O              | 217        | I/O              | 238        | I/O              |
| 176        | I/O              | 197        | I/O              | 218        | PRB, I/O         | 239        | I/O              |
| 177        | I/O              | 198        | I/O              | 219        | I/O              | 240        | QCLKD, I/O       |
| 178        | I/O              | 199        | I/O (WD)         | 220        | CLKB, I/O        | 241        | I/O              |
| 179        | I/O              | 200        | I/O (WD)         | 221        | I/O              | 242        | I/O (WD)         |
| 180        | GND              | 201        | V <sub>CCI</sub> | 222        | GND              | 243        | GND              |
| 181        | I/O              | 202        | I/O              | 223        | GND              | 244        | I/O (WD)         |
| 182        | I/O              | 203        | I/O              | 224        | V <sub>CCA</sub> | 245        | I/O              |
| 183        | I/O              | 204        | I/O              | 225        | V <sub>CCI</sub> | 246        | I/O              |
| 184        | I/O              | 205        | I/O              | 226        | I/O              | 247        | I/O              |
| 185        | I/O              | 206        | GND              | 227        | CLKA, I/O        | 248        | V <sub>CCI</sub> |
| 186        | I/O              | 207        | I/O              | 228        | I/O              | 249        | I/O              |
| 187        | I/O              | 208        | I/O              | 229        | PRA, I/O         | 250        | I/O (WD)         |
| 188        | MODE             | 209        | QCLKC, I/O       | 230        | I/O              | 251        | I/O (WD)         |
| 189        | V <sub>CCA</sub> | 210        | I/O              | 231        | I/O              | 252        | I/O              |
| 190        | GND              | 211        | I/O (WD)         | 232        | I/O (WD)         | 253        | SDI, I/O         |
| 191        | NC               | 212        | I/O (WD)         | 233        | I/O (WD)         | 254        | I/O              |
| 192        | NC               | 213        | I/O              | 234        | I/O              | 255        | GND              |
| 193        | NC               | 214        | I/O              | 235        | I/O              | 256        | NC               |

Package Pin Assignments (continued)

272-Pin BGA Package (Top View)



**272-Pin PBGA**

| Ball | A42MX36 Function | Ball | A42MX36 Function | Ball | A42MX36 Function | Ball | A42MX36 Function |
|------|------------------|------|------------------|------|------------------|------|------------------|
| A1   | GND              | C4   | I/O              | E19  | I/O              | K10  | GND              |
| A2   | GND              | C5   | I/O (WD)         | E20  | I/O              | K11  | GND              |
| A3   | I/O              | C6   | I/O              | F1   | I/O              | K12  | GND              |
| A4   | I/O (WD)         | C7   | QCLKC, I/O       | F2   | I/O              | K17  | I/O              |
| A5   | I/O              | C8   | I/O              | F3   | I/O              | K18  | V <sub>CCA</sub> |
| A6   | I/O              | C9   | I/O              | F4   | V <sub>CCI</sub> | K19  | V <sub>CCA</sub> |
| A7   | I/O (WD)         | C10  | CLKB             | F17  | I/O              | K20  | GND (LP)         |
| A8   | I/O (WD)         | C11  | PRA, I/O         | F18  | I/O              | L1   | I/O              |
| A9   | I/O              | C12  | I/O (WD)         | F19  | I/O              | L2   | I/O              |
| A10  | I/O              | C13  | I/O              | F20  | I/O              | L3   | V <sub>CCA</sub> |
| A11  | CLKA             | C14  | QCLKD, I/O       | G1   | I/O              | L4   | V <sub>CCA</sub> |
| A12  | I/O              | C15  | I/O              | G2   | I/O              | L9   | GND              |
| A13  | I/O              | C16  | I/O (WD)         | G3   | I/O              | L10  | GND              |
| A14  | I/O              | C17  | SDI, I/O         | G4   | V <sub>CCI</sub> | L11  | GND              |
| A15  | I/O              | C18  | I/O              | G17  | V <sub>CCI</sub> | L12  | GND              |
| A16  | I/O (WD)         | C19  | I/O              | G18  | I/O              | L17  | V <sub>CCI</sub> |
| A17  | I/O              | C20  | I/O              | G19  | I/O              | L18  | I/O              |
| A18  | I/O              | D1   | I/O              | G20  | I/O              | L19  | I/O              |
| A19  | GND              | D2   | I/O              | H1   | I/O              | L20  | TCK, I/O         |
| A20  | GND              | D3   | I/O              | H2   | I/O              | M1   | I/O              |
| B1   | GND              | D4   | I/O              | H3   | I/O              | M2   | I/O              |
| B2   | GND              | D5   | V <sub>CCI</sub> | H4   | V <sub>CCA</sub> | M3   | I/O              |
| B3   | DCLK, I/O        | D6   | I/O              | H17  | I/O              | M4   | V <sub>CCI</sub> |
| B4   | I/O              | D7   | I/O              | H18  | I/O              | M9   | GND              |
| B5   | I/O              | D8   | V <sub>CCA</sub> | H19  | I/O              | M10  | GND              |
| B6   | I/O              | D9   | I/O (WD)         | H20  | I/O              | M11  | GND              |
| B7   | I/O (WD)         | D10  | V <sub>CCI</sub> | J1   | I/O              | M12  | GND              |
| B8   | I/O              | D11  | I/O              | J2   | I/O              | M17  | I/O              |
| B9   | PRB, I/O         | D12  | V <sub>CCI</sub> | J3   | I/O              | M18  | I/O              |
| B10  | I/O              | D13  | I/O              | J4   | V <sub>CCI</sub> | M19  | I/O              |
| B11  | I/O              | D14  | V <sub>CCI</sub> | J9   | GND              | M20  | I/O              |
| B12  | I/O (WD)         | D15  | I/O              | J10  | GND              | N1   | I/O              |
| B13  | I/O              | D16  | V <sub>CCA</sub> | J11  | GND              | N2   | I/O              |
| B14  | I/O              | D17  | GND              | J12  | GND              | N3   | I/O              |
| B15  | I/O (WD)         | D18  | I/O              | J17  | V <sub>CCA</sub> | N4   | V <sub>CCI</sub> |
| B16  | I/O              | D19  | I/O              | J18  | I/O              | N17  | V <sub>CCI</sub> |
| B17  | I/O (WD)         | D20  | I/O              | J19  | I/O              | N18  | I/O              |
| B18  | I/O              | E1   | I/O              | J20  | I/O              | N19  | I/O              |
| B19  | GND              | E2   | I/O              | K1   | I/O              | N20  | I/O              |
| B20  | GND              | E3   | I/O              | K2   | I/O              | P1   | I/O              |
| C1   | I/O              | E4   | V <sub>CCA</sub> | K3   | I/O              | P2   | I/O              |
| C2   | MODE             | E17  | V <sub>CCI</sub> | K4   | V <sub>CCI</sub> | P3   | I/O              |
| C3   | GND              | E18  | I/O              | K9   | GND              | P4   | V <sub>CCA</sub> |



272-Pin PBGA (Continued)

| Ball | A42MX36<br>Function | Ball | A42MX36<br>Function | Ball | A42MX36<br>Function | Ball | A42MX36<br>Function |
|------|---------------------|------|---------------------|------|---------------------|------|---------------------|
| P17  | I/O                 | U6   | I/O (WD)            | V11  | I/O                 | W16  | I/O (WD)            |
| P18  | I/O                 | U7   | I/O                 | V12  | I/O                 | W17  | I/O                 |
| P19  | I/O                 | U8   | I/O                 | V13  | I/O (WD)            | W18  | I/O (WD)            |
| P20  | I/O                 | U9   | I/O (WD)            | V14  | I/O                 | W19  | GND                 |
| R1   | I/O                 | U10  | V <sub>CCA</sub>    | V15  | I/O (WD)            | W20  | GND                 |
| R2   | I/O                 | U11  | V <sub>CCI</sub>    | V16  | I/O                 | Y1   | GND                 |
| R3   | I/O                 | U12  | I/O                 | V17  | I/O                 | Y2   | GND                 |
| R4   | V <sub>CCI</sub>    | U13  | I/O                 | V18  | SDO, TDO, I/O       | Y3   | I/O                 |
| R17  | V <sub>CCI</sub>    | U14  | QCLKB, I/O          | V19  | I/O                 | Y4   | TDI, I/O            |
| R18  | I/O                 | U15  | I/O                 | V20  | I/O                 | Y5   | I/O (WD)            |
| R19  | I/O                 | U16  | V <sub>CCI</sub>    | W1   | GND                 | Y6   | I/O                 |
| R20  | I/O                 | U17  | I/O                 | W2   | GND                 | Y7   | QCLKA, I/O          |
| T1   | I/O                 | U18  | GND                 | W3   | I/O                 | Y8   | I/O                 |
| T2   | I/O                 | U19  | I/O                 | W4   | TMS, I/O            | Y9   | I/O                 |
| T3   | I/O                 | U20  | I/O                 | W5   | I/O                 | Y10  | I/O                 |
| T4   | I/O                 | V1   | I/O                 | W6   | I/O                 | Y11  | I/O                 |
| T17  | V <sub>CCA</sub>    | V2   | I/O                 | W7   | I/O                 | Y12  | I/O                 |
| T18  | I/O                 | V3   | GND                 | W8   | I/O (WD)            | Y13  | I/O                 |
| T19  | I/O                 | V4   | GND                 | W9   | I/O (WD)            | Y14  | I/O                 |
| T20  | I/O                 | V5   | I/O                 | W10  | I/O                 | Y15  | I/O                 |
| U1   | I/O                 | V6   | I/O                 | W11  | I/O                 | Y16  | I/O                 |
| U2   | I/O                 | V7   | I/O                 | W12  | I/O                 | Y17  | I/O                 |
| U3   | I/O                 | V8   | I/O (WD)            | W13  | I/O (WD)            | Y18  | I/O (WD)            |
| U4   | I/O                 | V9   | I/O                 | W14  | I/O                 | Y19  | GND                 |
| U5   | V <sub>CCI</sub>    | V10  | I/O                 | W15  | I/O                 | Y20  | GND                 |

## List of Changes

The following table lists critical changes that were made in the current version of the document.

| Previous version | Changes in current version (v6.0)  | Page |
|------------------|--|------|
| v4.0.1           | <p>Because the changes in this data sheet are extensive and technical in nature, this should be viewed as a new document. Please read it as you would a data sheet that is published for the first time.</p> <p>Note that the “Package Characteristics and Mechanical Drawings” section has been eliminated from the data sheet. The mechanical drawings are now contained in a separate document, “Package Characteristics and Mechanical Drawings,” available on the Actel web site.</p> | ALL  |

## Data Sheet Categories

In order to provide the latest information to designers, some data sheets are published before data has been fully characterized. These data sheets are marked as “Advanced” or Preliminary” data sheets. The definition of these categories are as follows:

### Advanced

The data sheet contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

### Preliminary

The data sheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

### Unmarked (production)

The data sheet contains information that is considered to be final.



Actel and the Actel logo are registered trademarks of Actel Corporation.  
All other trademarks are the property of their owners.



<http://www.actel.com>

**Actel Europe Ltd.**

Daneshill House, Lutyens Close  
Basingstoke, Hampshire RG24 8AG  
United Kingdom

**Tel:** +44 (0)1256 305600

**Fax:** +44 (0)1256 355420

**Actel Corporation**

955 East Arques Avenue  
Sunnyvale, California 94086  
USA

**Tel:** (408) 739-1010

**Fax:** (408) 739-1540

**Actel Asia-Pacific**

EXOS Ebisu Bldg. 4F  
1-24-14 Ebisu Shibuya-ku  
Tokyo 150 Japan

**Tel:** +81 03-3445-7671

**Fax:** +81 03-3445-7668