

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK4212 is N-channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for low voltage high current applications such as DC/DC converter with synchronous rectifier.

FEATURES

- Low on-state resistance
 $R_{DS(on)1} = 7.8 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 30 \text{ A)}$
 $R_{DS(on)2} = 14 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 20 \text{ A)}$
- Low total gate charge
 $Q_G = 27 \text{ nC TYP. (} V_{DD} = 15 \text{ V, } V_{GS} = 10 \text{ V, } I_D = 30 \text{ A)}$
- 4.5 V drive available
- Avalanche capability ratings

ORDERING INFORMATION

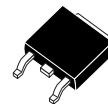
PART NUMBER	LEAD PLATING	PACKING	PACKAGE
2SK4212-ZK-E1-AY ^{Note}	Pure Sn (Tin)	Tape 2500 p/reel	TO-252 (MP-3ZK) typ. 0.27 g
2SK4212-ZK-E2-AY ^{Note}			

Note Pb-free (This product does not contain Pb in external electrode).

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	25	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 48	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 144	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T1}	35	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_{T2}	1.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$
Single Avalanche Current ^{Note2}	I_{AS}	17	A
Single Avalanche Energy ^{Note2}	E_{AS}	28.9	mJ

(TO-252)



Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

2. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 12.5 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$, $L = 0.1 \text{ mH}$

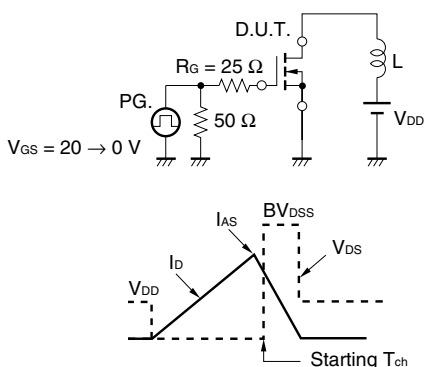
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ELECTRICAL CHARACTERISTICS (T_A = 25°C)

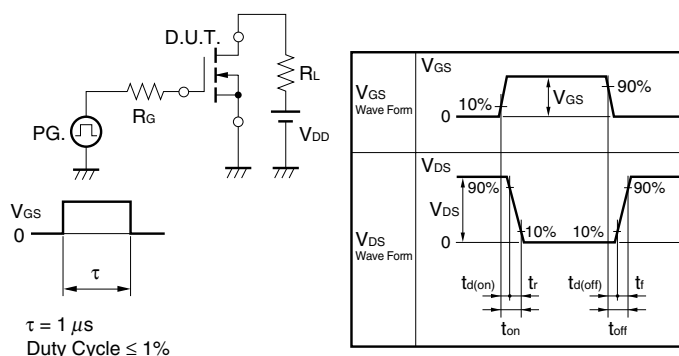
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 25 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±16 V, V _{DS} = 0 V			±100	nA
Gate to Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.5		3.0	V
Forward Transfer Admittance Note	y _{fs}	V _{DS} = 5 V, I _D = 12 A	10	22		S
Drain to Source On-state Resistance Note	R _{DS(on)1}	V _{GS} = 10 V, I _D = 30 A		5.5	7.8	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 20 A		8.5	14	mΩ
Input Capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V,		1200		pF
Output Capacitance	C _{oss}	f = 1 MHz		220		pF
Reverse Transfer Capacitance	C _{rss}			140		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 15 V, I _D = 30 A,		16		ns
Rise Time	t _r	V _{GS} = 10 V,		14		ns
Turn-off Delay Time	t _{d(off)}	R _G = 3 Ω		45		ns
Fall Time	t _f			11		ns
Total Gate Charge	Q _G	V _{DD} = 15 V,		27		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V,		4		nC
Gate to Drain Charge	Q _{GD}	I _D = 30 A		7		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = 30 A, V _{GS} = 0 V		0.88	1.5	V
Reverse Recovery Time	t _{rr}	I _F = 30 A, V _{GS} = 0 V,		26		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		14		nC

Note Pulsed

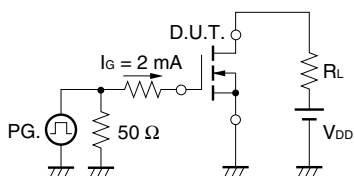
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

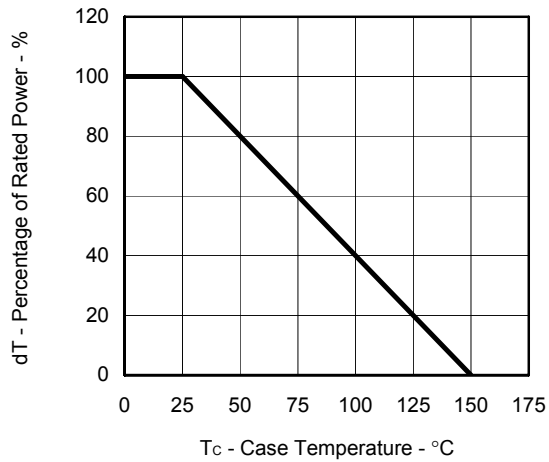


TEST CIRCUIT 3 GATE CHARGE

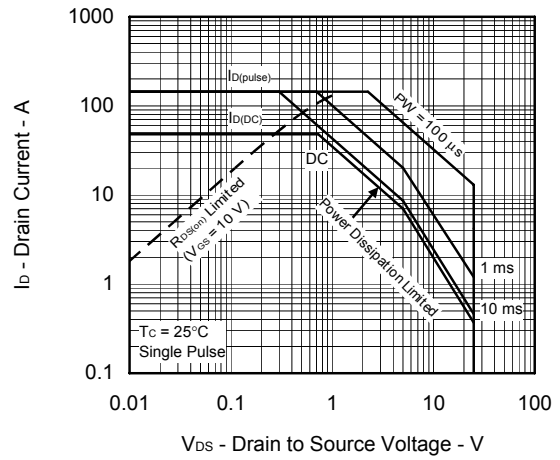


TYPICAL CHARACTERISTICS (T_A = 25°C)

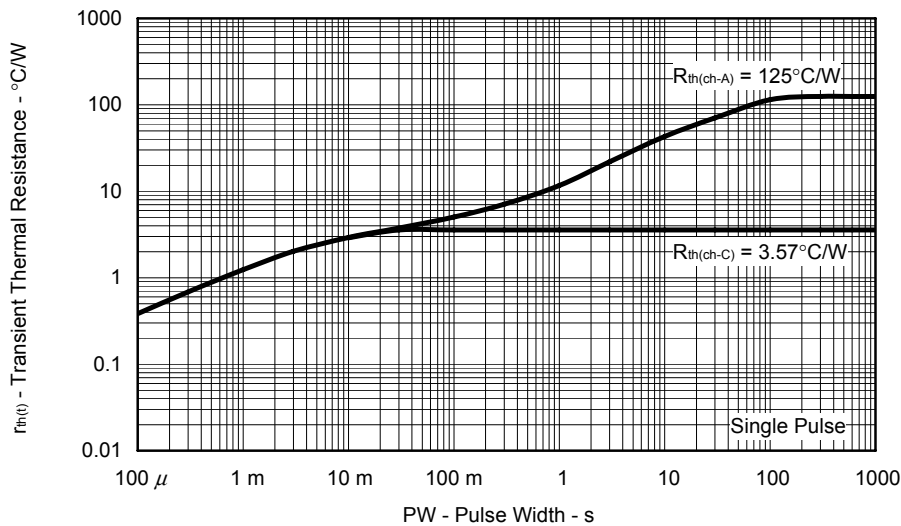
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



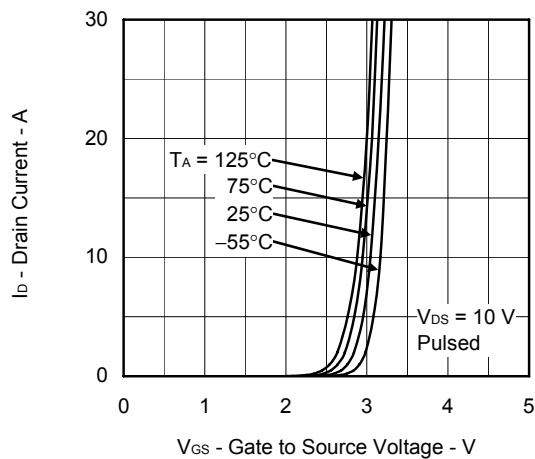
FORWARD BIAS SAFE OPERATING AREA



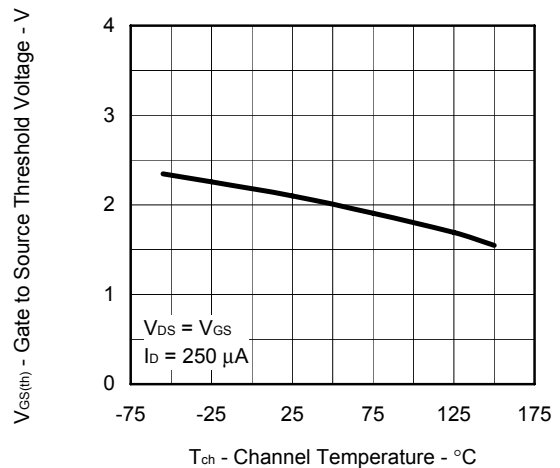
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

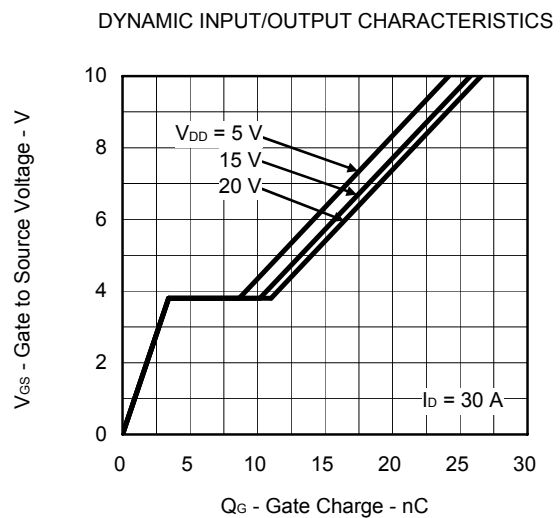
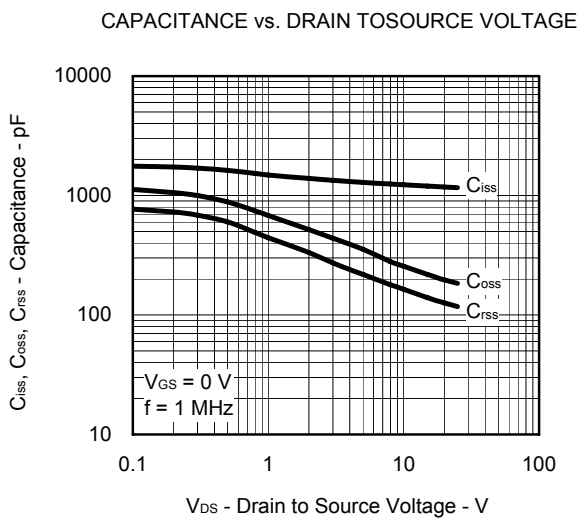
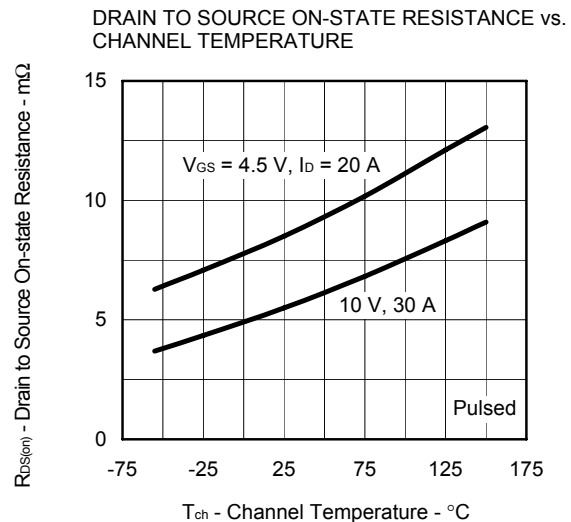
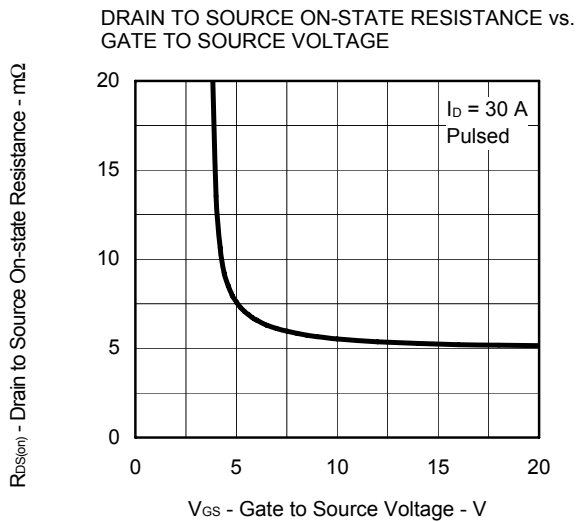
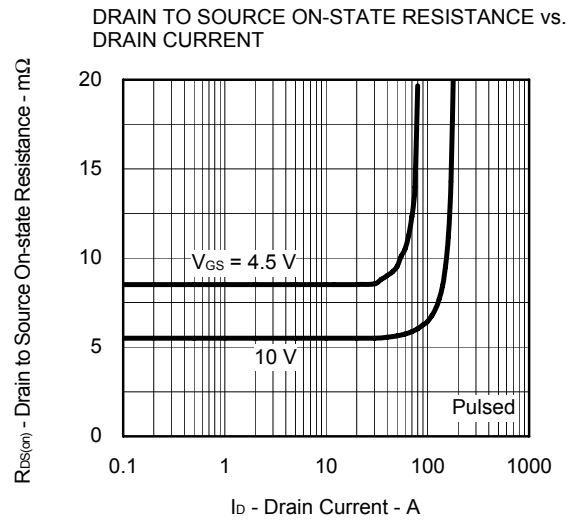
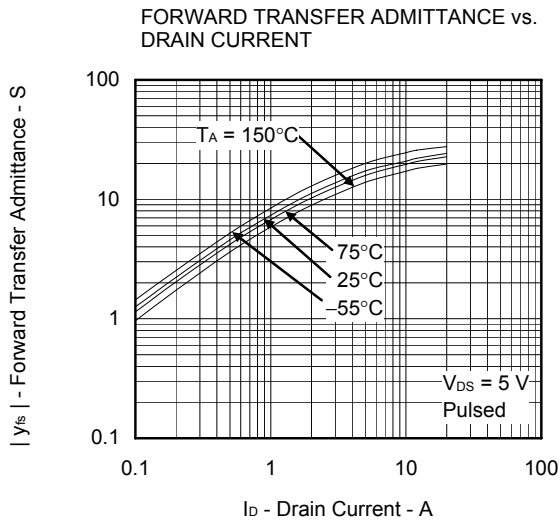


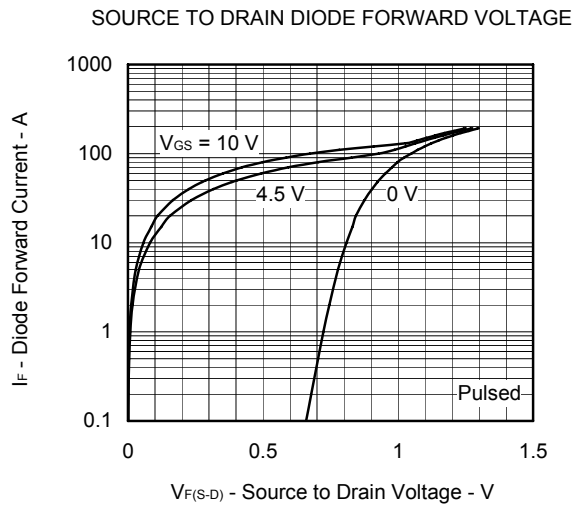
FORWARD TRANSFER CHARACTERISTICS



GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

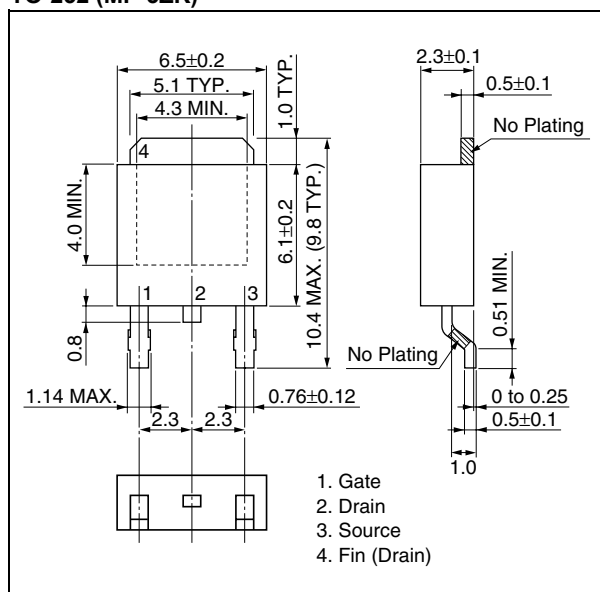




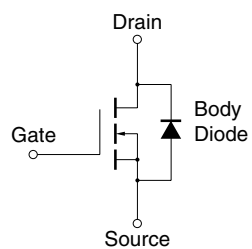


PACKAGE DRAWINGS (Unit: mm)

TO-252 (MP-3ZK)



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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